A Low Power Frequency Synthesizer for 60-GHz Wireless Personal Area Networks

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***Abstract*—In this brief, a 60-GHz frequency synthesizer for wireless personal area networks is designed using 0.13-μm CMOS technology. The synthesizer operates at 60 GHz with phase noises of −98, −117, and −128 dBc/Hz at 1-, 10-, and 40-MHz frequency offsets, respectively. The 60-GHz clock is generated by combining a phase-locked loop (PLL) and an injection-locked oscillator. The PLL provides frequency tuning of the 60-GHz voltage-controlled oscillator (VCO) using replica tuning. A pulse train is generated using a novel passive delay-locked loop and a CMOS pulse generator. This pulse train is then used for filtering the phase noise of 60-GHz VCO up to a high offset frequency. The total power consumption of the frequency synthesizer is 57 mW with a 1.2-V power supply.**

***Index Terms*—Delay-locked loop (DLL), edge combiner, frequency synthesizers, injection-locked oscillator (ILO), phase-locked loop (PLL).**

I. Introduction

THE UNLICENSED millimeter-wave industrial, scientific, and medical band around 60-GHz offers several advantages such as wider bandwidth and higher data rates. One of the key challenges in such systems is the design of a 60-GHz frequency synthesizer since its phase noise and frequency stability determine the sensitivity and bit error rate of the system. This brief focuses on the design of a 60-GHz frequency synthesizer with improved phase noise performance in comparison to existing architectures.

In Section II, the design challenges of a single phase-locked-loop (PLL)-based synthesizer are discussed. Then, we shall review and evaluate existing solutions for the 60-GHz synthesizer. In Section III, our proposed architecture will be presented. Implementation and simulation results will then be discussed in Sections IV and V, respectively. This brief is concluded in Section VI.

II. Design Challenges of the 60-GHz Synthesizer

Conventionally, PLLs are used for frequency synthesis. Each PLL requires a reference signal with good phase noise, which is usually met by an off-chip crystal oscillator. Typically, a crystal oscillator operates around 100 MHz. If a single PLL is used for generating a 60-GHz signal from this 100-MHz reference, then the multiplication ratio becomes large and results in several design challenges, for example, low PLL bandwidth and the need of a high-frequency divider.

The phase noise of a 60-GHz voltage-controlled oscillator (VCO) is significantly poorer compared with its lower frequency counterpart. Thus, a higher PLL bandwidth is desired to filter VCO phase noise. To overcome this problem, cascaded or dual PLLs [1] may be used. In this design, the first PLL offers significant part of the multiplication ratio. The second PLL provides an advantage of having a wider bandwidth for suppressing more VCO phase noise. Although this architecture is one possible solution for better phase noise filtering, it suffers from the complexity of designing high-frequency divider, phase-frequency detector, and charge pump.

For subsiding the design complexities of 60-GHz divider, buffer, etc., the second PLL can be replaced by an injection-locked oscillator (ILO) [2]. However, injecting the output of the VCO directly to the ILO introduces high-frequency spurs and results in a narrower lock range. Furthermore, the lack of a frequency-tracking loop for the 60-GHz VCO makes it an open-loop solution, and hence, it is process, voltage, and temperature (PVT) intolerant. In [3], a 60-GHz ring oscillator is injected with a 20-GHz reference. In our application, the reference frequency is only 150 MHz. Therefore, to generate a higher frequency reference, a PLL is required. In addition, to achieve better phase noise, an LC VCO is preferred instead of a ring VCO.

III. Proposed Architecture

In order to alleviate the high-frequency spurs of PLL–ILO solution [2], in the proposed architecture [see Fig. 1(a)], the ILO is injected with narrow pulses generated by the pulse generator. It is well known that the locking range and the bandwidth of an ILO reduce with increased multiplication ratio. Therefore, to relax the ILO's multiplication factor and thus increase its tracking bandwidth, a delay-locked loop (DLL) is used to generate additional phases of the PLL's output, which eventually generated additional pulses in the pulse generator. In this design, the DLL generated four phases of the 5-GHz PLL output. Using these phases, the pulse generator generated a pulse train with periodicity of 50 ps, i.e., fundamental frequency at 20 GHz. Thus, the 60-GHz VCO's free-running phase noise is now accumulated for only 3 clock cycles, increasing the bandwidth and the locking range. To further increase the locking range of the ILO, reduce frequency offset, and make the system PVT tolerant, a frequency-tracking loop was added.

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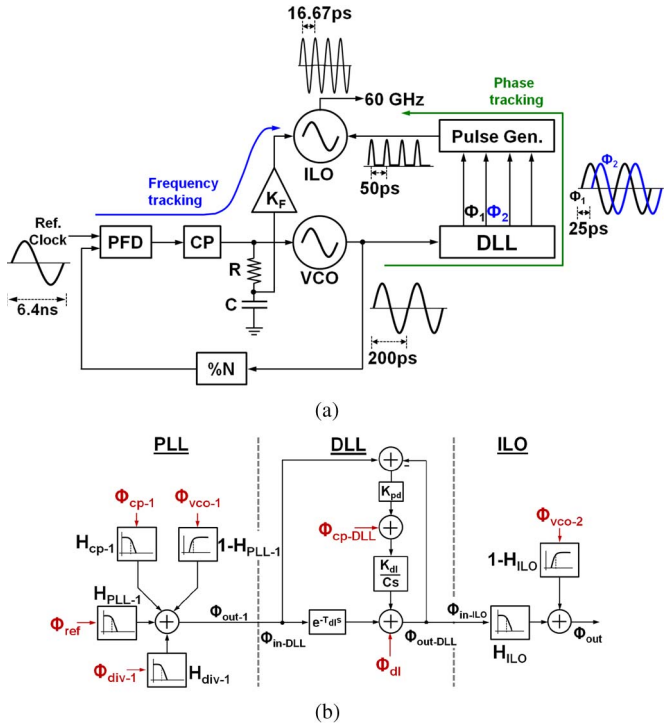


Fig. 1. Proposed frequency synthesizer (a) block diagram and (b) linear phase-domain model.

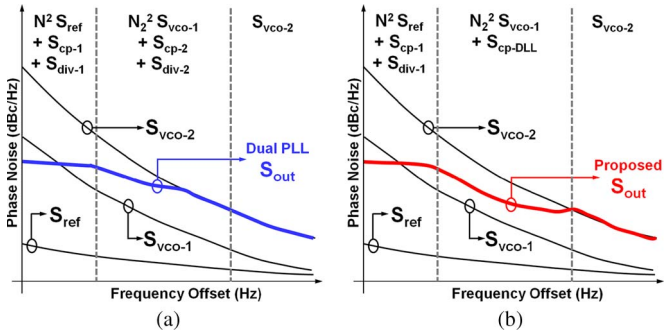


Fig. 2. Output phase noise of (a) dual PLL and (b) proposed architecture.

The first PLL achieves two functions, i.e., 1) it multiplies the 156.25-MHz reference to generate a 5-GHz clock, and 2) using replica tuning, it centers the second VCO around 60 GHz.

The phase noise of the conventional dual PLL can be separated in three regions, as shown in Fig. 2(a). At very low frequency (within the first PLL bandwidth), the phase noise is dominated by the reference noise amplified by the multiplication ratio $(N^2 S_{\rm ref})$. In addition, charge pump $S_{\rm cp-1}$ and divider $S_{\rm div-1}$ phase noises are also amplified and shaped by the PLL transfer function increasing total phase noise at low frequencies.

At midfrequency offset (beyond the bandwidth of the first PLL and within the bandwidth of the second PLL), phase noise is dominated by the first VCO's phase noise $(N_2^2 S_{\rm vco-1})$ and charge pump and divider noise of the second PLL. Note that cascading of PLLs is useful only when $S_{\rm vco-2} > S_{\rm vco-1}|1 - H_{\rm PLL-1}|^2 |H_{\rm PLL-2}|^2 + S_{\rm cp-2}|H_{\rm cp-2}|^2 + S_{\rm div-2}|H_{\rm div-2}|^2$. Here, $H_{\rm PLL}$, $H_{\rm cp}$, and $H_{\rm div}$ are well-known transfer functions of input, charge pump, and divider, respectively [4]. Finally, beyond the second PLL bandwidth, the output phase noise is dominated by the phase noise of the second VCO$(S_{\rm vco-2})$.

In the proposed architecture, the second PLL is replaced by a DLL and an ILO. The equivalent phase-domain model is shown in Fig. 1(b), where the first PLL behaves similar to a dual PLL. The output phase noise of the DLL $S_{\rm out-DLL}$ is given by

$$S_{\rm out-DLL} = S_{\rm in-DLL}|H_{\rm DLL}|^2 + S_{\rm cp-DLL}|H_{\rm cp-DLL}|^2 + S_{\rm dl}|H_{\rm dl}|^2 \quad (1)$$

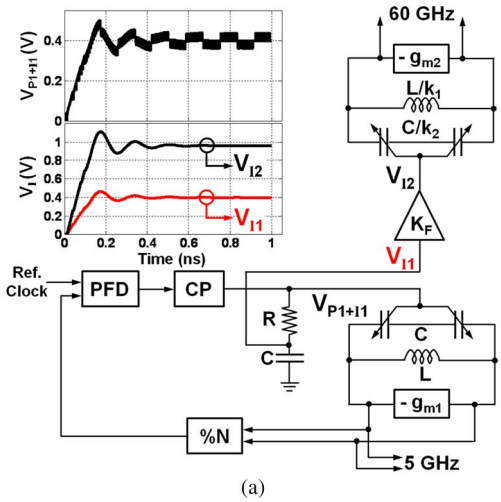
where $S_{\rm in-DLL}$, $S_{\rm cp-DLL}$, and $S_{\rm dl}$ are the phase noises generated at the input, charge pump, and delay line. From Fig. 1(b), DLL's input, charge pump, and delay-line transfer functions can be derived as $H_{\rm DLL} = (1 + se^{\tau_{\rm dl}s}/\omega_p)/(1 + s/\omega_p)$, $H_{\rm cp-DLL} = (1/K_{\rm pd})/(1 + s/\omega_p)$, and $H_{\rm dl} = (s/\omega_p)/(1 + s/\omega_p)$, respectively. Here, ω_p is the DLL bandwidth, $K_{\rm pd}$ is the phase detector (PD) gain, and $\tau_{\rm dl}$ is the total delay introduced by the delay line [5].

The ILO behaves similar to a PLL without having any phase noise contribution from a charge pump or divider. As shown in Fig. 2(b), the output phase noise of the proposed PLL shows significant improvement in the center region mainly due to two reasons, i.e., 1) the ILO has a larger bandwidth compared to the PLL, and hence, the 60-GHz VCO noise is filtered up to high frequencies, and 2) DLL and ILO do not require any divider. Therefore, the overall phase noise is improved by $S_{\rm div-2}|H_{\rm div-2}|^2$ compared to the dual-PLL architecture.

IV. Implementation

A. Five-GHz PLL and Replica Frequency Tracking

The main concept of replica tuning is that, when the control voltage of the first PLL centers its VCO frequency at 5 GHz, the second VCO of the ILO is also centered at 60 GHz. To implement this replica tuning concept, the control voltage of the 5-GHz VCO will be used to tune the free-running frequency of the 60-GHz VCO. Note that the control voltage of the 5-GHz VCO is continuously adjusted by the PLL; hence, it tends to be noisy, as shown in Fig. 3(a). A more stable control voltage can be obtained by using only the integral path output V_{I1}, which completely captures the required frequency information. Thus, a scaled version of V_{I1} is used to adjust the control voltage of the 60-GHz VCO, i.e., V_{I2}. In an ideal scenario, any frequency change Δf in the 5-GHz VCO should be also reflected as $12 \times \Delta f$ in the 60-GHz VCO. To make this happen, the required condition is $K_{\rm vco-2} = 12 \times K_{\rm vco-1}$, which is difficult to achieve in practical implementation. Since the frequency of oscillation is determined by the product $LC(f_o = 1/2\pi\sqrt{LC})$, the 5-GHz tank's LC product needs to be 144 times that of the 60-GHz tank. Inductor L and capacitor C used for the 5-GHz tank were 1 nH and 1 pF, respectively. However, at higher frequencies, the parasitic capacitance dominated the overall tank capacitance C. Therefore, to keep a reasonable tuning range at the 60-GHz tank, inductance L was scaled by 24 and capacitance C was scaled by 6, which lead to 42 pH and 167 fF, respectively, as shown in Fig. 3(a). Usually, this reduction in the L/C ratio degrades the quality factor and the phase noise of the VCO. Since the ILO has a wider bandwidth,



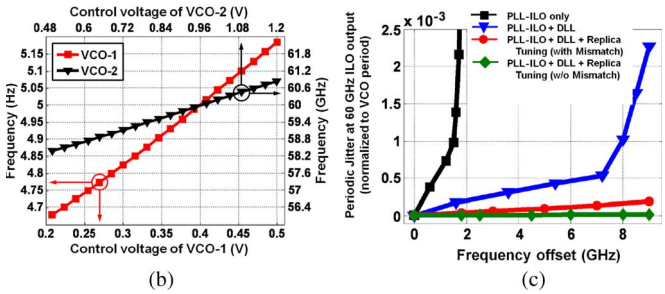


Fig. 3. (a) Frequency tracking of the VCOs with $K_1 = 24$ and $K_2 = 6$. (b) Frequency-tuning curve for 5- and 60-GHz VCOs. (c) Jitter plot of ILO for different injections.

most of this phase noise will be filtered. Note that in our implementation, the gain of VCO-2, i.e., $K_{\text{vco}-2}$, is five times that of VCO-1, i.e., $K_{\text{vco}-1}$. Therefore, gain block K_F is used to amplify the control voltage by $12 \times K_{\text{vco}-1}/K_{\text{vco}-2} = 2.4$. For PVT tolerance, this amplifier may be kept tunable such that its amplification factor may be initially adjusted. During operation, any further mismatch between the VCOs would cause the natural frequency of the 60-GHz VCO to slightly divert from 12 times VCO-1's frequency, but, for as long as it is within the locking range of ILO, the output frequency would always be 12 times that of VCO-1's frequency. However, this frequency error will be still significantly less compared to an open-loop solution without any frequency tracking. Note that the frequency offset between the natural and locked frequencies of the ILO would cause periodic jitter, as shown in Fig. 3(c). An advantage of the DLL and replica tuning over the existing simple PLL–ILO solution can be observed from the improved periodic jitter performance. The DLL creates additional injection pulses limiting the jitter accumulation to 3 clock cycles only. Using replica tuning frequency offset is further reduced, and as a result, combining these two techniques significantly improves the periodic jitter of the ILO.

When the ILO is injected with 5-GHz pulse train, the locking range was around 1.5 GHz, i.e., 2.5% of its center frequency. When injected with 20-GHz pulse train, the locking range improved to more than 8% of its center frequency. When a frequency-tracking loop is added, only the tuning range of the 60-GHz VCO limits the locking range of the ILO, which was around 15% (9 GHz).

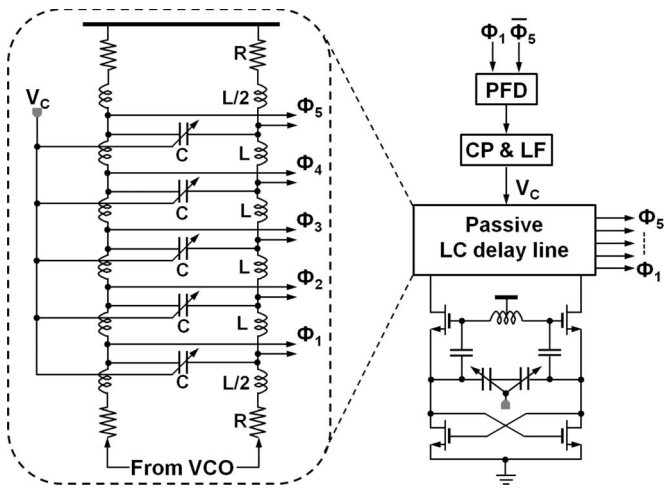


Fig. 4. Five-GHz VCO with passive DLL.

B. DLL for Pulse Generation

1) DLL: A DLL consists of a delay line, PD, charge pump, and loop filter. Conventionally, active delay lines using buffers as delay cells are commonly used. For high-frequency operations and better supply noise rejection, current mode logic (CML) buffers are preferred over CMOS buffers but at a cost of higher power consumption. In this brief, passive delay lines are used to conserve power at the cost of larger area. It is well known that a DLL does not suffer from jitter accumulation, and the main source of jitter in a DLL is duty cycle distortion (DCD). In an active DLL, DCD jitter is amplified due to the limited bandwidth of the delay stage. However, in passive delay elements, due to their bandpass characteristics, DCD is rather filtered.

The passive delay line is stacked on top of the 5-GHz VCO, as shown in Fig. 4. The delay introduced by each stage of the differential LC delay line is given by $T_D = \sqrt{LC}$, where L and C are the inductance and the capacitance of each stage of the delay line, respectively [6]. In order to account for any mismatch in the delay line, the outputs of the first ϕ_1 and the last ϕ_5 delay stages were compared in the PD, and they were integrated by the charge pump and the loop filter to generate control voltage V_C. This control voltage controlled the capacitance C of the varactor such that the total delay introduced by the delay line was equal to half a clock cycle, i.e., 100 ps. For achieving a delay of 25 ps by each delay stage, L was chosen to have a value of 1.25 nH, and C was kept around 469.2 fF. The outputs of the delay line, i.e., from ϕ_1 to ϕ_4, were then inserted in the pulse generator. The passive delay line consumes 8.53 mW, which is significantly lower than the simulated active DLL that consumes about 50 mW. The downside of the passive DLL is the additional area consumed by the inductors. Similar to the active delay line, mismatch between different delay sections causes periodic jitter. However, the frequency of this periodic jitter is very high and will be significantly attenuated by the low-pass jitter transfer characteristics of the following ILO.

2) Pulse Generator: The pulse generator generates narrow pulses at the rising and falling edges of the 5-GHz input signal. This can be easily done by XOR-ing two consecutive outputs of the DLL. Unfortunately, CML XOR consumes additional power with direct-current offsets.

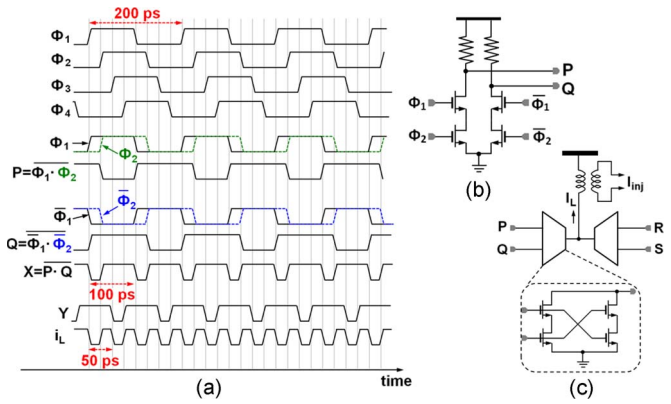


Fig. 5. (a) Timing diagram. (b) NAND gate. (c) Edge combiner.

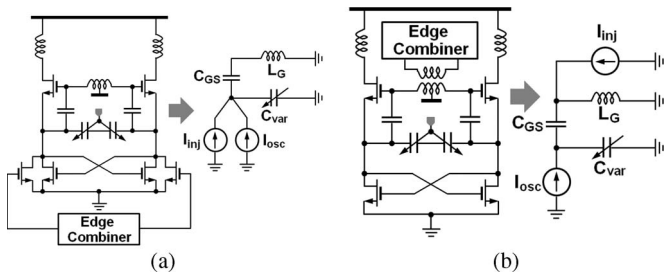


Fig. 6. ILO and its equivalent half-circuit with (a) active injection and (b) passive injection.

In our design, multiple CMOS NAND gates were used to perform XOR operations, as shown in the timing diagram in Fig. 5. The first two outputs of DLL, i.e., ϕ_1 and ϕ_2, and their complements, i.e., $\overline{\phi_1}$ and $\overline{\phi_2}$, were NAND-ed to get signals P and Q. Similarly, signals R and S were generated using the last two output phases. $P-Q$ and $R-S$ were NAND-ed again using symmetrical NAND gates to obtain the 10-GHz signals, i.e., X and Y. Their outputs were then combined together using the edge combiner, which generated a 20-GHz output current i_L (see Fig. 5).

C. ILO

The 20-GHz subrate pulse train generated from the DLL and the edge combiner is injected into the ILO. The ILO oscillates at 60-GHz center frequency, which is the third harmonic of its input.

There are two possible techniques of injections using an ILO. The first conventional method is known as active injection, i.e., a differential amplifier can be used to inject the pulse train into the VCO [see Fig. 6(a)] [7]. This conventional method leads to three limitations, i.e., 1) loading the critical nodes with additional capacitance of the differential pair leaves a small tuning range; 2) injection strength K is limited by the gain of the differential stage g_m, which is relatively low at 20 GHz; and 3) last, the differential pair used for injection consumes additional power. Hence, we consider the alternative method, which is to use passive injection using transformer coupling, as shown in Fig. 6(b). For the proposed injection method, the injection strength can be derived to be $K=(I_{\rm inj}/I_{\rm osc})(1+(C_{\rm var}/C_{GS}))$. Compared to the conventional injection factor $K=I_{\rm inj}/I_{\rm osc}$, injection strength is improved by $C_{\rm var}/C_{GS}$. In addition, capacitive loading on the LC tank is significantly reduced.

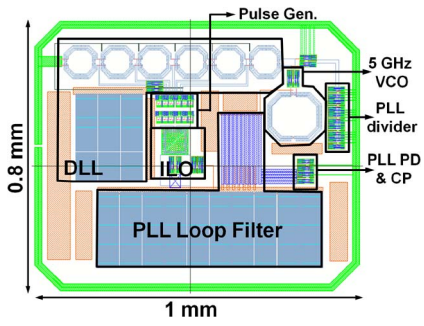


Fig. 7. Layout of the proposed frequency synthesizer.

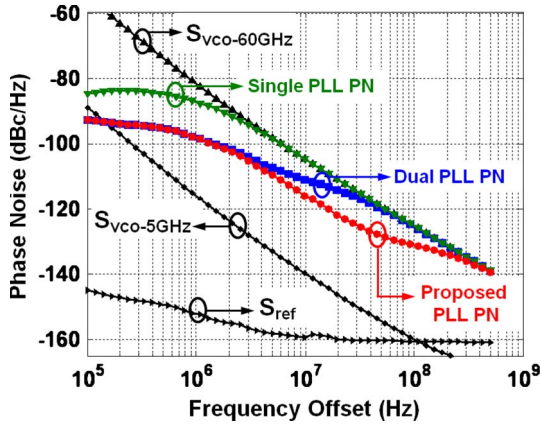


Fig. 8. Output phase noise.

V. Simulation Results

The proposed 60-GHz frequency synthesizer was simulated in transistor level over PVT in CMOS 0.13-μm technology using spectre in cadence environment. The total power consumed by the synthesizer from a 1.2-V power supply is 57 mW. The 5-GHz PLL along with the DLL consumed total power of 30.13 mW, and the 60-GHz ILO consumed 12-mW power. Additional 14.4-mW power was burned in the pulse generation circuitry. As shown in the layout in Fig. 7, the synthesizer was estimated to have an area of around 0.8 mm $\times$ 1 mm. The LC delay line is implemented with differential inductors, which reduced the area penalty. On-chip decoupling capacitors are used to reduce the power supply sensitivity in this design. For further improvement of supply rejection, regulators can be used.

For phase noise comparison, three types of frequency synthesizers were simulated to generate the 60-GHz clock from the 156.25-MHz reference signal (see Fig. 8). From transistor-level simulation (with extracted parasitic capacitance from the layout), the phase noise generated at the reference, VCO, charge pump, loop filter, and divider was captured. Equivalent noise sources are added in behavioral simulation in MATLAB similar to the technique described in [13]. The output noise obtained from transient time-domain behavioral simulation was then compared with the transistor-level phase noises shaped by theoretical transfer functions.

At very low frequencies, well within the PLL bandwidth, the output phase noise is same for all three cases, i.e., reference noise $S_{\rm ref}$ is amplified by $20\log(60\ {\rm GHz}/156.25\ {\rm MHz})=52$ dB. For single-PLL architecture, due to its large multiplication ratio, the bandwidth of the PLL was small, which is around 1.53 MHz. Note that close to its bandwidth, the

TABLE I
PERFORMANCE SUMMARY

	[8]	[9]	[10]	[11]	[12]	[2]	**This Work (simulated)**
Process	CMOS 90nm	CMOS 130 nm	CMOS 90 nm	Bi CMOS 130 nm	Bi CMOS 250 nm	CMOS 180 nm	CMOS 130 nm
Output (GHz)	61.1 – 63.3	45.9 – 50.5	58 - 60.4	56.5 - 63	50 - 53	53 – 58	60
Freq. Synth. Architecture	PLL	PLL	PLL	PLL + Tripler	PLL + Freq. Doubler	PLL +ILO	PLL + Pulse Gen.+ILO
Mult. Ratio f_{out}/f_{ref}	$\frac{62GHz}{60MHz}$	—	$\frac{60GHz}{230MHz}$	$\frac{63GHz}{285.7MHz}$	$\frac{53GHz}{262MHz}$	$\frac{55GHz}{350MHz}$	$\frac{60GHz}{156.25MHz}$
Power	78mW	57mW	80mW	144mW	160mW	35mW	57mW
VDD	1.2V	1.5 / 0.8 V	1.2 V	1.2 / 2.7V	2.5 V	1.8 V	1.2 V
Area (mm x mm)	0.6 x 0.6 (active)	1.16 x 0.75 (incl. pads)	0.95 x 1 (incl. pads)	0.68 x 1 (incl. pads)	1.2 x 1 (incl. pads)	0.96 x 0.84 (incl. pads)	0.8 x 1 (active)
Phase Noise (dBc)	-72@100KHz -80@1MHz	-64@50kHz -72@1MHz	-85@1MHz -99@10MHz	**For 16GHz:** -90@100KHz -124@10MHz	-73@100KHz -81@1MHz -102@10MHz	-85.2@1MHz -90.9@10MHz	-98@1MHz -117@10MHz -128@40MHz

high-pass filtered 60-GHz VCO phase noise is much larger than the low-pass filtered amplified reference noise; hence, the output noise has a peak around this region. Beyond its bandwidth, it followed the free-running phase noise of the 60-GHz VCO $S_{\mathrm{vco-60\,GHz}}$. The output phase noises of the 60-GHz signal were -87 dBc/Hz at 1 MHz, -105 dBc/Hz at 10 MHz, and -118 dBc/Hz at 40 MHz.

Compared to single PLL, dual PLL allows the flexibility of optimizing the bandwidth to lower the output phase noise. For simulation of the dual-PLL architecture, the first and second PLLs operated at 5 and 60 GHz with a bandwidth of 2.5 and 20 MHz, respectively. At a frequency offset of less than 2.5 MHz, the 60-GHz output phase noise followed that of S_{ref} amplified by 52 dB. For frequencies up to 20 MHz, $S_{\mathrm{vco-5\,GHz}}$, which is amplified by $20\log(60\ \mathrm{GHz}/5\ \mathrm{GHz}) = 21$ dB, dominated the output. Beyond this, it followed $S_{\mathrm{vco-60\,GHz}}$. For this design, the output phase noises were -98 dBc/Hz at 1 MHz, -111 dBc/Hz at 10 MHz, and -118.5 dBc/Hz at 40 MHz.

In the proposed approach, the 60-GHz VCO's phase noise can be filtered more efficiently, which further improves the overall phase noise of the synthesizer. Similar to dual-PLL architecture, the first PLL was designed to have a bandwidth of 2.5 MHz. The second PLL was replaced by a DLL, a pulse generator, and an ILO. Since DLL does not accumulate phase noise, its contribution to the overall phase noise is negligible. In our design, the ILO provided a multiplication factor of 3, and it had a bandwidth of 200 MHz. Similar to the dual-PLL design, the output phase noise followed the amplified S_{ref} up to 2.5 MHz. However, in this design, the ILO had a much larger bandwidth upon comparing to the second PLL in the dual-PLL architecture. Hence, the free-running phase noise of the 60-GHz VCO was filtered to much higher frequencies. This led to a significant output phase noise improvement between 10 and 100 MHz. The output phase noises for our proposed architecture were -98 dBc/Hz at 1 MHz, -117 dBc/Hz at 10 MHz, and -128 dBc/Hz at 40 MHz.

VI. CONCLUSION

In this brief, a 60-GHz DLL-based frequency synthesizer has been presented. The performance comparisons among the proposed 60-GHz frequency synthesizer and some recent studies are summarized in Table I. The phase noise performance of a CMOS synthesizer is poorer compared to their bi-CMOS counterpart [11], [12]. Within CMOS-based synthesizers, dual-loop solutions such as PLL–ILO [2] provide better phase noise and higher power efficiency compared to single-PLL architecture. The proposed solution further improves the PLL–ILO solution by reducing periodic jitter and improving lock range.

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