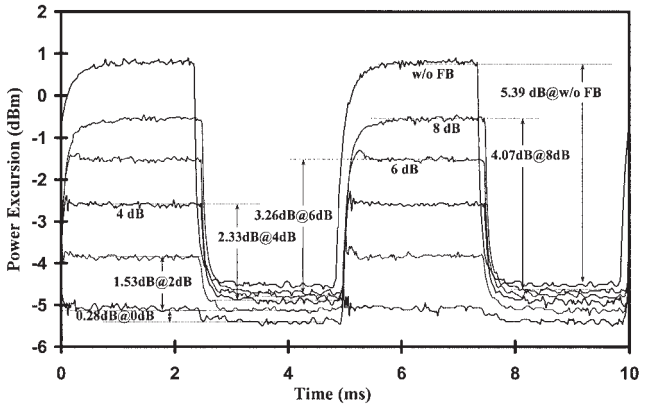

Figure 3 Amplified output for various feedback ASE attenuations at a per channel power of −25 dBm with maximum pump power of 97 mW

suppressed below 0.28 dB with slight transient behavior. A power spike, or overshoot, is observed at the leading edge of the output-signal pulse, which is followed by a steady-state gain condition. Progressive increments of the attenuation levels from 0 to 8 dB show increasing gain excursion, due to the attenuation increment reducing the feedback ASE levels of the three FBGs. The lowered levels enable a higher gain in the signal and vice versa, where the strongest clamping is seen at 0-dB attenuation.

The results of the pump-power variation used to arrest the power excursions in the surviving channels are shown in Figure 4. It is found that the dynamic excursions are relatively higher if pumped at low or medium pump power. However, at higher pump power, the oscillation in the surviving-channel response are effectively suppressed and the resultant power overshoot/undershoot at the output can be kept below 1 dB. With increasing signal/channel power, the feedback ASE power necessary to compensate for channel addition/removal increases, and the gain excursion at the surviving channel decreases as well. In order to eliminate oscillation in the surviving-channel response to the channel add/drop, it is, therefore, desirable to operate the proposed all-optical narrowband ASE feedback GC-EDFA at the highest achievable pump power of 97 mW.

Although not based on the ring-lasing mechanism, the proposed GC-EDFA still experiences transient-power excursion at rising edges due to relaxation oscillation, even though its amplitude (gain excursion) is very small. This relaxation oscillation caused by the excessive gain experienced by the reflection from the three FBGs, which have 33-dB reflectivities.

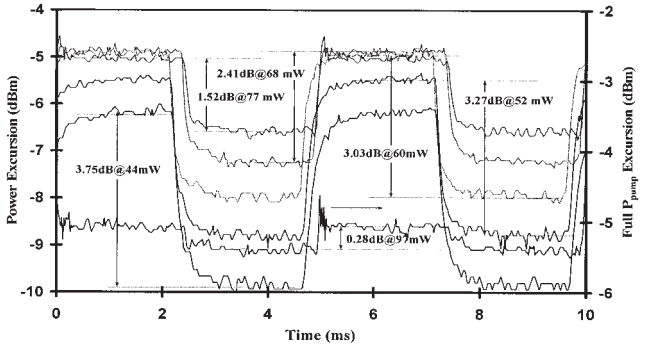

Figure 4 Gain excursion of the surviving wavelength at 1553.3 nm for different pump-power values with input power for the surviving channel of −25 dBm at 0-dB attenuation

CONCLUSION

The transient response of surviving-channel power in a narrowband ASE feedback GC-EDFA has been shown to depend upon the feedback ASE attenuation level and pump-power variation. This experiment has demonstrated that in order to minimize variation of surviving-channel power to less then 0.28 dB for channel add/drop, the ASE feedback attenuation level and pump power are critical.

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23-GHz LOW-NOISE AMPLIFIER USING PARALLEL FEEDBACK IN 0.18-μm CMOS

B. M. Frank,[1] M. M. Hossain,[1] and Y. M. M. Antar[2]
[1] Department of Electrical and Computer Engineering
Queen's University
Kingston, Canada
[2] Department of Electrical and Computer Engineering
Royal Military College of Canada
Kingston, Canada

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ABSTRACT: *A three-stage low-noise amplifier (LNA) fabricated in a standard 0.18-μm CMOS process (f_T = 45 GHz) with a maximum gain of 18 dB at 23.2 GHz and a 5.8-dB noise figure is presented. Parallel feedback between the gate and drain is used in all three stages. This configuration also provides much better linearity than other LNAs presented by resonating out the effect of C_{gd}. The amplifier has an output-referred 3rd-order intercept of 10 dBm, and a 3-dB bandwidth of approximately 1 GHz. This paper demonstrates that parallel feedback is a viable technique for the design of 20+-GHz CMOS LNAs.* © 2005 Wiley Periodicals, Inc. Microwave Opt Technol Lett 45: 309–312, 2005; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.20806

Key words: *microwave circuits; low-noise amplifiers (LNAs); CMOS; MOSFETs; MMICs*

1. INTRODUCTION

Microwave circuits in low-cost standard CMOS processes are becoming more common as device sizes scale downwards. Re-

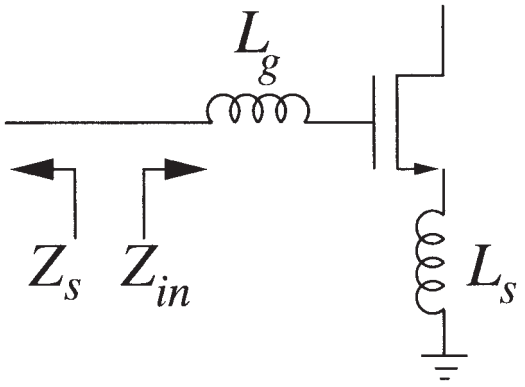

Figure 1 Inductive degeneration for low-noise amplifiers

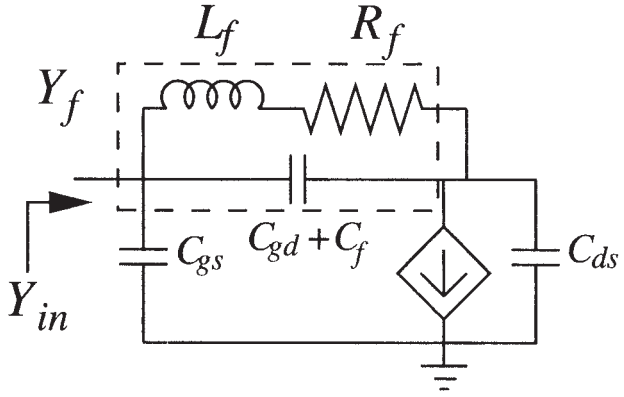

Figure 3 Inductive feedback for low-noise amplifiers

cently, two 20+-GHz low-noise amplifiers (LNAs) were presented in standard CMOS processes. In [1], a three-stage amplifier consisting of a common-gate input stage and common-source inductively degenerated second and third stages was presented. It offered a maximum gain of 22 dB at 21.8 GHz and a noise figure of 6.0 dB. In [2], a three-stage amplifier consisting exclusively of inductively degenerated common-source stages was presented. It offered a maximum gain of 12.86 dB at 23.5 GHz and a noise figure of 5.6 dB.

Parallel feedback has been used in the implementation of microwave amplifiers; the influence of parallel feedback has been studied for MESFET amplifiers [3], and the noise properties of two-port networks with feedback has been studied from a theoretical perspective [4]. Parallel feedback has also been used for a single-stage MOSFET amplifier at 20 GHz [5], but noise analysis was not considered.

This paper presents a 23-GHz CMOS LNA that uses common-source stages with parallel feedback; this topology is promising for the design of high-frequency low-noise CMOS amplifiers.

2. DESIGN AND FABRICATION

Low-noise MOSFET amplifiers are often designed using inductive degeneration, as shown in Figure 1, to provide a good simultaneous noise and power match at the device input, including LNAs operating at frequencies over 20 GHz (see, for example, [2]). The inductor L_s is used to provide a real input impedance Z_{in}, and together with the gate inductor L_g provides a power match at the input of the amplifier. It is also used to shift the optimum source impedance for minimum noise Z_{opt} close to the reference impedance of the system [6].

However, there is a problem with this technique: the gain of the amplifier is reduced due to the voltage drop across the source inductance L_s. This reduces the gate-to-source voltage v_{gs}, and lowers the gain. Since the maximum gain G_{max} of the 0.18-μm MOSFETs used for this work was quite low at frequencies exceeding 20 GHz, this reduction in gain can be problematic. In contrast, parallel gate-to-drain inductive feedback is simply used to resonate out the effect of the gate-to-drain FET capacitance C_{gd}, and does not deteriorate the gain; in fact, by resonating out C_{gd} it improves the gain at the resonant frequency. It has also been shown that appropriate parallel feedback can be used to decrease the noise figure of a transistor [7].

For this design, gate-to-drain parallel feedback, as shown in Figure 2, was used at each stage to partially resonate out the gate-to-drain parasitic capacitance C_{dg} in the transistor, and to modify the source impedance to the optimum Z_{opt} for low noise. It was also used in the first stage to shift the optimum source-reflection coefficient Γ_s. While the feedback results in a fairly small bandwidth, the use of inductive degeneration results in a similarly narrowband response. A large blocking capacitor was placed in series with the feedback inductor in order to maintain the appropriate bias conditions.

In this approach, care must be taken to ensure that the input impedance does not take on a negative real part. Using the simple small-signal model shown in Figure 3, it can be shown that the real part of the input admittance $G_{in} = \Re(Y_{in}) = \Re(1/Z_{in})$, looking into the gate of a MOSFET with inductive feedback, is approximately given by

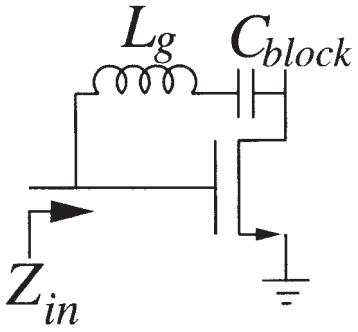

Figure 2 Inductive feedback for low-noise amplifiers

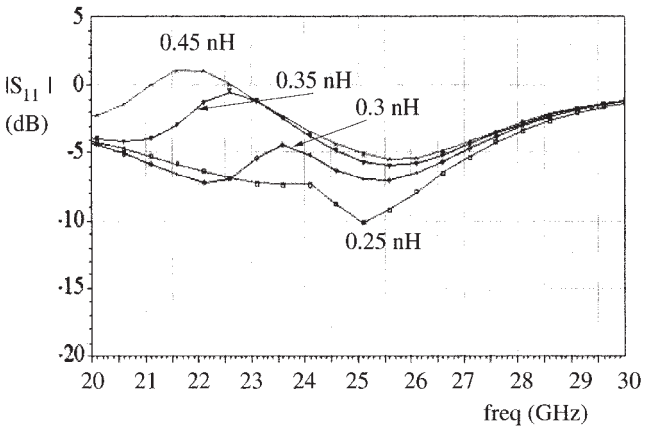

Figure 4 Simulated $|S_{11}|$ for various values of feedback inductance L_f

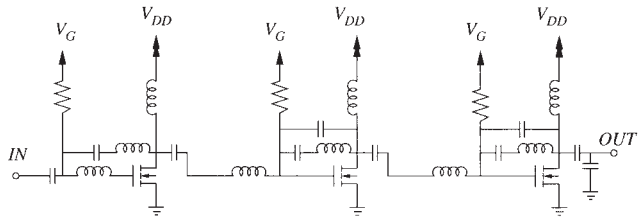

Figure 5 LNA schematic

$$Y_{in} = Y_f + \frac{g_m[1 - \omega^2 L_f(C_f + C_{gd})]}{1 - \omega^2 L_f(C_f + C_{gd} + C_{gs})}. \quad (1)$$

A negative input admittance is produced when the numerator and denominator of the second term have opposite signs. The range of ω over which the second term is negative is from $\omega = (L_f(C_f + C_{gd} + C_{ds}))^{-1/2}$ to $\omega = (L_f(C_f + C_{gd}))^{-1/2}$ (the frequency at which unilateralization occurs). To ensure stability, $\Re(Y_f)$ must be larger than the negative resistance produced by the second term. Using this condition, we require that

$$L_f \geq \frac{Q^2(C_{gd} + C_{ds})}{(1 + Q^2)^2 k^2 g_m^2}, \quad (2)$$

where $Q = (\omega L_f/R_f)$ is the Q of the feedback inductor and

$$k = \frac{1 - \omega^2 L_f C_{gd}}{1 - \omega^2 L_f(C_{gd} + C_{ds})}. \quad (3)$$

A plot of the input reflection coefficient for various L_f is shown in Figure 4. As can be seen, chosing a large feedback inductor (0.45 nH) will result in potential instability, but if inductors less than 0.3 nH are used, the input resistance will be positive over all frequencies. The stability of the entire amplifier will be examined in the next section.

The inductors were implemented as spiral inductors and simulated using ADS Momentum, and the whole circuit was designed using Agilent's ADS suite. The LNA was designed using a MOSFET model available from the foundry that is intended to be used only up to 10 GHz. It was fabricated in a standard aluminum six-metal layer 0.18-μm mixed-signal CMOS process ($f_T = 45$ GHz, $f_{MAX} = 60$ GHz) with MIM capacitors but without low-k dielectrics. The substrate resistivity is approximately 10 $\Omega \cdot$ cm. The Q of the inductors is approximately six.

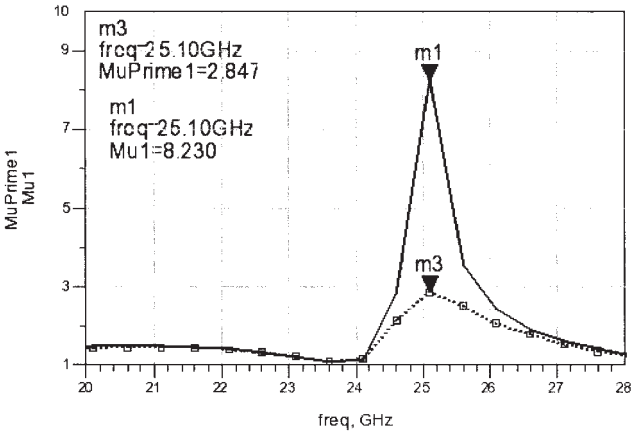

Figure 7 Simulated stability factors μ and μ'

A three-stage design, shown in Figure 5, was used to provide a gain of about 17 dB with a noise figure of approximately 5 dB. The simulated S-parameters and noise figure of the LNA are shown in Figure 6. The first stage was designed as a low-noise stage with moderate gain (approximately 4 dB), and the latter two stages are higher gain stages (approximately 6-dB each). The device was designed to operate at $V_{ds} = 1.8$ V and a total bias current of $I_{bias} = 88$ mA. The simulated output-referred 3rd-order intercept was 13.4 dB. This is quite high, relative to the previously presented amplifiers, due to the fact that C_{gd} is resonated out by the feedback inductor [7].

Figure 7 shows the simulated stability factors μ and μ' for the amplifier. As can be seen, the amplifier is unconditionally stable at all frequencies.

3. MEASUREMENTS

Figure 8 shows the measured S-parameters of the LNA. In comparison with the simulated results, there is a frequency shift of 2 GHz. Part of the reason for this is undoubtedly due to the inaccuracy resulting from using an extrapolated transistor model, and part is most likely due to the challenges in accurately modeling spiral inductors at these frequencies.

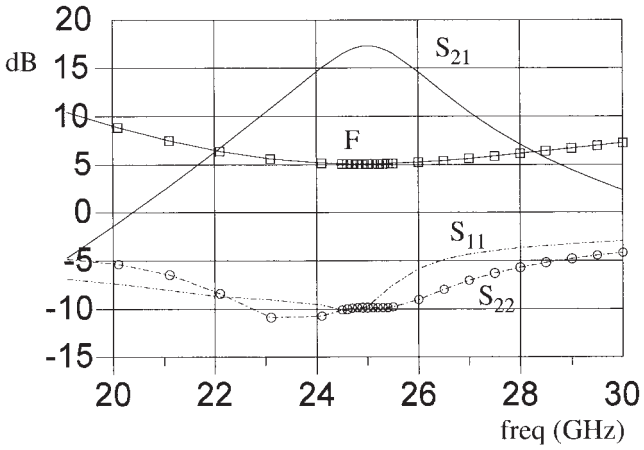

Figure 6 Simulated performance of the LNA

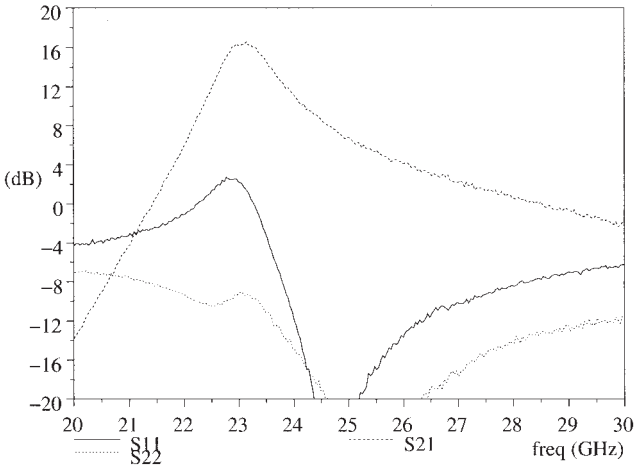

Figure 8 Measured S-parameters of the LNA

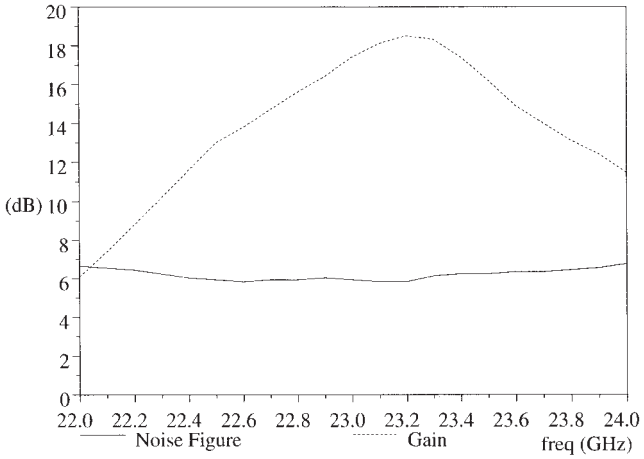

Figure 9 Measured gain and noise figures of the LNA

It may also be seen that the magnitude of $|S_{11}|$ is greater than one at the frequency of maximum gain. Post-measurement simulations indicate that this is due to a the fact that the output capacitance of the first stage was underestimated in the circuit design, resulting in a negative input admittance at 23 GHz. As discussed in section 2, the capacitance C_{ds} at the output of the MOSFET can produce a negative input resistance; hence, $|S_{11}| > 1$ at the resonant frequency of the feedback inductor and C_{ds}. The discrepancy in the value of the output capacitance of the first stage is likely partly due to the modeling of the spiral inductor, and partly due to the transistor model that is not intended for use past 10 GHz.

The gain and noise figures of the LNA are shown in Figure 9. At the highest gain frequency of 23.2 GHz, the amplifier has a gain of approximately 18 dB and a noise figure of 5.8 dB. The noise figure is similar to two other published CMOS LNA results, but due to the extrapolation of the transistor model used for this design, it is expected that better results are possible with this topology. The output-referred 3rd-order intercept was measured to be approximately 10 dBm.

4. CONCLUSION

A 23-GHz LNA in a standard CMOS process that uses inductive feedback rather than inductive source degeneration has been presented. A comparison with the only two CMOS LNAs previously presented at this frequency using this process demonstrates that this amplifier provides higher gain than that in [2], while maintaining a slightly lower noise figure than that in [1], even though both of these designs used higher f_T processes. Improvements in the input match, gain, and noise figure should be possible when higher-frequency transistor models are available for this process, thus allowing for a higher gain for a given noise figure.

ACKNOWLEDGMENTS

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A NOVEL COMPACT MINIATURIZED WIDEBAND MICROSTRIP BANDPASS FILTERS WITH DUAL-MODE RING RESONATORS

Chu-Yu Chen,[1] Cheng-Ying Hsu,[1] and Sung-Fong Lin[2]
[1] Department of Computer and Communication
SHU TE University
Kaoshsiung, Taiwan, ROC
[2] Department of Electrical Engineering
National Cheng Kung University
Tainan, Taiwan, ROC

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ABSTRACT: *This paper presents a novel, compact, low-insertion-loss, sharp-rejection, wideband microstrip bandpass filter. The filter is based on a ring resonator with direct-connected orthogonal feed lines, and uses two stepped-impedance open stubs to construct a wideband passband with two sharp stopbands. The unit cell of the ring resonators is easily cascaded and also has the feature of a compact structure. The filter is designed to reduce interference in full-duplex systems for satellite communications.* © 2005 Wiley Periodicals, Inc. Microwave Opt Technol Lett 45: 312–315, 2005; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.20807

Key words: *bandstop filter; dual mode; ring resonator; wideband bandpass filter; stepped impedance*

1. INTRODUCTION

The recent advance of RF/microwave applications has stimulated the rapid develop of new communication system such as cellular telephones, fiber-optic systems, digital satellite TV, and GPS systems. To satisfy the growing demand for devices in the RF/microwave area, the requirements for high performance, small size, lighter weight, and lower cost have become more stringent than ever.

Microwave bandpass filters can enhance the performance of RF front ends and are widely used in communication systems. Therefore, how to design a bandpass filter at low cost and with high performance is currently of great interest. Microstrip bandpass filters can be easily mounted on a dielectric substrate and can provide a more flexible design of the circuit layout. The use of miniaturized and reduced-weight dual-mode resonators in microwave bandpass filters with high selectivity has been demonstrated in modern wireless communications [1–6]. However, the passbands of these filters are narrow band, and insertion loss exists due to the coupling gap. A ring resonator using a high temperature