A 14-Gb/s 32 mW AC coupled receiver in 90-nm CMOS

Masum Hossain, Anthony Chan Carusone
Department of Electrical and Computer Engineering, University of Toronto
Email: {masum,tcc}@eecg.utoronto.ca

Abstract

This paper introduces a high-speed AC coupled receiver architecture for high density interconnects. The proposed architecture combines a novel hysteresis circuit path and a linear broadband amplifier path to recover a NRZ signal from an 80-fF capacitively coupled channel. Using this dual path technique, a 90-nm CMOS prototype achieves 14-Gb/s operation while consuming 32 mW from a 1.2-V supply. The measured sensitivity of the receiver is better than 100 mVp-p differential.

Introduction

Data rates above 1Gb/s over 50-150 fF capacitively-coupled interconnects are demonstrated in [1],[2] as a possible solution for System-In-Package (SiP) applications. In this design we propose a novel receiver architecture (Fig. 1) for a 80-fF capacitively-coupled channel. Due to the small coupling capacitances only the high frequency transitions of the transmitted NRZ data are detected at the receiver. The result is a stream of positive and negative pulses corresponding to the rising and falling edges of the Tx data as shown in Fig. 2.

The main challenge of the receiver front end is to recover NRZ data from the low swing pulses. To address this particular challenge, both clocked [3] and clock-less [4], [5], [6] approaches have been investigated. The clock-less receiver architectures implemented in [4], [5], [6] recover the NRZ data using a non-linear circuit to restore the lost low fequency signal content; the clock is then recovered using traditional clock recovery techniques from the NRZ signal. However, the speed of these circuits has been limited to 6 Gb/s.

Circuit Description

In this paper a novel front-end architecture is introduced that can operate up to 14-Gb/s for a 80-fF capacitively-coupled channel. The receiver employs a dual path architecture: the first path uses a non-linear hysteresis circuit to recover the NRZ signal from the low swing pulses. The second path uses a linear broadband amplifier to amplify the data transitions. A weighted sum of the two paths is formed to mitigate the ISI introduced by the speed limitations of the hysteresis block. Another important consideration is the sensitivity of the receiver, which is defined as the minimum input pulse signal swing required to recover NRZ signal. A lower sensitivity receiver implies a large bandwidth is required on the transmitter side to generate very sharp transitions and hence, high amplitude pulses at the receiver front-end. Thus, the receiver sensitivity has been limited to 120 mVp-p differential [5], [6]. In this design a 4 stage pre-amp was used to improve the sensitivity to 80 mVp-p and enable single ended testing.

The hysteresis circuit in [2] used a single ended CMOS latch and was limited to 1 Gb/s in a 0.35 um process. This single ended architecture suffers from common mode

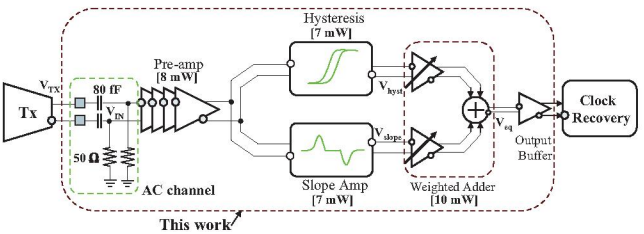

Fig. 1. Block diagram of the receiver

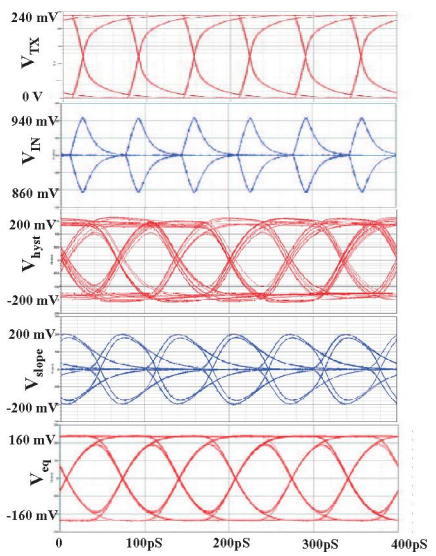

Fig. 2. Simulated eye diagrams at different nodes of the front end at 15 Gb/s

disturbances such as ground and power supply noise. A front end based on sense amplifier was used in [4] to achieve a 1 Gb/s bit-rate while consuming 5.6 mW in a 0.10-um CMOS process. The receiver descried in [5] used a single ended pre-amp and cross-coupled PMOS devices as latch to achieve 3 Gb/s in 0.18-um process and consumes 10mW power. In [6], cross coupled NMOS transistors replace PMOS devices to achieve 6-Gb/s speed. In the proposed architecture, we introduce a new hysteresis circuit, shown in Fig. 3(a). This hysteresis circuit uses an additional differential pair, g_{m3}, for positive feedback that provides several advantages: (a) The critical node V_{LATCH} has less capacitive loading since the following stage is isolated from this node by g_{m2};(b) R_{L2} and R_{L3} distribute the output capacitance to improve speed. To investigate the speed improvement of this hysteresis topology, a prototype was implemented in a 0.18-um CMOS process. The measured results proved the functionality of the hysteresis block above 10 Gb/s. There are two sources of ISI in this receiver: (a) limited bandwidth of the pre-amp and (b) limited speed limitation of the hysteresis circuit. However, the resulting degradation of the output NRZ eye quality can be

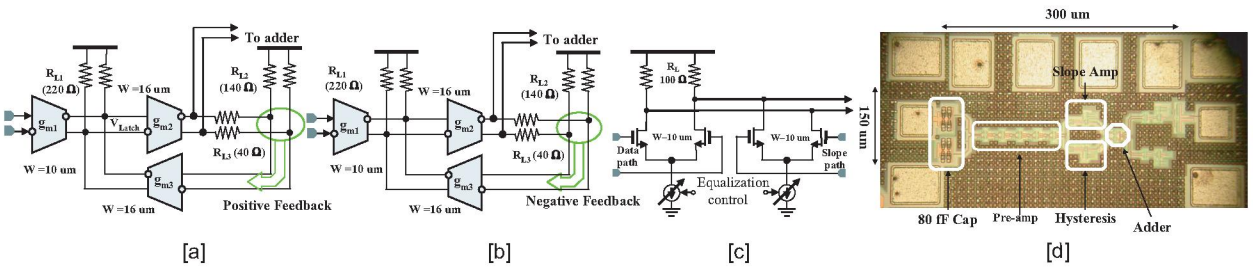

Fig. 3. Building blocks of the receiver front-end:(a) hysteresis (b) linear amplifier (c) Weighted summer. transconductors are simple NMOS diff pairs with minimum gate length (100-nm) drawn and device widths are as labeled (d) Die photo of AC receiver in 90nm CMOS

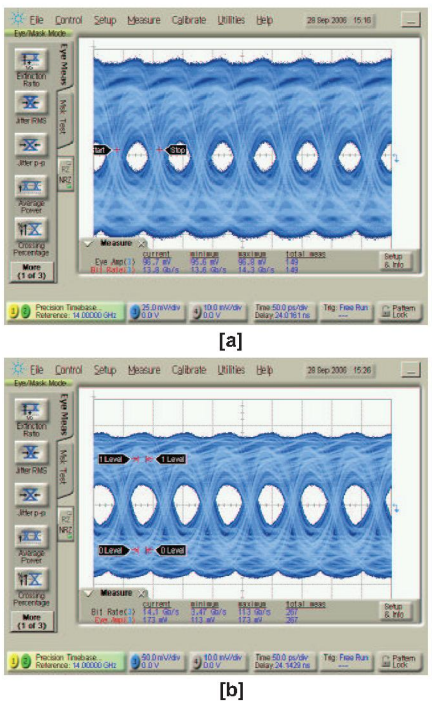

Fig. 4. Measured single ended 14 Gb/s output eye with a pattern length of $2^{31}-1$; [a] Linear path turned off (50ps/div horizontal and 25mv/div vertical); [b] Linear path activated (50ps/div horizontal and 50mv/div vertical).

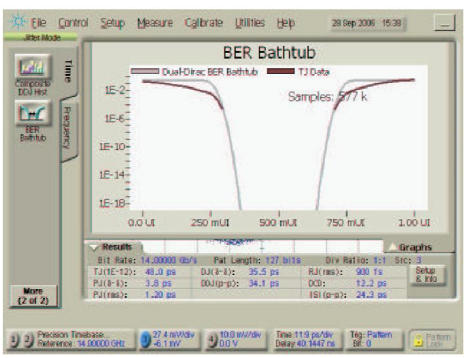

Fig. 5. BER Bathtub curve at 14 Gb/s for 2^7-1 Pattern

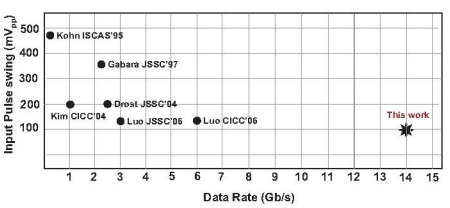

Fig. 6. Comparison of state-of-the art AC coupled receiver front-ends

compensated using the available input pulses which contain only the high frequency content of the NRZ signal.

A broadband amplifier (Fig. 3(b)) is placed in a parallel singnal path whose latency matches that of the non-linear path.The linear amplifier uses the same circuit topologyas the hysteresis circuit. By swapping the feedback nodes, feedback becomes negative improving the bandwidth to 13 GHz. Since the same architecture is used in both the linear and non-linear paths, latency through both paths are well matched at 15 Gb/s (Fig. 2).The two signal paths are added using the weighted analog summer shown in Fig. 3(c).

Measured Results

A prototype of the proposed front-end was implemented in a 90-nm CMOS process as shown in Fig. 3(d). The design was pad limited, occupying an active area of 0.045 mm^2. AC coupling was implemented using an on-chip 80-fF native metal-metal capacitance. The testing was done using a single ended PRBS generator with a swing of 240 mVp-p resulting in a pulse swing of 100 mV at the input of the front-end. Measured 14-Gb/s single ended eye diagrams and the corresponding BER bathtub cureve are shown in Fig. 4 and Fig. 5. The achieved bit rate of 14 Gb/s is the fastest published AC coupled receiver (Fig. 6). Measured results show a significant improvement in eye opening due to the additional linear path.

Acknowledgment: This work has been supported by Intel Corporation.CAD and fabrication facilities are provided by Canadian Microelectronic Corporation.

References

[1] S. Mick, J. Wilson, and P. Franzon, "4 gbps high-density ac coupled interconnection," in *IEEE Custom Integrated Circuits Conf.*, pp. 133–140, May 2002.

[2] R. J. Drost, R. D. Hopkins, R. Ho, and I. E. Sutherland , "Proximity communication," *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 1529–1535, Sep 2004.

[3] K. Kanda, D. Antono, K. Ishida, H. Kawaguchi, T. Kuroda, and T. Sakura , "1.27 gb/s/pin 3 mw/pin wireless superconnect (wsc) interface scheme," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, no. 2, pp. 186–187, Feb 2003.

[4] J. Kim, J. Choi, C. Kim, M. F. Chang, and I.Verbauwhede, "A lowpower capacitive coupled bus interface based on pulsed signaling," in *IEEE Custom Integrated Circuits Conf.*, pp. 35–38, Oct 2004.

[5] L. Luo, J. Wilson, S. Mick, J. Xu, L. Zhang, P. Franzon, "3gb/s ac-coupled chip-to-chip communication using a low-swing pulse receiver," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 522–523, Feb 2005.

[6] L. Luo, J. Wilson, S. Mick, J. Xu, L. Zhang, E. Erickson and P. Franzon , "A 36gb/s acci multi-channel bus using a fully differential pulse receive," in *IEEE Custom Integrated Circuits Conf.*, pp. 773–776, May 2006.