Performance of a Low Voltage Highly Linear 24 GHz Down Conversion Mixer in 0.18-µm CMOS

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Abstract — **A K-band low voltage, highly linear Gilbert cell mixer is presented in this paper. The goal of this work is to achieve highest possible linearity when the supply voltage is as low as 2 V. The proposed low voltage mxer topology has been experimentally verified with a down conversion mixer fabricated in a 0.18 µm CMOS process. Utilizing PMOS devices in the transconductance stage and using a 2 V supply voltage, the mixer can down convert from 24GHz to 10MHz with an input referred third order intercept of +20dBm and a conversion gain of +2dBm, thus making it a candidate for single chip receiver applications.**.

Index Terms — **Mixer, Gilbert cell mixer, K-Band, CMOS, linearity**

I. Introduction

The scaling of CMOS gate length and corresponding improvement in f_T has made CMOS process an attractive alternative to GaAs for high frequency front-end design. Though several K-band LNAs in CMOS have been reported in recent years, comparatively little research has been done on K-band CMOS mixers. A K-band CMOS mixer using single balanced Gilbert cell topology has been reported in [1] for down conversion from 24 GHz to 5 GHz, with more focus on the LNA. In [2], a 25 GHz mixer using 0.18-um CMOS was demonstrated. However, low voltage operation was not considered as a 5V supply was used. On the other hand a low voltage CMOS mixer topology has been presented recently in [3]. However, performance of this mixer for K band applications was not considered. In this work we consider both high frequency and low voltage applications without sacrificing linearity. The proposed new CMOS mixer down converts from 24 GHz to a low IF of 10 MHz and at the same time achieves a high IIP_3 of +20 dBm using 2.0 V supply. The *I-Q* mixer implementation with a single transconductance stage is shown in Fig. 1. It is important to analyze mixer performance for K-band receiver design, as the performance of the front end limits the receiver sensitivity.

In today's single chip integrated receivers both image rejection receivers and direct conversion mixers require highly linear mixers. In image reject mixers, if the IF frequency is selected to be high enough, then the image band effectively gets suppressed.

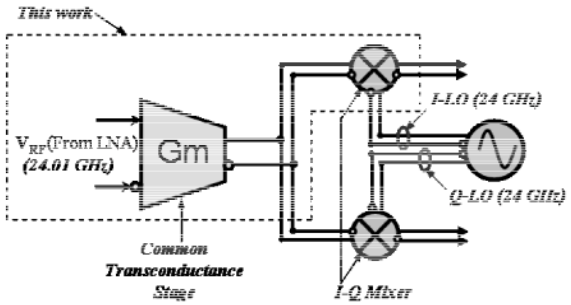

Fig.1 24 GHz low IF Down conversion receiver

However, the nearby interferer bands remain at significant levels. The suppression of these nearby bands require high selectivity IF filtering which cannot be achieved in integrated circuit technology. However, one way to reduce this selectivity requirement is to use a highly linear mixer [4]. In the case of the direct conversion receivers, distortion degrades their sensitivity as compared to the image rejection receivers. As a result, the direct conversion receiver must use a balanced mixer with greater linearity to achieve similar immunity to distortion [5]. Thus one of the goals of this work is to improve the linearity of the Gilbert cell with less emphasis on the other performance parameters such as conversion gain and noise performance.

II. K Band Low Voltage Mixer Topology

Most of the on-chip CMOS double balanced mixers used for down conversion are based on the traditional bipolar cross coupled differential modulator stage introduced by Barry Gilbert in his original paper in 1968 [6], as shown in Fig. 2. In recent years several topologies have been investigated by researchers to accommodate reducing supply voltage and to reduce the tradeoff issues at the same time. The PMOS Folded mixer shown in Fig. 3 can address several limitations that arise from using a low supply voltage. By avoiding transistor stacking, extra headroom is available and this improves the conversion gain as well as the linearity.

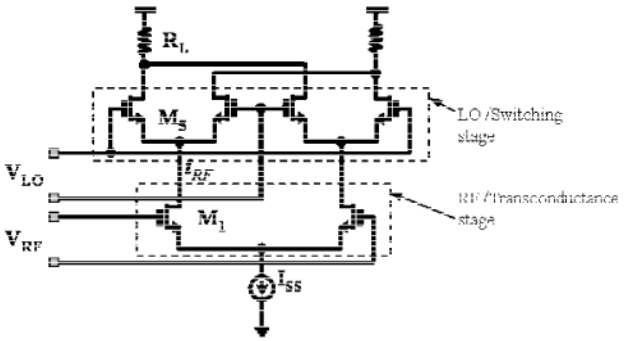

Fig.2 Standard Gilbert Cell Mixer

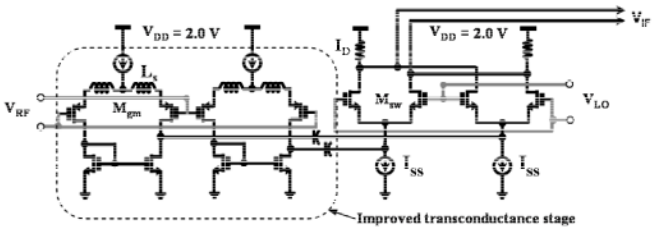

Fig.3 A PMOS Folded Mixer

The use of a PMOS device can be justified considering the limitation of the linearity performance of the topology.We will first consider the linearity of the proposed mixer. The available headroom in most cases is limited by V_{DD} and for low voltage design transistor stacking further reduces the maximum output voltage swing. The available voltage headroom is related to the bias conditions and choice of load resistance (R_L). Although inductive loading can be used to increase available headroom, it has minimal effect for an IF as low as 10 MHz. Similarly using a MOS device as an active load also degrades the noise performance.

CMOS switches can also produce distortion in both low and high frequency. The analysis of high frequency distortion has been reported in [7]. According to [7], intermodulation distortion (IM_3), has strong bias dependence which can influence the over all IIP_3. Although both the transconductance stage and the switching stage contribute nonlinearity and hence limit the IIP_3, for scaled devices at high frequency and low voltage applications, it is the switching stage distortion that primarily sets the IIP_3. For submicron CMOS the IIP_3 can be approximately expressed as follows, assuming enough headroom is available in the IF stage:

$$IIP_3 \approx 10\left[1+\log\left(128\sqrt{2}/3\right)-\log(\theta)-\log\left(g_m/I\right)\right] \quad (1)$$

Here θ is vertical mobility degradation factor to take in to account the mobility degradation

$$\mu_{eff} = \mu/(1+\theta(V_{GS}-V_T)) \quad (2)$$

Considering a 12X2.5 µm CMOS transistor that has a drain current of approximately 0.15mA /µm, the upper limit of IIP3 due to the transconductance stage can be estimated to be +25 dBm from (1). However the low IIP_3 of a K-band Gilbert cell mixer [8] indicates that the distortion of the switching stage severely limits the IIP_3 of the mixer.

The conversion gain (A_{CG}) of the proposed CMOS K-band mixer in Fig. 3 is relatively low because of the small transconductance in the RF stage at high frequencies due the use of PMOS devices. The mixer conversion gain can be approximated usng an approach described in [9] that incorporates transition delay caused by the sinusoidal LO drive.

$$A_{CG} \approx \frac{2\sqrt{2}g_{mPMOS}R_{eq}V_{LO}}{(V_{GS}-V_T)_{switch}\pi}\sin\left(\frac{\sqrt{2}(V_{GS}-V_T)_{switch}}{V_{LO}}\right) \quad (3)$$

$$R_{eq} = r_0 \parallel R_L = \frac{\lambda R_L}{\lambda + R_L I_{ss}/2} \quad (4)$$

Where λ is the body factor, and $(V_{GS}-V_T)_{switch}$ is the over-drive voltage of the switch.

III MIXER DESIGN

The optimization technique for Gilbert cell mixer which has been presented in [9] is applicable for low frequency applications. However, in a K-band mixer, design of the switching core is critical as the transistors are operating close to f_T. The switching sage was designed to minimize the swithching delay. The optimum condition for the switching stage was found to be a minimum gate length transistor with 0.15 mA/um current densities for minimum switching delay in the 0.18 µm process. Determining the size of transconductance stage devices is fairly simple; with the device biased at peak f_T current density [10], the device size is determined by the allowable power consumption. Using expressions (1) and (3), the required conversion gain and IIP_3 can be selected for a particular application and by optimizing the switching quad it is possible to achieve both conversion gain and linearity performance close to the specification. The source degeneration inductors of 300 pH are added in the transconductance stage to achieve higher linearity at the cost of conversion gain.

III. Experimental Results

To experimentally verify the presented mixer topology and optimization technique a K Band down conversion mixer has been designed to down convert an RF signal to the band from 10MHz – 1.5 GHz. The fabricated die photo is shown in Fig. 4.

Since linearity is the primary concern of the design, and to limit the power consumption, comparatively smaller transistors (10 X 2.5 um) were chosen in the RF stage resulting in a transconductance of approximately 10 mS.

The expressions given in (1) and (3) predict an approximate conversion power gain better than +2 dBm and linearity better than +25 dBm. To reduce the even order distortion a CPW-CPS transition has also been used in this design. Since in a CPS line most of the electric fields of the even order modes are coupled to the ground through lossy substrate, the even order mode will experience more attenuation compared to that in a differential CPW line.

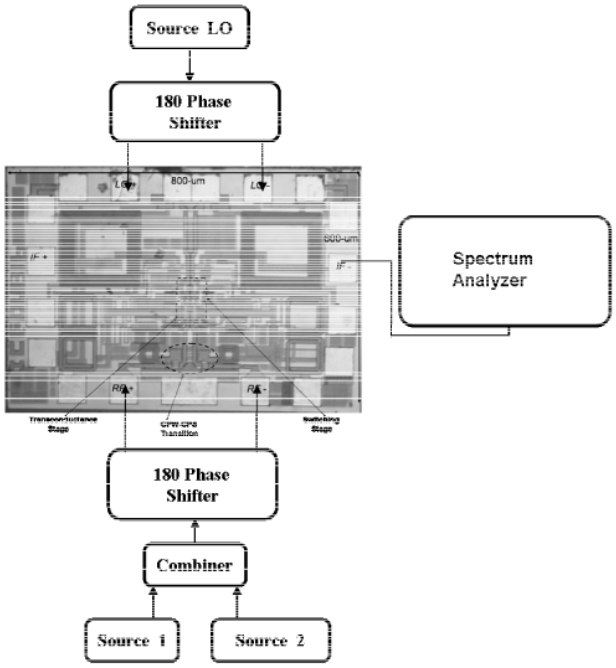

Fig.4 Experimental setup for the two tone test

Although a gate width of 4 X 2.5 um was found to be the optimum size for devices in the switching stage, a width of 12X2.5 µm was used to provide a good match to the LO input at around 24 GHz and to reduce the loading effect of the transistor M_{load}, When integrated with an on-chip VCO, a 4 X 2.5 µm size is recommended as the optimum size.The output buffer and the transmission line matching were used for the measurements and they were later on carefully de-embedded to evaluate the actual mixer performance.The measurements were done by measuring a single ended IF due to measurements constraints so the second order intermodulation intercept IM_2 could not be measured.

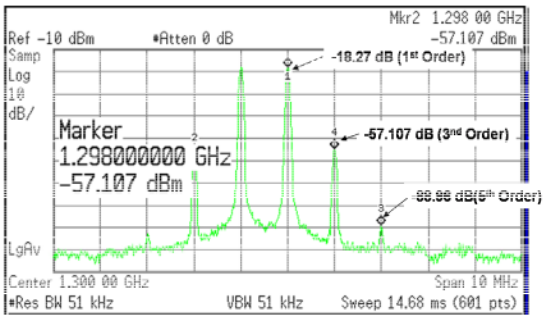

Fig.5 Measured IF Spectrum of two tone test with f_{RF1}=24.3 GHz, f_{RF2}=24.99 GHz f_{LO}=24.29 Ghz P_{LO}=0 dB

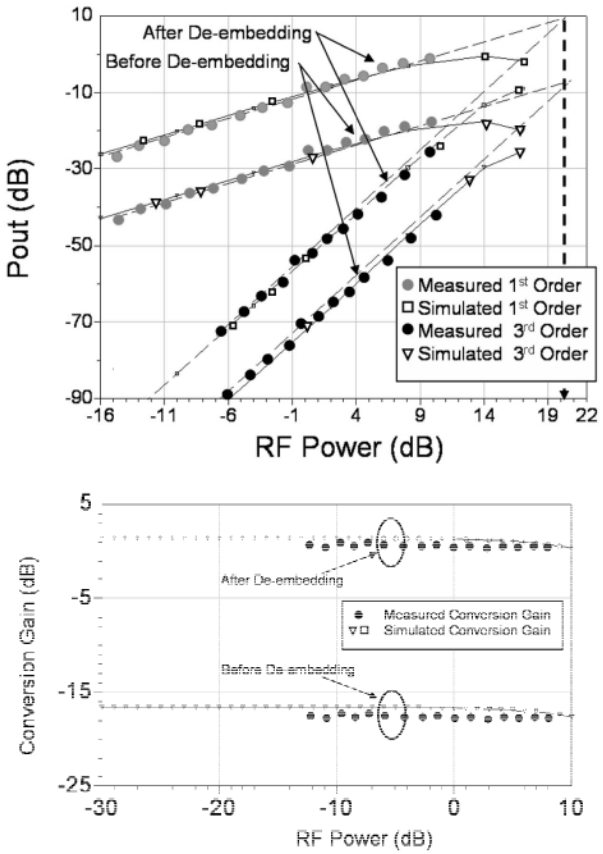

Fig.6 Measured and Simulated (a) conversion gain and (b) *IIP_3*.

Fig. 4 shows the measurement setup. The results of the two tone test when the mixer down converts the signal

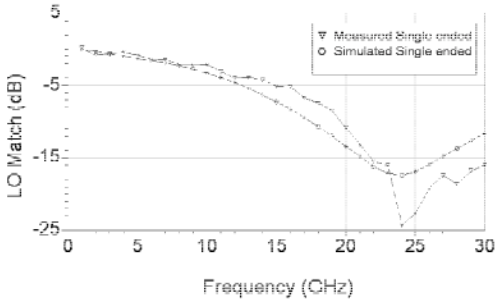

Fig.7 Measured and simulated LO matching

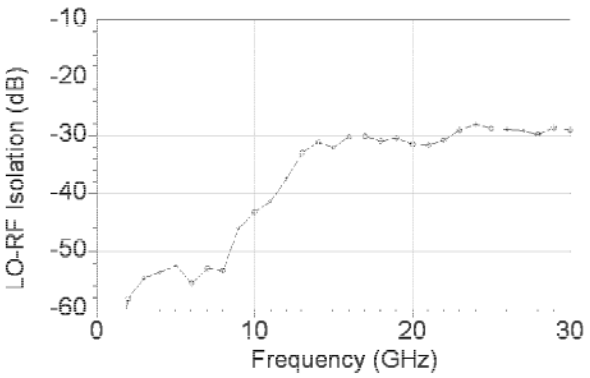

Fig.8 Measured LO-RF Isolation

from 24 GHz to 1.3 GHz are shown in Fig. 5. In simulation the mixer achieved an IM_2 of -73dBm. Measurement results show good consistency with simulated performance. The combination of conversion gain >2 dB, and linearity of +20dB indicates that by optimizing the switching speed, the IIP_3 limit of the transconductance stage can be approached (Fig. 6). Good agreement between measured and simulated LO matching was observed in Fig .7. The measured LO-RF isolation was found to be better than -28 dBm. The RF and IF matching was not measured due to the difficulty in achieving an accurate differential on-chip calibration.

VI. Conclusion

A high frequency mixer has been presented in this paper. The proposed topology utilizes folded architecture to enable low voltage operation. This is the first experimental demonstration of PMOS device for K-band application. Thus PMOS devices can be used even at K-band frequencies to reduce *1/f* noise. The achieved input-referred third order intercept of 20 dBm is the highest reported using this technology and a 2.0 V supply voltage. This high linearity is achieved using PMOS devices and the folded mixer topology. By increasing the DC power consumption, it is possible to achieve higher conversion gain.

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