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Name of Author: Norman J. Buchanan

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Norman J. Buchanan
#104 Centre for Subatomic Research
University of Alberta,
Edmonton, Alberta
Canada, T6G-2N5

Date: _____

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THE RADIATION QUALIFICATION OF A SWITCH CAPACITOR ARRAY CONTROLLER FOR USE IN ATLAS

by

Norman J. Buchanan

A thesis submitted to the Faculty of Graduate Studies and Research in partial fulfillment of the requirements for the degree of **Doctor of Philosophy**.

Department of Physics

Edmonton, Alberta
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University of Alberta

Faculty of Graduate Studies and Research

The undersigned certify that they have read, and recommend to the Faculty of Graduate Studies and Research for acceptance, a thesis entitled **The Radiation Qualification of a Switch Capacitor Array Controller for use in ATLAS** submitted by Norman J. Buchanan in partial fulfillment of the requirements for the degree of **Doctor of Philosophy**.

Dr. D. Gingrich (Supervisor)

Dr. X. Sun

Dr. J. Beamish

Dr. M. Vincter

Dr. A. Meldrum

Dr. D. Hanna (External examiner)

Date: _____

To my father, Norman Buchanan Sr.

Abstract

A switch capacitor array controller for use in the ATLAS detector was radiation qualified. Five prototypes of the controller were examined: Xilinx XC4036XLA and XC2S150 field programmable gate arrays, an Altera EPF10K50 complex programmable logic device, a radiation-hardened DMILL and a deep sub-micron application-specific integrated circuit. All of the devices, except for the XC4036XLA device, were irradiated with x-rays to test for total ionizing dose effects. The XC2S150 and EPF10K50 devices showed increases in power supply current at average total ionizing doses of (331 $\pm$ 29) Gy(SiO_2) and (832 $\pm$ 90) Gy(SiO_2), respectively. The application specific integrated circuit devices showed no increases in power supply current when irradiated to doses anticipated during ATLAS operation.

The XC4036XLA had a single-event upset saturation cross-section value of $(1.3 \pm 0.2)\times10^{-10}$ cm^2/device for the user defined circuit and $(26 \pm 1)\times10^{-10}$ cm^2/device for the configuration switches. The device exhibited a threshold energy of (22 $\pm$ 1) MeV for proton-induced single-event upsets. It was estimated that if the XC4036XLA was used in ATLAS, one of the devices in the electro-magnetic barrel calorimeter would require a reconfiguration every 12 minutes on average. The DSM device had a single-event upset saturation cross-section of $(5 \pm 1)\times10^{-13}$ cm^2/device and a single-event upset threshold energy of (44 $\pm$ 24) MeV for upsets that could not be corrected. It was estimated that one uncorrectable upset would occur, on average, every 65 device·days of operation

in ATLAS. One single-event latch-up was observed when the XC40346XLA was irradiated with 105 MeV protons. It was estimated, at the 95% confidence level, that the mean time between proton-induced latch-ups for the XC4036XLA in ATLAS would be between 388 device·yr and 7.87×10^5 device·yr. No permanent single-event effects were observed in the application specific integrated circuits.

Acknowledgements

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Chapter 1

Introduction

The radiation levels within the ATLAS detector and specifically the liquid argon calorimeter will be sufficiently high that embedded electronics will be susceptible to transient errors and permanent damage. The radiation qualification of the digital switch capacitor array controller to be located within the ATLAS detector is described.

The controller design was implemented in five different technologies. Two Xilinx field programmable gate arrays (FPGAs)*, an XC4036XLA and an XC2S150, were used as prototype controllers, as was an Altera EPF10K50 complex programmable logic device (CPLD). In addition, two radiation-hardened application specific integrated circuits (ASICs) were used as prototypes: a DMILL (Durci Mixte Isolant Logico Lineaire) ASIC utilizing radiation hardening techniques and a deep sub-micron (DSM) ASIC utilizing radiation hardening techniques and mitigation techniques. The ASICs are more radiation tolerant than commercially available devices but have more risks associated with their production. Thus both types of devices were studied.

The chosen prototype was expected to survive radiation levels similar to those expected in ATLAS without suffering effects related to the associated radiation levels. Each device was tested for the permanent effects associated with total ionizing dose (TID) and for single-event effects (SEEs), both transient and permanent. Figure 1.1 summarizes the types of tests performed on each prototype, along with the radiation used for the tests. Total ionizing dose tests were performed on the EPF10K50, XC2S150, DMILL, and DSM prototypes using an x-ray generator. A ^{60}Co facility was used for some of the TID tests of the EPF10K50 device. Proton irradiations were performed on the DSM device and the

*A glossary of acronyms used can be found in Appendix A.

total ionizing dose for these tests contributed significantly to the total amount of TID absorbed for the device. Proton irradiations were used to test the XC4036XLA, DMILL, and DSM prototype controllers for SEEs. The DSM devices were irradiated with neutrons to ensure that no displacement effects would degrade the operation of the device.

In addition to the description of the tests performed, this thesis gives some background to the ATLAS project, specifically the switch capacitor array controller that will be used in the liquid argon calorimeter readout electronics. An overview of radiation effects on microelectronic systems is also given. Discussion pertaining to how the results impacted the decision of which prototype controller was ultimately chosen for use in the ATLAS detector is presented.

1.1 Personal Contributions

My personal contributions to the work presented in this thesis, and toward my PhD, are now given. I was present for all of the proton irradiations and all of the x-ray irradiations. I had a significant role in the planning, organizing and performing of all the tests. I modified the data acquisition and communication code used for the XC4036XLA, EPF10K50E, and deep sub-micron tests. I wrote the data acquisition and monitor code used for the tests of the XC2S150 and DMILL prototypes. I consulted in the design of the test systems with the technicians and other researchers involved in the project. I performed all of the analysis presented within this thesis.

In addition to the work presented in the thesis, during the past 4 years I contributed significantly to the early commissioning of the x-ray facility, which included: the installation of the x-ray generator; ensuring that the facility adhered to the strict federal and provincial radiation safety regulations; and initial testing of the x-ray generator. I also carried out the calibration of the ion chamber used since June 2002 for x-ray dosimetry. I performed Fricke dosimetry for the ^{60}Co irradiations. I assisted with some of the thermal tests performed on the DSM device. I also spent time studying possible alternate approaches to the modeling of single-event upsets. In addition, I gained experience with the `egs` simulation package [1] and had begun using the package to study the effects of dose enhancement on micro-electronic devices.

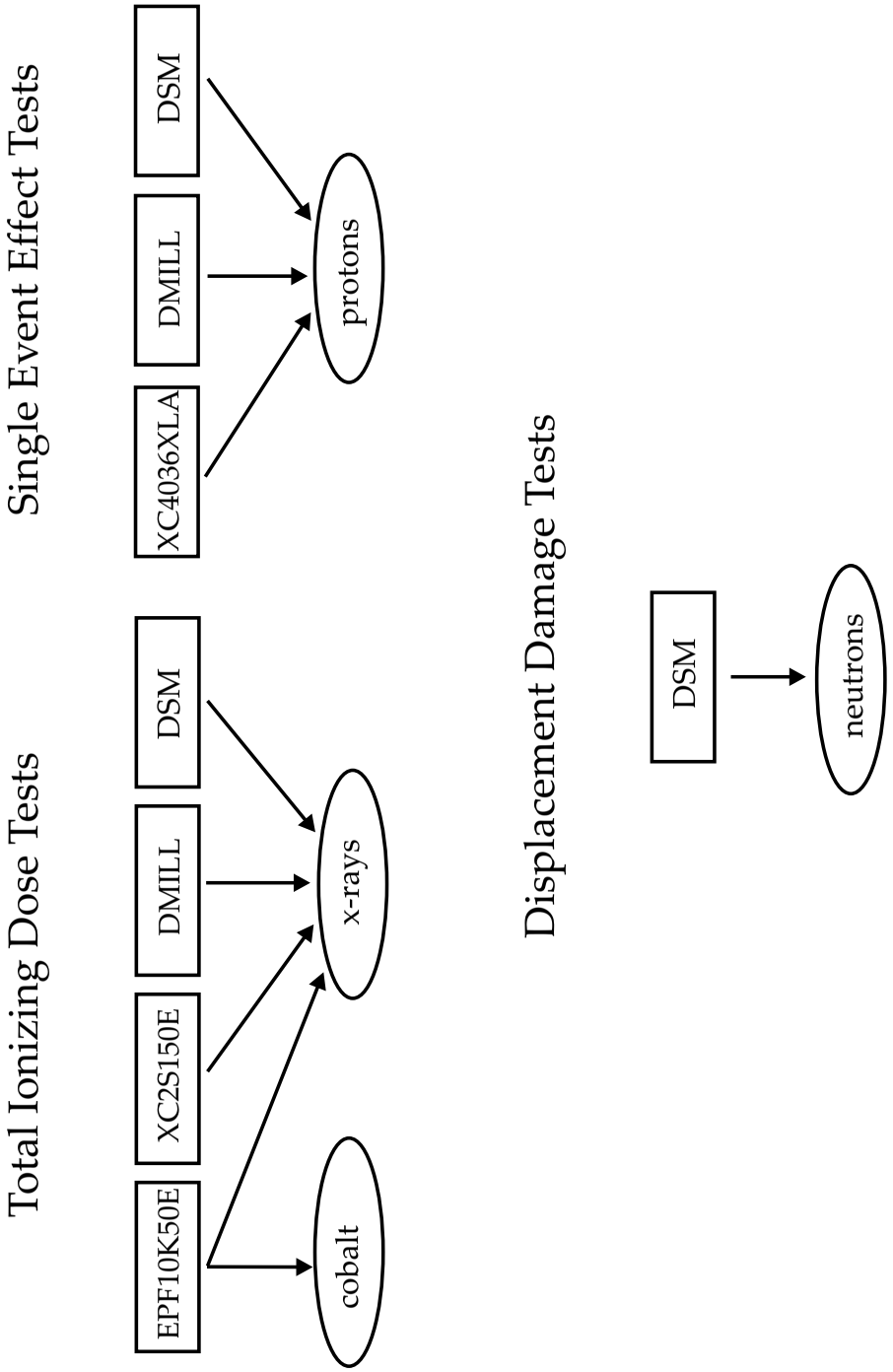


Figure 1.1: Diagram summarizing the test results and termination points of prototype testing.

Chapter 2

Physics Motivation and Experimental Background

2.1 Introduction

Over the past century, subatomic physics experiments have, in general, become increasingly large and complex. Each experiment is designed to probe a particular energy range and once the physics in that region has been sufficiently studied, focus moves on to the next regime. Studying physics in higher energy regimes demands that the particles under study be accelerated to increasingly higher energies. A description of the machines that accelerate particles for such experiments is extensive and can be found elsewhere (Refs. [2], and [3] for example.). The latest particle accelerator under development is the Large Hadron Collider (LHC), at CERN in Geneva. The primary goal of the LHC is to discover the last outstanding piece of the Standard Model of particle physics, the Higgs boson, which is theorized to provide mass to other particles [4, 5]. Existing accelerators have failed to discover the Higgs boson and the LHC was designed to allow higher energies to be probed. It will collide protons at the highest energies ever produced, and at an extremely high rate. The combination of using protons as the primary particles, accelerating them to high energies, and having the collisions occur at a high rate, will lead to high levels of radiation in the detectors. Such radiation levels will be potentially hazardous to the materials that make up the detectors. This is particularly a concern for electronic components used in the detector.

2.2 Large Hadron Collider

In the year 2007 the LHC will go online producing high luminosity* (10^{33} $cm^{-2}s^{-1}$ to 10^{34} $cm^{-2}s^{-1}$) proton on proton collisions with a centre of mass energy of 14 TeV. The collider will initially operate at a lower luminosity of 10^{33} $cm^{-2}s^{-1}$ providing an opportunity to study processes that depend upon precise measurements of particle properties near to the beam, such decays of short lived τ-leptons or bottom-quarks (b-quarks) [7]. Such precise measurements are more easily made with a reduction of the remnants of earlier interactions (or "pile-up") that would be associated with a higher luminosity. There is also concern that running at the projected maximum luminosity of 10^{34} $cm^{-2}s^{-1}$ for too long could damage the parts of the detectors that are closest to the beam (a description of a particle detector that will operate at the LHC is given in Section 2.3). The LHC will then be run at the higher luminosity providing the opportunity to make measurements which require a greater number of events and do not depend as much on precision measurements near the beam. The discovery of the Higgs boson, for example, would require high luminosity as the interactions which produce the Higgs will be relatively rare compared to the τ-leptons and b-quarks mentioned above.

The LHC will use the existing Large Electron-Positron (LEP) accelerator tunnel, which has a circumference of 27 km, making it the largest hadron collider ever constructed. The LHC will contain four detectors (Figure 2.1). Two beams of protons in side-by-side rings will be accelerated to 7 TeV in opposite directions and will collide at the four interaction regions. To reach the maximum luminosity of 10^{34} $cm^{-2}s^{-1}$, each of the rings will be filled with 2835 bunches, or groupings, of 10^{11} protons [8]. The injection system used for the LHC will be an upgraded version of the currently existing Super-Proton-Synchrotron (SPS). Protons will be accelerated to 1.4 GeV, for injection into the LHC [9].

The bunch crossing period will be 25 ns, corresponding to a frequency of 40 MHz and giving a bunch separation of 7.5 m. The resulting beam current will be 0.54 A. It is expected that there will be 10-20 collisions per bunch crossing.

A magnetic field of 8.36 T will be required to direct the 7 TeV proton beams around

*Luminosity is a measure of the number of particles passing an interaction region per second. In a collider where there are N particles per bunch, the bunch interaction has a cross-sectional area A, and f is the frequency of bunches passing the interaction region, the luminosity is given as $L = N^2 f/A$ and has the units of $s^{-1}cm^{-2}$ [6].

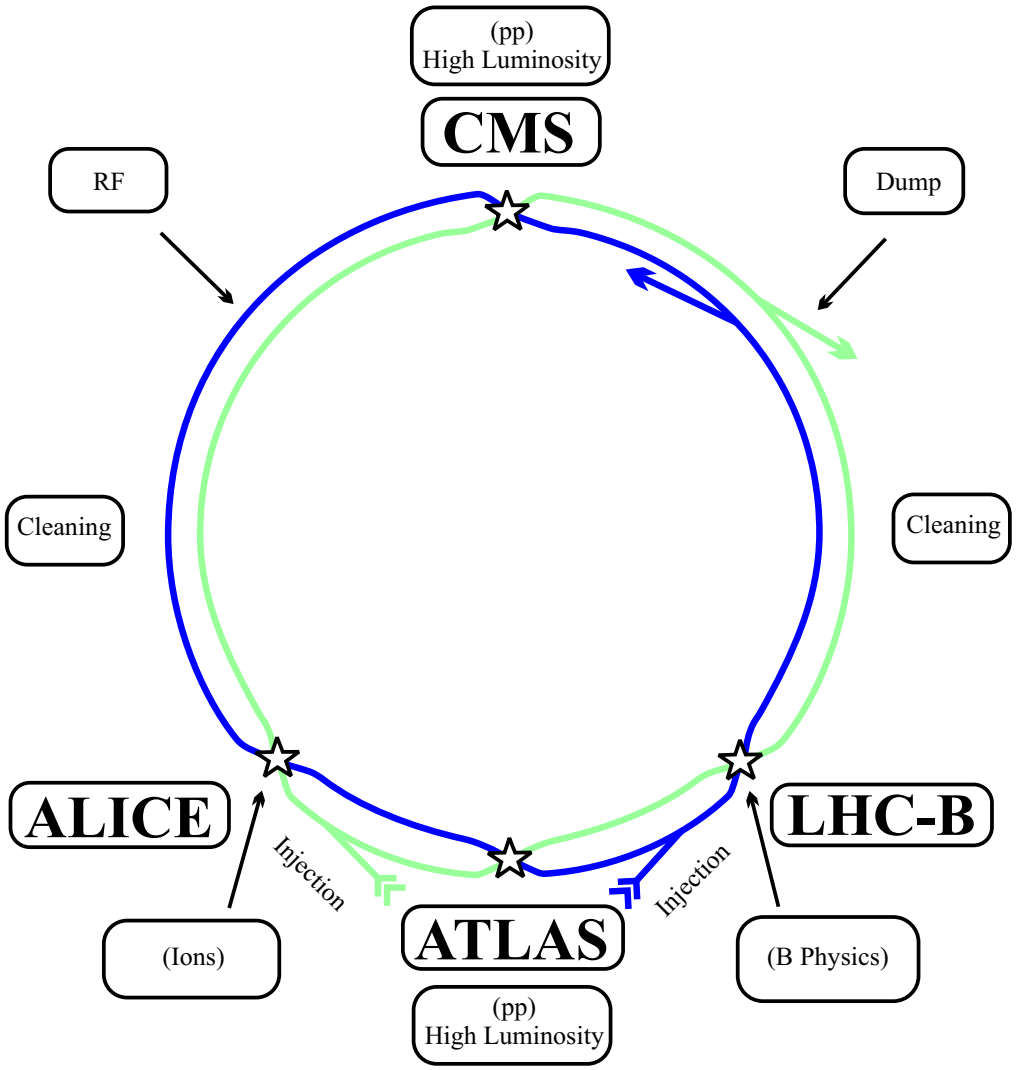


Figure 2.1: Layout of Large Hadron Collider and associated detectors. Based on figure in Ref [7].

the ring. To achieve this high magnetic field super-conducting magnets will be utilized.

2.3 A Toroidal LHC Apparatus (ATLAS)

The ATLAS detector (Figure 2.2) is a multi-purpose detector that will provide measurements allowing data to be accurately reconstructed. ATLAS will be required to provide the following [7]: very good electro-magnetic energy measurement, or calorimetry, permitting the detection of photons and electrons; the simultaneous measurement of the particle paths corresponding to charged particles, with good efficiency for lepton identification and tracking, as well as the measurement of particles produced close to the beam; and precise muon momentum measurements. To achieve the measurement objectives described above, there will be three sub-detector systems: an inner detector containing a transition radiation tracker, and semiconductor detectors; a calorimeter system made up of electro-magnetic and hadronic components; and a muon spectrometer.

The inner detector will be used to obtain tracking information on charged particles coming from the interaction region. The calorimeter will measure the energy deposited, from electro-magnetic and hadronic showers, of particles traversing it. The muon detector will provide tracking information of muons coming from the decays of secondary particles.

2.4 ATLAS Trigger

An important element of the ATLAS detector is the trigger. A trigger is a device that uses a subset of the event[†] information to determine whether to use more resources to further study and store the event. A trigger usually uses a small separate sub-detector or a portion of the total detector to make this decision. This minimizes the resources required and keeps the trigger decision time (latency) to a minimum. An example of a trigger could be a pair of thin scintillating paddles situated in the beam line several meters in front of a fixed target experiment. The trigger decision might require a coincidence between the

[†]An event in this context is a set of data collected within the detector that corresponds to a particular particle interaction.

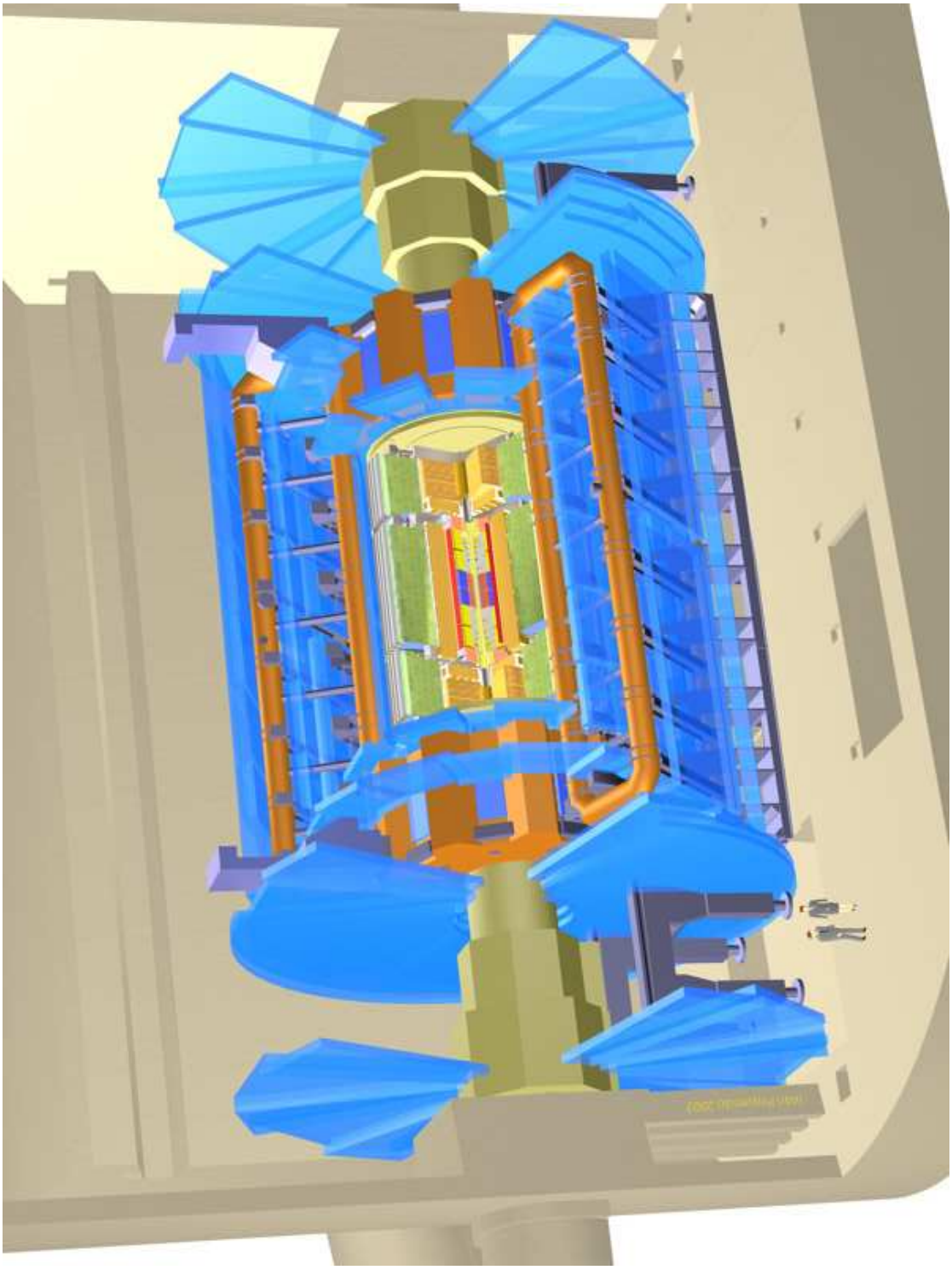


Figure 2.2: The ATLAS detector shown as it will be installed in the cavern [10].

tiles within a fixed time. Readout would then be initiated and the event would be stored for further consideration. Typically, the trigger will reduce the amount of information stored for off-line analysis by reducing the number of events recorded.

The trigger for ATLAS will be a three level system, as shown in Figure 2.3. The level-1 (LVL1) trigger will use a subset of the calorimeter and muon detector, but not the inner detector where the number of particle tracks will be too high to provide useful information for initial trigger decisions. The LVL1 will be used to locate regions of the detector containing potentially interesting features, such as electro-magnetic clusters with high transverse momentum [7]. It will process data that comes from segments of the detector, which are groupings of smaller segments (i.e. coarse granularity). The LVL1 trigger will accept data at the LHC bunch-crossing rate of 40 MHz and have a trigger latency of 2.5 μs. This is the time taken to form the decision using data from the sub-detectors, as well as signal transmission time [11]. The calorimeter data is held in analog memories during this period. The output of the LVL1 trigger has a maximum mean rate of 100 kHz. The event acceptance rate of the level-2 (LVL2) trigger is between 0.1 kHz and 1 kHz with a variable latency of 1 ms to 10 ms. All detector subsystems, including the inner detector, will be used in the LVL2 trigger decisions (using finer granularity data), which is also made on tracking and transverse momentum measurements. Events selected by the LVL2 trigger will be sent through an event builder to a farm of processors. These processors make up the level-three (LVL3) trigger which reconstructs events at a rate of 10 Hz to 100 Hz. The LVL3 trigger will use more complicated reconstruction algorithms, similar to those used off-line, to make selection decisions. After events are selected by the LVL3 trigger, they will be recorded for further detailed analysis.

2.5 Liquid Argon Calorimeter Electronics

The calorimeter in ATLAS (Figure 2.4) is composed of two technologies: a calorimeter composed of high density scintillating blocks, or tiles, designed primarily to measure the energy deposited by hadronic showers propagating radially outward from the beam, and a sampling calorimeter, utilizing a liquid argon technique, which will measure both hadronic and electro-magnetic energy deposition. The electronics described in this thesis

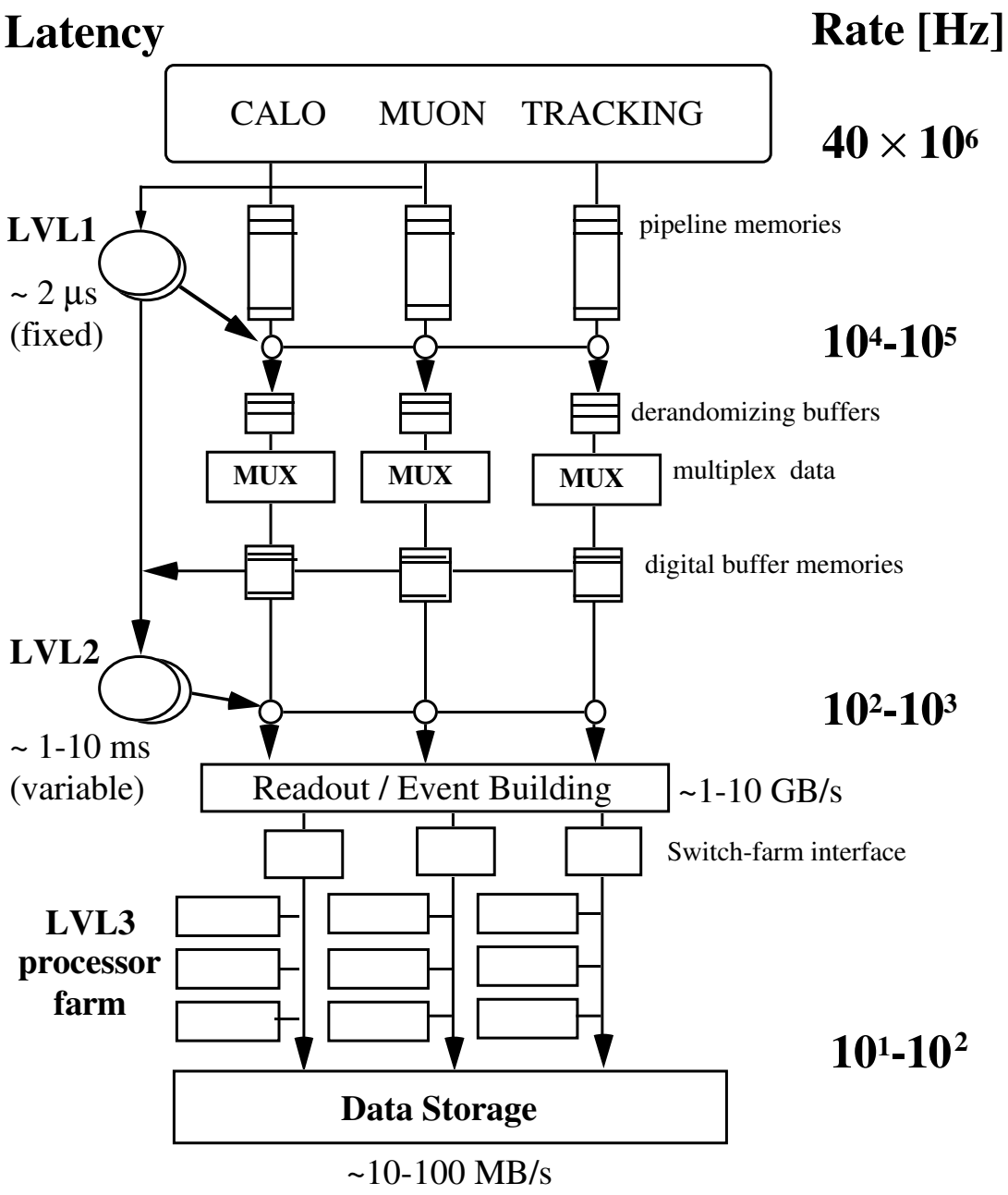


Figure 2.3: ATLAS trigger architecture (taken from Ref. [7]).

pertain exclusively to the liquid argon (LAr) sampling calorimeter. The LAr calorimeter is composed of a lead-LAr electro-magnetic barrel calorimeter that sits just outside of the solenoid for the inner detector (Figure 2.4), as well as electro-magnetic lead-LAr and tungsten/copper-LAr hadronic endcap calorimeters that sit at the ends of the detector. Forward calorimeters sit inside of the hadronic endcap calorimeters, closer to the beam. The LAr calorimeter of ATLAS requires the careful time synchronization of approximately 190,000 high speed, large dynamic range readout channels. There will be 110,208 channels for the electro-magnetic barrel, 63,744 for the electro-magnetic endcap, 4,416 for the hadronic endcap, and 11,288 for the forward calorimeter, for 189,656 total readout channels. The energy deposited in a particular calorimeter cell can be as high as 3 TeV [13]. At an energies just above pile-up and electronic noise, which is estimated to be 50 MeV [13], measurements of the signal energy need to be made. Since 3 TeV divided by 50 MeV is 60,000, a dynamic range of at least 16 bit (65,536) is required to cover the range.

The readout electronics for the LAr calorimeters can be grouped into two main categories: on-detector and off-detector, which can be seen in Figure 2.5. The off-detector calorimeter electronics consists of the trigger electronics, as well as electronics for processing and storing the data after it has been selected by the trigger and digitized. Processing of the data coming from the front-end readout board (FEB) is performed by electronics and the readout driver (ROD) modules. The on-detector electronics consists of the front-end boards, the tower builder (a circuit for summing the data in calorimeter towers[‡]), and calibration electronics.

2.5.1 The Front-End Board

The chain of electronics used for reading out the signals from the electrodes inside the calorimeter will now be described. The front-end electronics system will amplify, shape, store, and digitize the signals. A photograph of the FEB is shown in Figure 2.6 and a block diagram of the analog part of the readout electronics is shown in Figure 2.7. The analog signals from the detector are amplified early in the readout chain prior to the introduction of noise and passed to the tri-gain shapers which split and amplify the detector signals.

[‡]A calorimeter tower is a group of calorimeter cells segmented in solid angle and extending radially through the depth of the calorimeter.

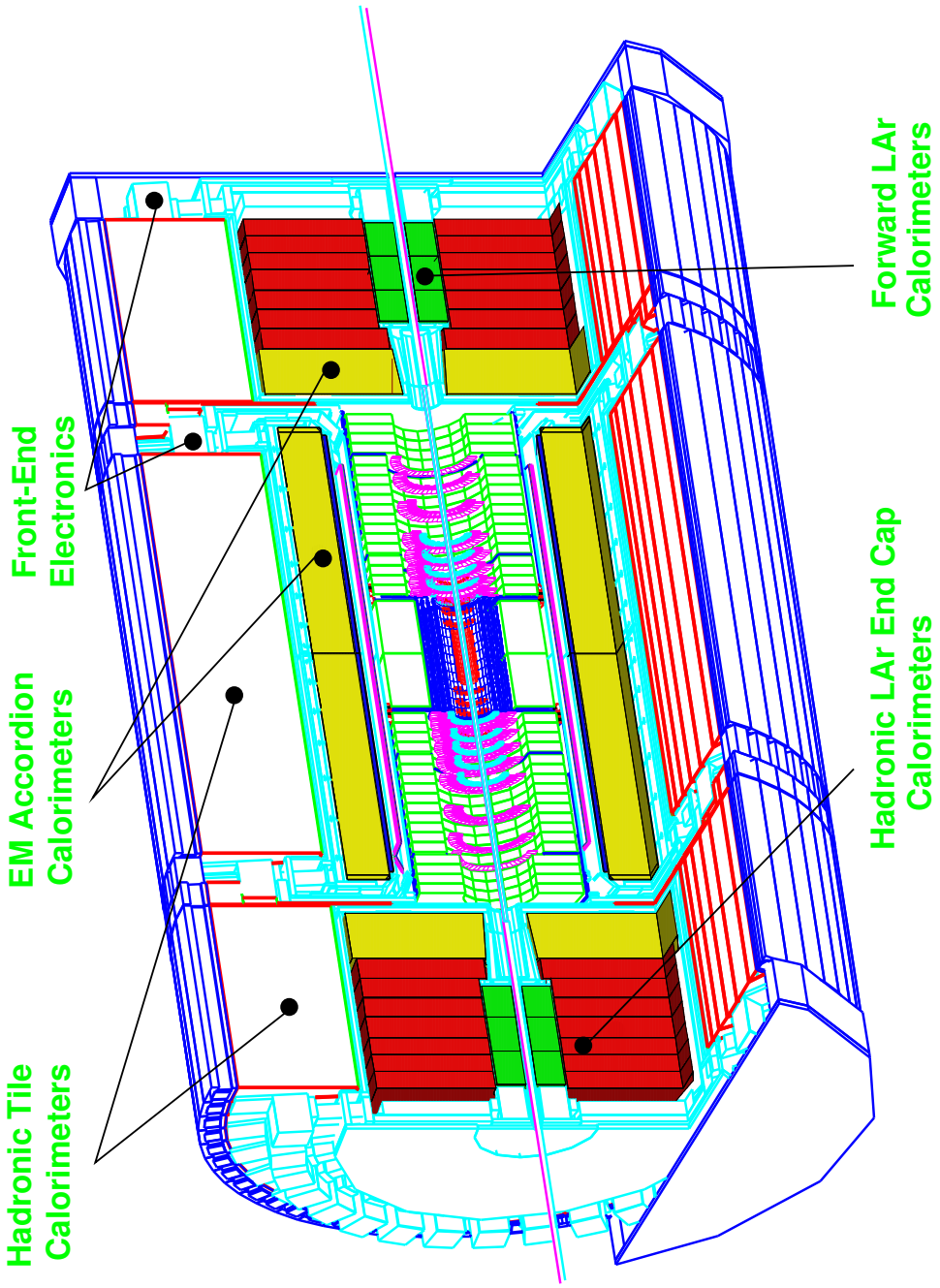


Figure 2.4: The ATLAS calorimeter showing the liquid argon and tile components (the calorimeter is approximately 8 m in diameter). The space where the electronics will reside is labeled. Figure from Ref. [12]

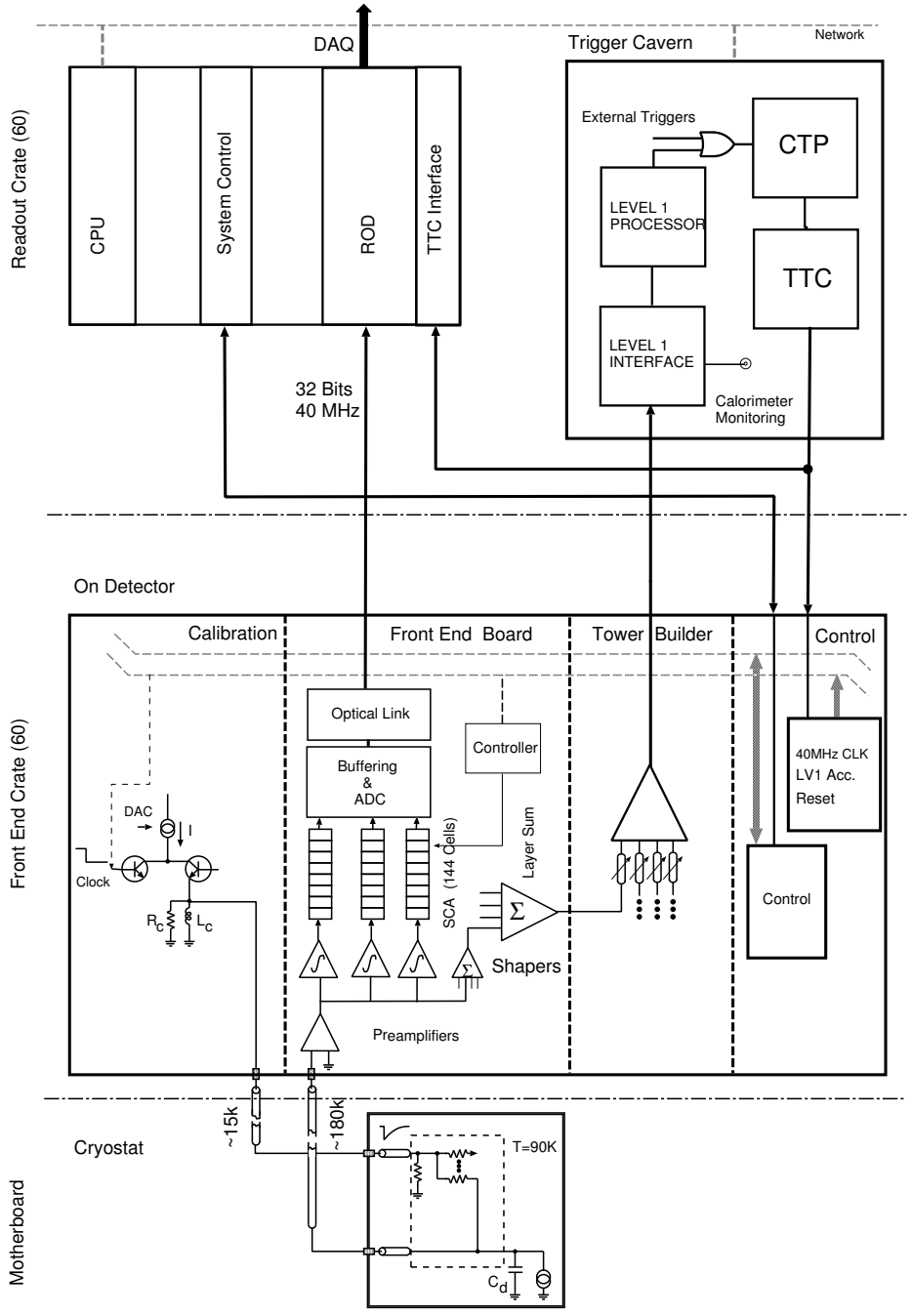


Figure 2.5: Block diagram of the ATLAS LAr readout electronics (taken from Ref. [12]).

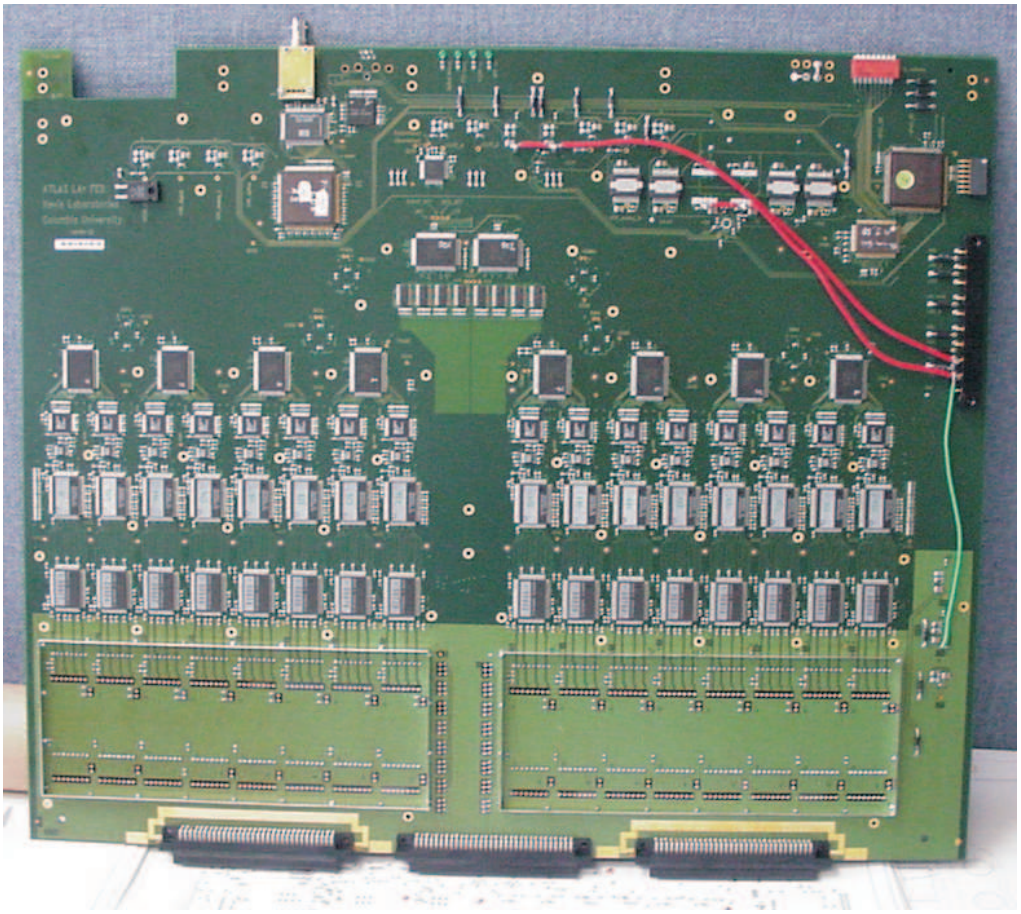


Figure 2.6: ATLAS front-end readout board (from Nevis Laboratory, Columbia University).

The preamplifiers should thus be the sole contributers of electronics noise [12]. In the shapers the signals are converted from the triangle pulses (triangular in charge versus time with a negative slope) coming from the electrons drifting in the liquid argon to bipolar pulses[§]. The shapers also amplify the signals by a factor of 10 and by a factor of 100 and pass the three signals, along with a reference signal, to analog pipelines for storage. The analog pipeline memories, based on switch capacitor arrays (SCAs) [14], store the three signals associated with each calorimeter cell read out.

The bipolar signals charge a capacitor in the pipeline every 25 ns. Each charged capacitor is said to have "sampled" the signal at a particular time. Typically 5 sequential

[§]The bipolar signals are voltages that vary with time and have positive and negative slopes (Figure 2.8).

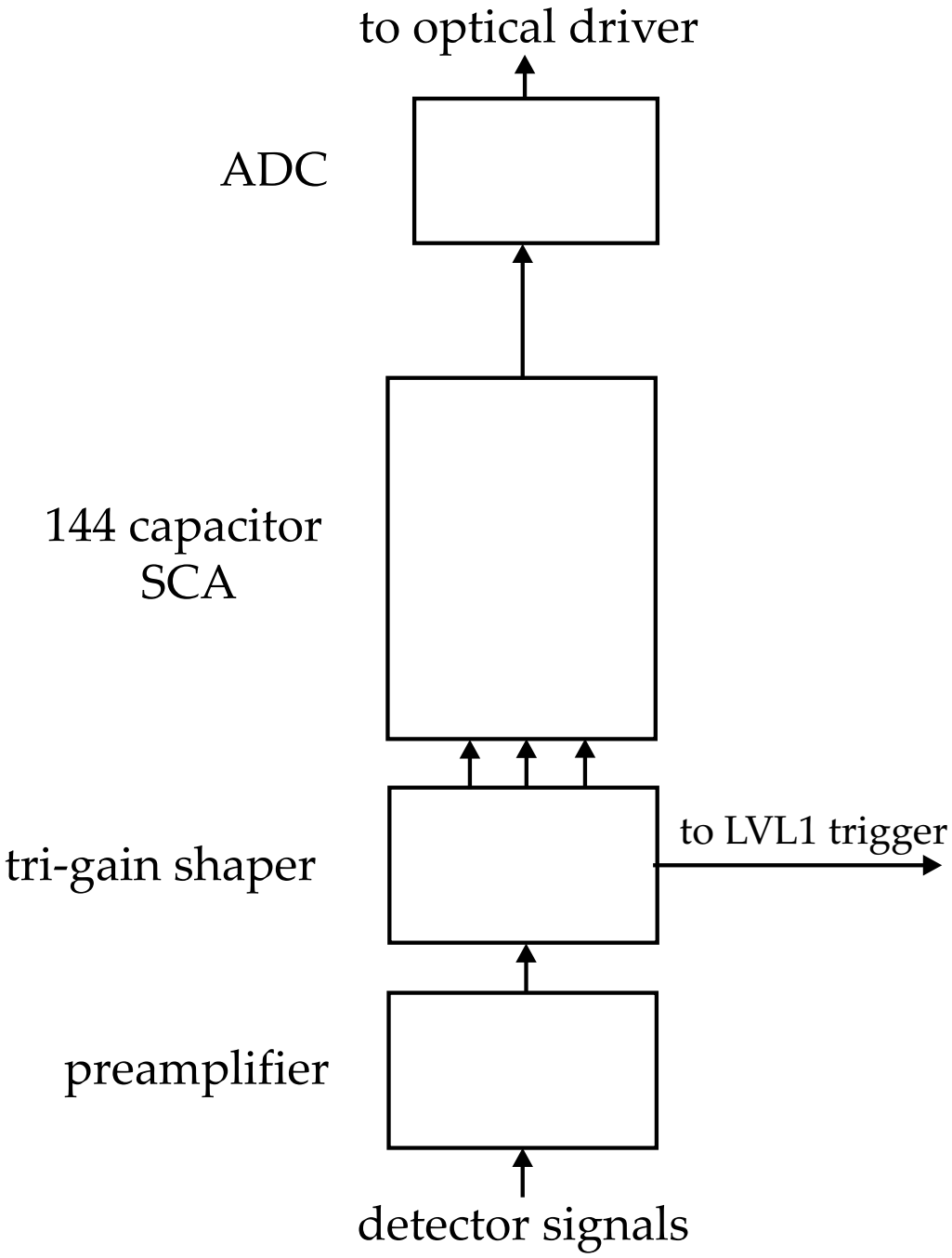


Figure 2.7: Simplified block diagram of 4 channels of the analog readout chain.

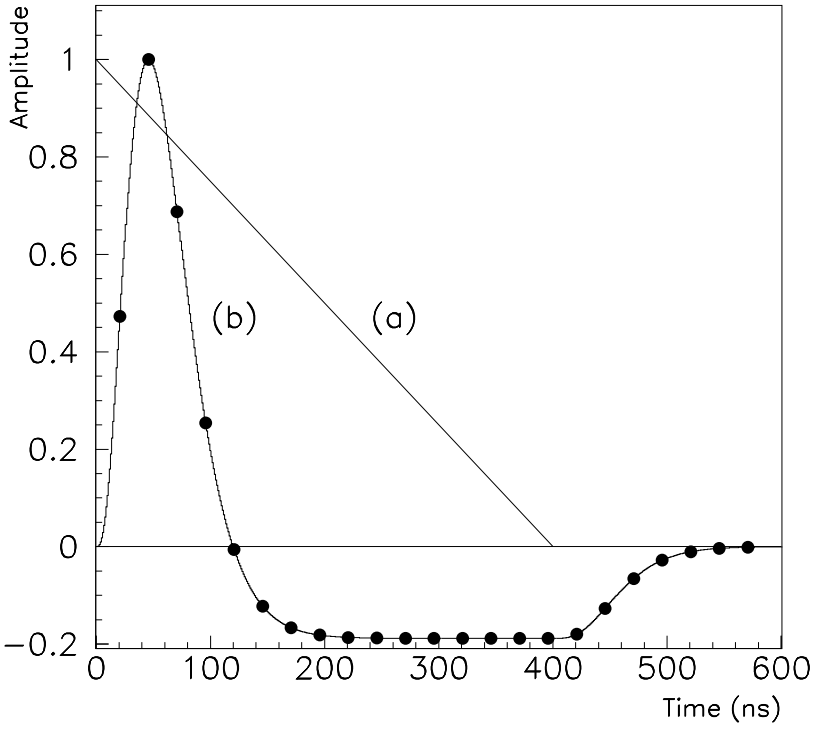


Figure 2.8: Diagram of the pulses coming from the detector before and after shaping. Pulse (a) is the triangular pulse coming from the electrode in the calorimeter, while the pulse in (b) is the bipolar pulse that results from the shaping procedure. Pulse (a) is in units of charge, while the units of (b) are voltage (from Ref. [7]).

samples, will correspond to the pulse for an event in each channel. Five samples will allow the shape, and more importantly the time and maximum of the bipolar signal to be determined above pile-up. Each pipeline memory will contain 144 capacitors times 4 channels in each SCA, allowing 7 5-sample events to be stored in addition to 100 cells needed to cover the 2.5 μs trigger latency. The SCA is a random access memory since the read and write busses are separate (a write is independent of a read) and thus access time for any storage cell[¶] is the same. Reading and writing events in the SCA pipeline can occur simultaneously. The read and write addresses will be supplied by the SCA controller chip, which will be described in more detail in the next section. The controller chip will also receive signals from the timing, trigger and control distribution receiver chip (TTCrx), which provides timing and trigger accept signals, and the gain select chip, which determines the gain at which to digitize the pulse.

Once a trigger decision to read the event has been made, the corresponding 5 samples are digitized and read out. The sample near the peak of the signal is first digitized at the medium ($\times$10) gain and compared to two reference voltages which determines which of the three gains will be digitized for subsequent samples. This approach avoids the need for analog comparators [15]. The analog-to-digital converters will have a dynamic (voltage) range of 12-bits and multiplexing will be used to reduce cost, board space, and power. The digitized events will then be sent, via optical links, to the readout drivers some distance away.

2.5.2 Switch Capacitor Array Controller

The function of the SCA controller (SCAC) is to control the FEB (the SCACs are the two large chips at the top of the board in Figure 2.6). This is achieved by keeping track of the addresses corresponding to SCA capacitors which are free (write addresses) and those that correspond to data awaiting trigger decisions (read addresses). In addition to this function, the SCAC will also provide event information to the gain selector chip [16, 17]. The basic operation and data flow is shown schematically in Figure 2.9. The SCAC contains a series of first-in first-out (FIFO) memories for keeping track of the read and write

[¶]A storage cell is any capacitor with switches for reading and writing in the analog pipeline, i.e. there will be 144 storage cells per channel.

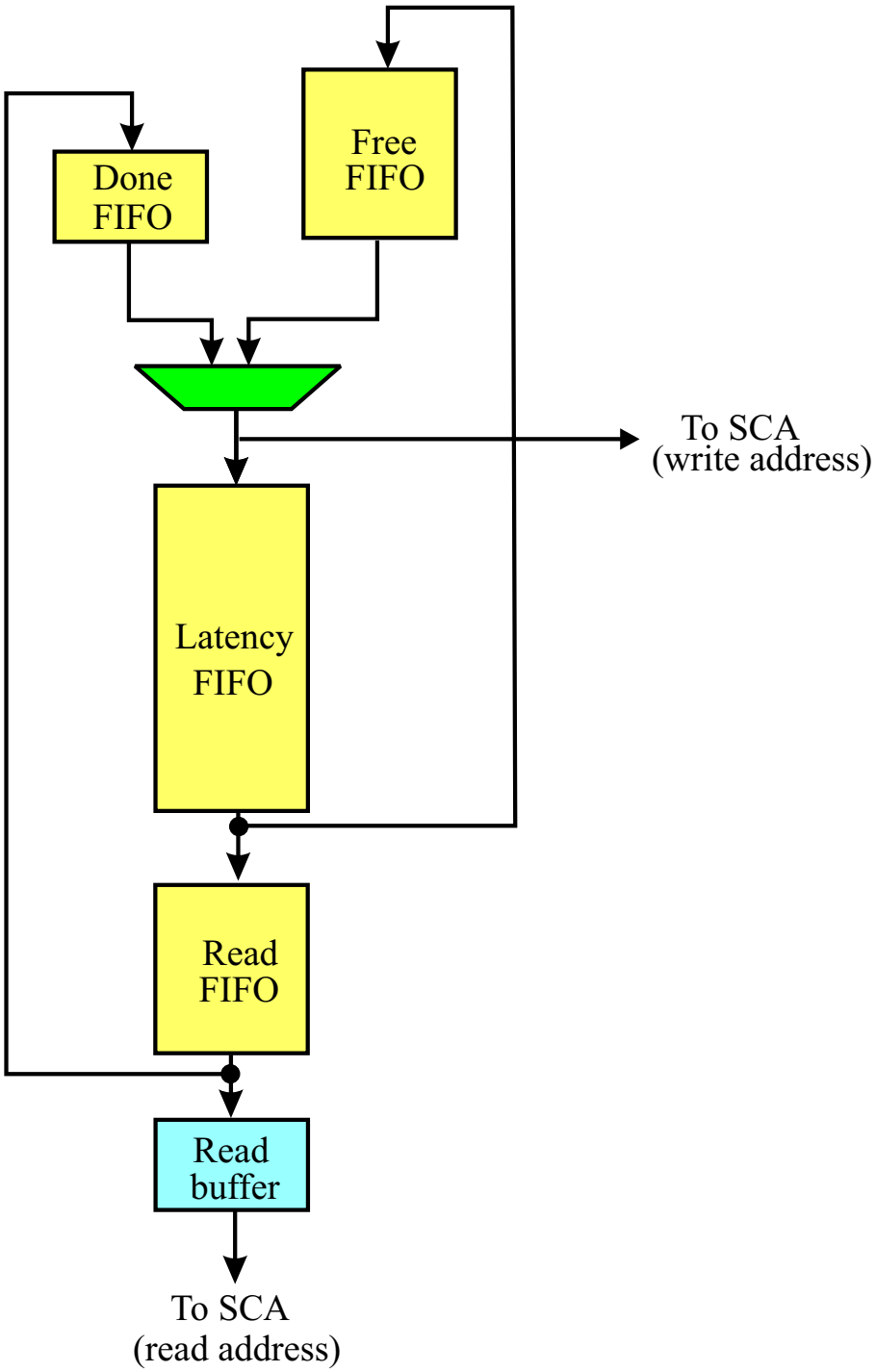


Figure 2.9: SCA address flow diagram for SCAC (taken from Ref. [18]). This diagram shows the address flow scheme used for the circuit in the DMILL and FPGA versions of the SCAC [16].

addresses for the SCA. There will be 144 8-bit addresses continuously cycled through the SCAC. As a sample is written to the SCA, the corresponding address, is passed to the LATENCY FIFO from the FREE or DONE FIFOs. The memory addresses in the LATENCY FIFO are stepped through at the bunch crossing rate (40 MHz). After passing through the LATENCY FIFO the addresses will either be passed to the READ FIFO if they are part of an event that has been selected by the trigger, or they will be passed to the DONE FIFO for reuse. Once events have been read out, the corresponding addresses, along with event and gain information, and a status word, will be passed to the DONE FIFO for reuse. To preserve the monotonically increasing order of the addresses a comparator is used to select the address from the DONE or FREE FIFO that best preserves the correct ordering. To reduce addressing noise in the SCA the addresses are Gray encoded[‖].

The SCAC also provides read addresses, bunch crossing identification numbers, gain bits and a status word to the gain selector chips [19]. There will be one SCAC device for every 64 channels, or two controllers for every front-end board.

It is crucial that the SCAC be operated in perfect synchronization with the accelerator and LVL1 trigger to ensure that events are properly identified. The TTCrx interfaces with the SCAC to provide trigger accept and device reset signals for the counters continuing the bunch crossing identifiers and the event number, which identifies the event for later reconstruction. The TTCrx will also provide an initialization signal, which will cause the SCAC to reset all state machines and renew proper operation. The addresses coming from the two SCACs on a FEB are compared by the ROD. If there is a difference between the two addresses it would mean that the one of the addresses has become corrupted, possibly by radiation, or that one of the SCACs has "locked up" and ceased to correctly function or some other component in the chain is at fault. If a difference is detected, a signal is sent to the TTC system which issues a reset to the appropriate TTCrx to ensure that the FEB and SCAC are properly synchronized again and operation resumes.

Various other bookkeeping tasks will also be performed by the SCAC, in the form of debugging tasks and sample ordering.

[‖] A Gray code is a homomorphic mapping from a sequentially ordered sequence of numbers to a sequence of numbers that each differ by a single bit. Gray encoding is used to reduce switching noise in a digital system.

2.6 ATLAS Radiation Environment

High energy hadron colliders present varying amounts of challenges and complications with respect to radiation levels in and around associated experiments [20, 21, 22, 23, 24]. The combination of high energy protons colliding at high collision rates will contribute to large radiation backgrounds in the vicinity of the interaction region [25, 26, 27]. The increasing trend in relative radiation levels in modern colliders is roughly shown in Figure 2.10. The relative dose rate is plotted against the product of the nominal luminosity and the centre of mass energy. The 100 TeV collider shown in Figure 2.10 represents a scenario where the LHC is operated at the same luminosity, but at a higher centre of mass energy.

Radiation levels within detectors will scale approximately as the inverse square of the distance in the detector from the interaction region and therefore components in the innermost parts of ATLAS, such as those within the inner tracker, will operate in the highest radiation fields. Even at a distance of 3 m from the interaction region, roughly where the LAr readout electronics will reside, the radiation levels will still be large enough to be detrimental to the electronics located there. This thesis concentrates on the efforts to qualify the SCAC, or to determine that it will function satisfactorily in the ATLAS detector for ten years. This qualification process is not unique to the SCAC. Other groups are involved in similar efforts for devices to be used on the ATLAS LAr front-end board and a brief review of these can be found in Ref. [28]. Simulations of the radiation levels within the ATLAS detector have been done by Mike Shupe of the University of Arizona using the GEANT3 simulation package with the GCALOR interface [29]. To simulate the levels in the LAr electronics region secondary particles were tracked through the inner detector and liquid argon calorimeter to the electronic crate region. The spectra of particle fluxes in the region containing the LAr readout electronics are histogrammed in Figure 2.11. It was important to have the simulated particle spectra as they provided a means to determine the radiation tolerance** requirements for devices to be operated in ATLAS. The particle spectra were also considered when choosing appropriate radiation facilities for device

**Radiation tolerance describes the radiation levels at which a device will continue to function acceptably, whereas radiation hardness is a measure implicit in the design of a device. Some devices might be radiation hardened against the effects caused by ionizing radiation and would thus be said to be designed to prevent ionizing radiation effects. Such devices would have a high tolerance against ionizing radiation.

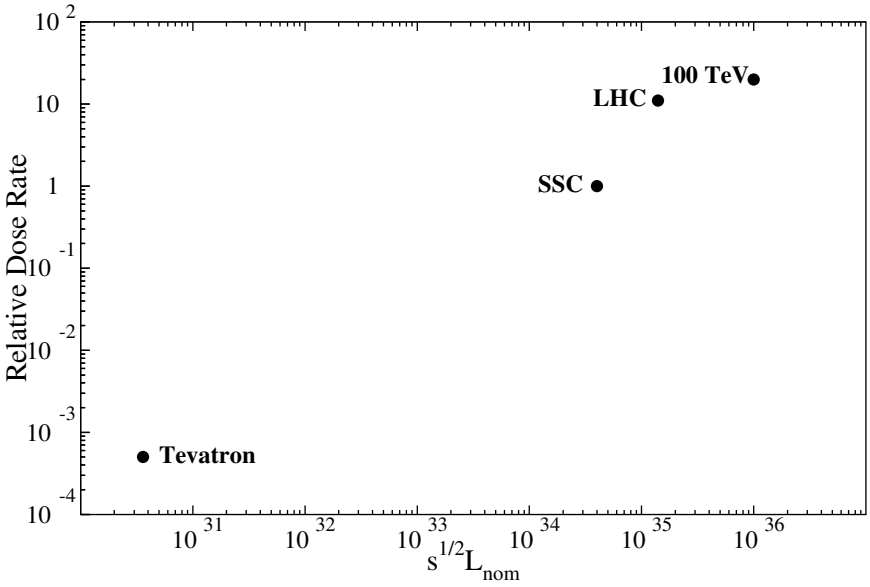


Figure 2.10: Relative radiation levels at various hadron colliders plotted against the product of the centre-of-mass energy and the nominal luminosity. Data is from Ref. [22]

testing.

In order to simulate the particles and energy deposition relevant to determining the effects of radiation on electronics, the electronic crate region was replaced with a single volume of silicon and the deposited energy and associated 1 MeV equivalent in Si neutron flux of the particles penetrating the region were calculated. Details pertaining to types of damage and other radiation-related quantities are discussed in Chapter 3.

The TID, hadron flux, and 1 MeV equivalent in Si neutron flux, are shown in Figures 2.12, 2.13, and 2.14 respectively. The space was divided into segments 10 cm in radius, R, from the beam axis and 10 cm in distance, Z, along the beam from the interaction region[††]. The worse case values of each type of radiation quantity was determined over the region containing the crates (Table 2.1). The total ionizing dose levels and charged hadron environment, both flux and energy, in the region of the LAr readout electronics are similar to those that exist in outer space in the vicinity of the Earth (i.e. in orbits where spacecraft routinely fly) [30]. The total ionizing doses and neutron fluences in the electronics regions will be many orders of magnitude smaller than those in the proximity of a

[††]The radiation is expected to be symmetric in azimuthal angle, ϕ.

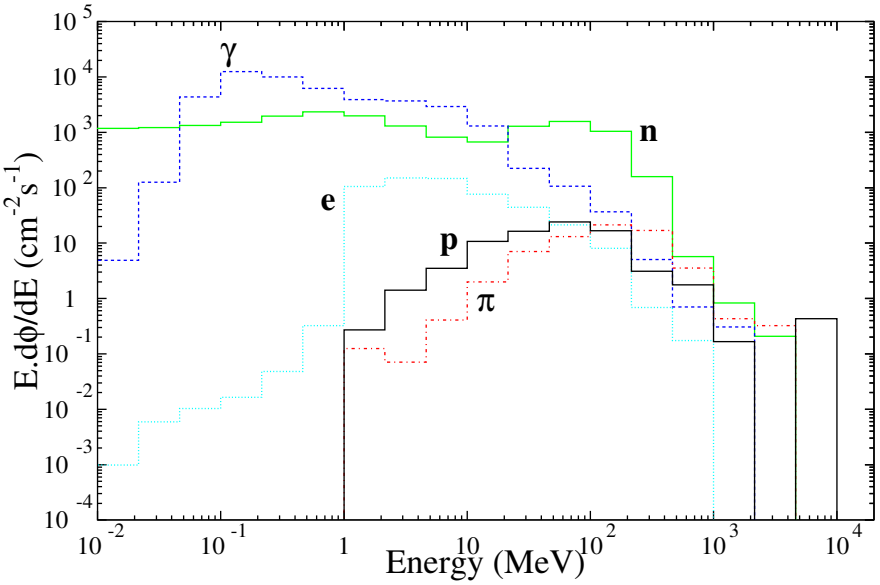


Figure 2.11: Particle fluxes in crate region that houses the readout electronics for the barrel liquid argon calorimeter.

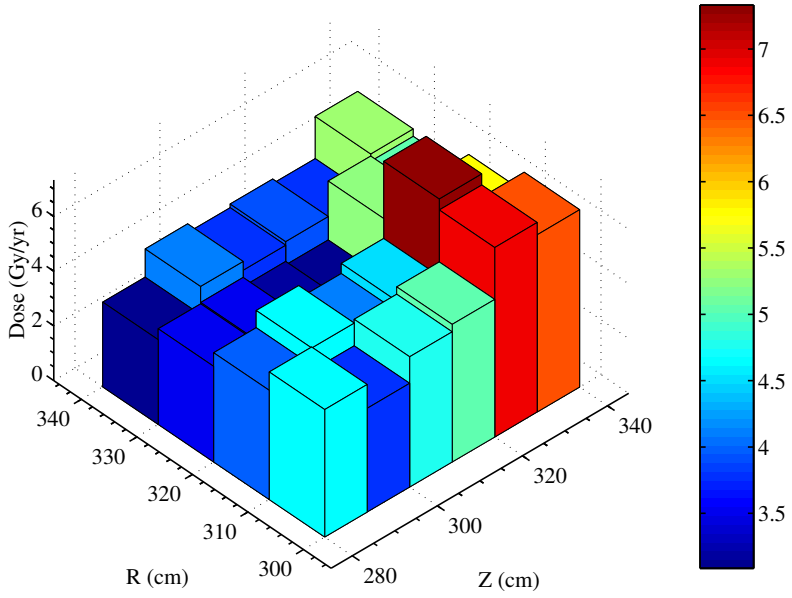


Figure 2.12: Total ionizing dose rate map of the region that houses readout electronics for the barrel liquid argon calorimeter.

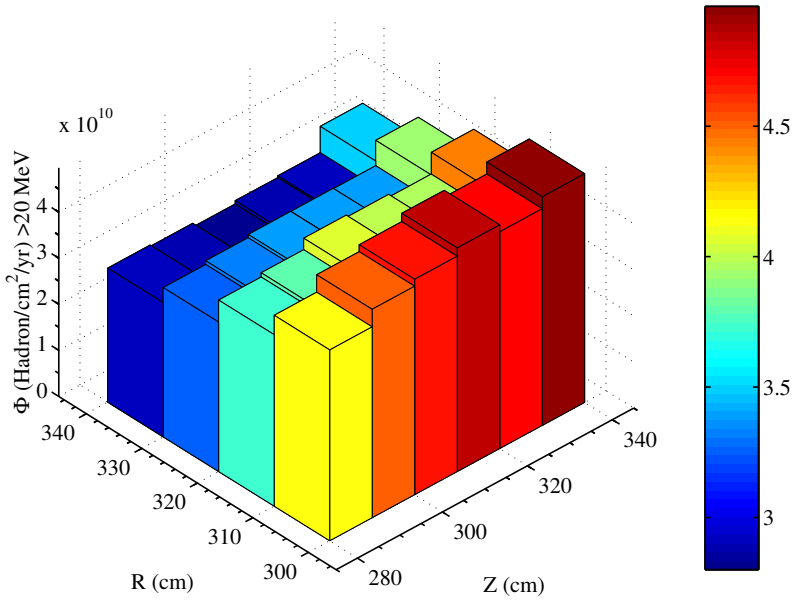


Figure 2.13: Integrated flux map of particles (E > 20 MeV) in the region that houses readout electronics for the barrel liquid argon calorimeter.

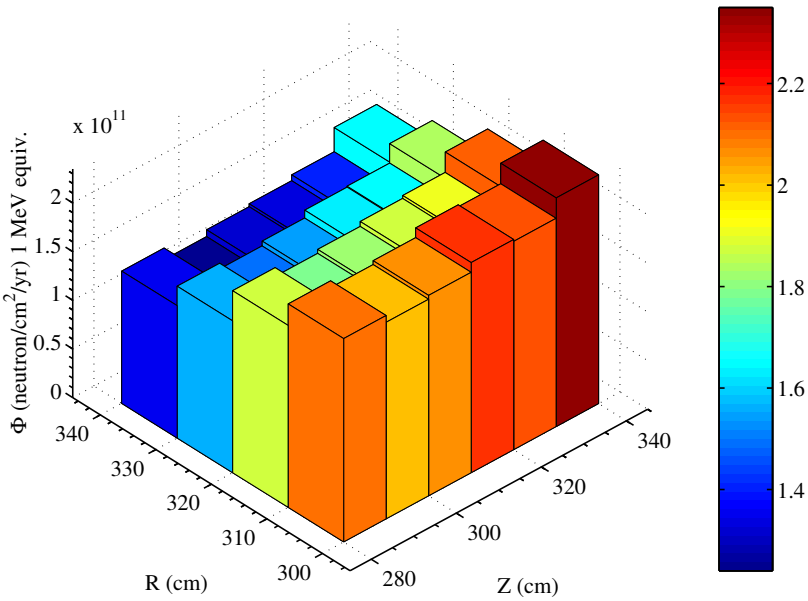


Figure 2.14: Integrated flux map of 1 MeV equivalent in Si neutrons in the crate region that houses readout electronics for the barrel liquid argon calorimeter.

Location	Radiation	Worse Case Value
Front-end Board	Total Ionizing Dose	7.3 Gy/yr
	Hadron Flux	5.0×10^{10} h/cm^2/yr
	Equivalent Neutron Flux	2.4×10^{11} n/cm^2/yr
SCAC	Total Ionizing Dose	3.94 Gy/yr
	Hadron Flux	2.87×10^{10} h/cm^2/yr
	Neutron Equivalent Flux	1.34×10^{11} n/cm^2/yr

Table 2.1: Worse case values of radiation within the location of the FEB, and the region of the SCAC.

nuclear reactor. The SCAC will be located within the small region of 300 cm $< Z <$ 320 cm and 330 cm $< R <$ 340 cm. It can be seen from the radiation maps that the SCAC will be situated in a part of the crate where the radiation levels will be smaller than the average within the space occupied by the FEB. The fluxes used in rate calculations were taken to be the predicted worse case flux in the SCAC region.

2.7 Radiation Qualification Process for Electronics in ATLAS

Due to the high radiation environment within the ATLAS detector and the limited access[‡‡] to the electronics residing there, a policy has been developed to ensure that electronic devices used in ATLAS are reliable. This section summarizes the ATLAS radiation tolerance policy and related qualification procedures. A comprehensive definition of the policy can be found in Ref. [31].

A list of components required for the ATLAS detector was compiled and the radiation levels within the detector were simulated (the latest version of which were described in Section 2.6). A set of radiation tolerance criteria (RTC) was compiled for various regions within the detector and for various electronic technologies. Table 2.2 contains the relevant RTCs for the region of the detector where the SCAC will be situated. The RTCs are defined to be the simulated radiation levels (SRL) at the location of interest multiplied by three safety factors (SFs). One SF (SF_{sim}) corresponds to inaccuracies in the SRLs due to the uncertainties in the simulation of the radiation levels. A second SF (SF_{ldr}) accounts for

[‡‡]In addition to the induced radioactivity of the detector components after LHC operation, there will be limited access to the region of the detector since the LAr readout electronics are embedded in the detector.

Technology	Radiation Effect	SRL (10 yr)	SF			RTC (10 yr)
			SIM	LDR	LOT	
Rad-hard ASIC	TID	39.4 Gy(Si)	3.5	1.5	2	414 Gy
	NIEL	1.34×10^{12} n/cm^2	5	1	2	1.34×10^{13} n/cm^2
	SEE	2.87×10^{11} h/cm^2	5	1	2	2.87×10^{12} h/cm^2
COTS	TID	39.4 Gy(Si)	3.5	5	4	2.76 kGy
	NIEL	1.34×10^{12} n/cm^2	5	1	4	2.68×10^{13} n/cm^2
	SEE	2.87×10^{11} h/cm^2	5	1	4	5.74×10^{12} h/cm^2

Table 2.2: Radiation tolerance criteria relevant to the SCAC. Values calculated using procedure outlined in Ref. [31]

low dose rate effects, which is an increase in the damage produced by total ionizing dose on CMOS and bipolar devices when irradiation is applied at low dose rates (on the order of 0.1 mGy/s) [32]. The final factor (SF_{lot}) is to account for variation in radiation tolerance between lots, or production batches, and between devices within each lot. The criteria given in Table 2.2 are for commercial-off-the-shelf (COTS) devices of unknown lot, while the application specific integrated circuits (ASICs) have been manufactured using some level of radiation hardening techniques (see Chapter 4) and are from traceable lots.

The criteria from Table 2.2 must be met by any prototype device chosen for use within the ATLAS detector. In order to ensure that all chosen devices have met the criteria, a set of standards has been set for radiation tolerance testing. The production devices must also satisfy the criteria, although some SFs will be reduced [31].

The standards for radiation testing of CMOS devices have been largely based on radiation test methods and standards devised by the United States Department of Defense and the European Space Agency [33, 34, 35]. The standards pertain to aspects of testing such as the types of radiation that are sufficient to simulate those expected within the detector, as well as methods that must be used during the testing.

The TID testing of CMOS devices was to follow the following procedure. Ten devices, plus one used as a control are chosen. Electrical measurements and functional testing are performed on the devices prior to irradiation. The devices are irradiated, while they are under normal operating bias voltage, to the RTC_{TID} and the current is monitored during the tests, or at regular intervals. Following the test, electrical measurements and

functional tests are again made to determine if the device is functioning as it was prior to the radiation test, or *in situ* measurements can be made during testing. Irradiated devices are to be annealed, or healed of radiation damage, by leaving them at room temperature under bias. Post irradiation annealing must be done for 24 hr (and 168 hr for devices of unknown batch), after which electrical measurements and functional testing are again to be performed. Annealing is required as TID effects can continue to evolve during and after the irradiation period due to the complex nature of the charge trapping within the oxides of the device (Section 3.6).

If all of the devices successfully operate following irradiation to $\mathrm{RTC_{TID}}$ they may be chosen to be used in ATLAS, as long as they pass the other required RTC. If the device still functions after it is placed under bias and heated to 100^{o} C for 168 hr following 24 hr room temperature annealing, the low dose rate safety factor can be reduced from 5 to 1. If one device of the ten tested fails any part of the qualification procedure, the entire batch is rejected. It should be noted that the measurements made on the device during testing must be made using a dedicated test board or using an entire system board (such as a FEB). If a system board is used for testing, its architecture must be such that the functionality of each

component on it can be checked.

Single-event effects testing is to be performed to search for three types of effects: soft effects, which are transient; hard effects, which require some external intervention to be cleared; and permanently damaging effects. The SEE test procedure requires four devices plus one control device. Electrical and functional tests are to be performed on the devices prior to irradiation with protons. During testing the device is to be irradiated while other components on the test, or system, board are to be shielded from the radiation. On-line measurements must be made with soft, hard, and destructive SEEs being recorded. An estimate of the soft and hard SEE rate in ATLAS must be computed. A maximum allowable rate for soft and hard SEEs does not currently exist, but will be determined by the projected effect the SEE rates will have on the data, such as the number of missed events per SEE related failure. Any device which experiences a permanently damaging SEE will not be chosen for use in ATLAS. As with the TID tests, if any one of the irradiated devices in a batch fails to meet the $\mathrm{RTC_{SEE}}$ the entire batch is rejected. It is required that protons

with energies between 60 MeV and 200 MeV be used to test a device for soft SEEs and that protons with energies between 200 MeV and 500 MeV be used to test a device for hard or permanent SEEs.

Testing for displacement damage effects (or alternatively non-ionizing energy loss effects) requires ten devices for irradiation and one device to be used as a control. As with the TID and SEE tests, electrical measurements and functional testing must be performed before and after testing. Devices are not required to be under bias during neutron irradiations for displacement damage tests. During such tests it is important that the pins on the device are grounded so that charge build-up during irradiation can drain out of the device and not cause damage to it. If all of the devices are irradiated beyond the $\mathrm{RTC}_{\mathrm{NIEL}}$ without exhibiting degradation in operation they may be considered for use in ATLAS.

Any pure CMOS device must pass at least the SEE and TID tests to be considered for use in ATLAS. The failure of any one of the tests described above would cause the rejection of the device for further consideration.

Chapter 3

Electronic Devices and the Effects of Radiation On Them

The effects of radiation on electronic devices is a complex field of study. Different types of radiation will affect different types of devices in different ways. This thesis deals with the effects of radiation on the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) devices. The chapter consists of three parts: an introduction to various types of radiation, an overview of electronic devices, and the effects of radiation on MOSFET-based micro-electronics.

3.1 Types of Radiation

Radiation is defined as energy radiated in the form of waves or particles [36]. Radiation can come in many forms. For the purpose of this work radiation will refer to the energy radiated in the form of leptons, charged and neutral hadrons, and photons.

Photons are quanta of electro-magnetic energy and will only interact with charged particles. Photons will participate in any electro-magnetic interaction and can be introduced via reactions, such as the annihilation of an electron and positron pair.

Leptons and hadrons are fundamentally different types of particles. Leptons are considered to be fundamental, without internal structure, while hadrons are not. Hadrons can contain as few as two quarks, such as the kaon, or many, such as a helium nucleus*.

*Typically the term hadron refers to a single particle like a meson or nucleon, but it will be convenient to refer to nuclei in the same manner

For the purpose of the work described in this thesis, the distinguishing features between types of charged particles will be the magnitude of charge and mass.

3.2 Interactions Between Radiation and Matter

The interactions between different types of radiation and matter can be broken down into two basic types: electro-magnetic and nuclear. The details of nuclear interactions can be quite complex, but for this work it is possible to assume a nuclear interaction is either elastic or inelastic and neglect the deeper details. The interactions between charged hadrons and matter will be discussed, followed by the interactions between neutrons and photons and matter.

3.2.1 Interactions Involving Charged Particles

Charged hadrons can take part in both electro-magnetic and nuclear interactions with matter. At different energies different types of interactions will occur with different probabilities. In general the electro-magnetic interactions between the incoming charged particle and electrons in the medium will dominate. Nuclear interactions will occur less frequently. A 100 MeV to 500 MeV proton, for example, will take part in a nuclear interaction once for every 10^9 electronic interactions. The differential energy lost per track length for a charged particle moving through a medium is given by the Bethe-Bloch formula[37],

$$-\frac{dE}{dx} = \frac{4\pi z^2 e^4}{m_0 v^2} NZ \left[ln\left(\frac{2m_0 v^2}{I}\right) - ln\left(1 - \frac{v^2}{c^2}\right) - \frac{v^2}{c^2} \right], \tag{3.1}$$

where z, and v are the atomic number and velocity of the incident particle, N and Z are the number of atoms per cubic centimeter and atomic number of the medium, e is the unit of electric charge, m_0 is the electron mass, I is the mean excitation energy of the medium, and c is the speed of light in the medium. It can be seen that the energy loss is most sensitive to the properties of the incident particle, where it is proportional to the square of its charge, z, and inverse square of its velocity. Figure 3.1 shows the dE/dx curves for several particles. The energy lost by the particle is used to ionize atoms in the medium. This will become important in the discussion on radiation damage in electronic devices.

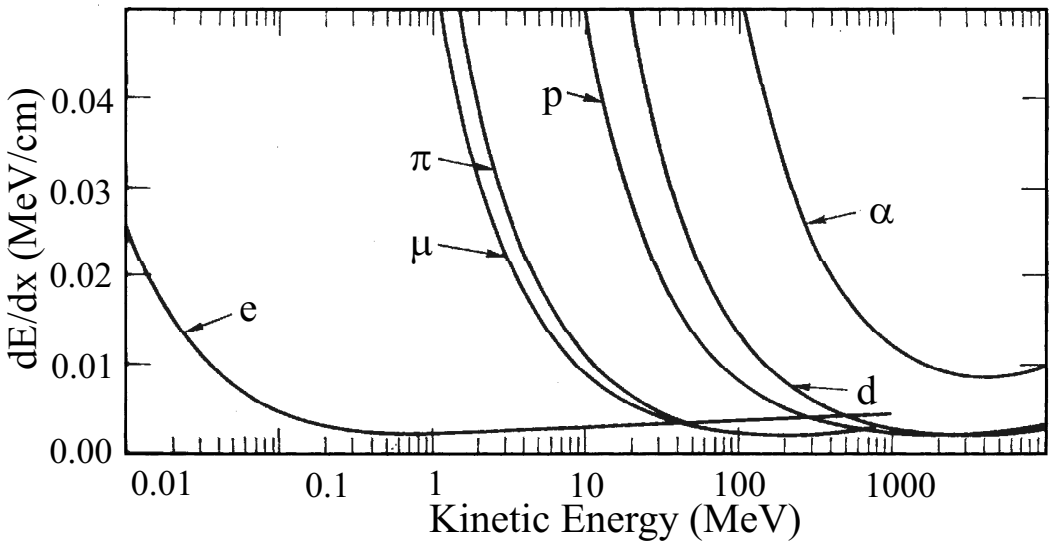


Figure 3.1: Differential energy loss per path length for electrons, muons, pions, protons, deuterons, and alpha particles (taken from Ref. [38]).

Nuclear interactions between charged particles and the nuclei in a material will occur when the incident particles obtain sufficient energy to overcome the coulomb barrier presented by the target nucleus. The nuclear interaction may be elastic or inelastic with the probability of each being dependent on the energy of the incident particle. In the case of an elastic interaction, the target ion will be displaced to some degree while the incident particle will be scattered at some angle, whereas for an inelastic interaction there will be a number of products emitted after the collision which may in no way resemble the initial ion and nucleus. In either case the products of a nuclear reaction will propagate through the medium interacting in the same manner that the initial ion interacted with the medium. Figure 3.2 shows the flow of radiation following the initial ion entering the medium. The incident ion and products of interactions between it and the medium will continue to move through the medium, losing energy via electro-magnetic and nuclear interactions, until they are stopped in the medium or leave it. As the incident ion traverses the medium it will continue to lose energy, as per equation 3.1 until the kinetic energy of the particle is depleted. The distance a charged particle of energy E_0 will pass through a

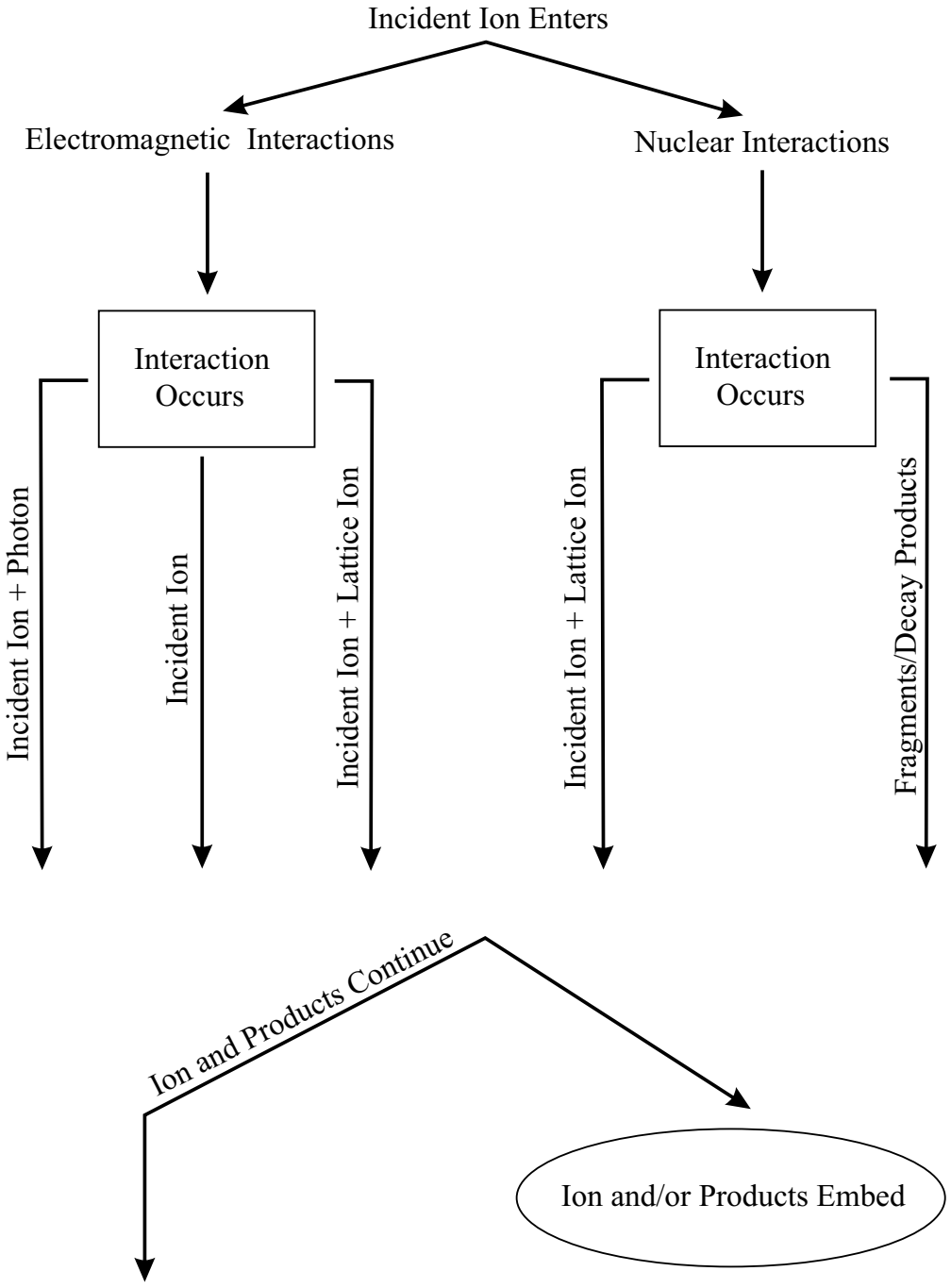


Figure 3.2: Diagram of the flow of interactions within a medium initiated by an incident charged hadron or ion. The interactions will be either electro-magnetic or nuclear and the process will occur until the incident ion and all of the interaction products come to rest in the medium, or exit it.

Incident Ion	Energy (MeV)	Target Medium	Range (μm)
p	1	silicon	16
	10		710
	100		42,000
^{28}Si	1	silicon	1.3
	10		5
	100		35
p	1	hard plastic (PVC)	18
	10		880
	100		54,000

Table 3.1: Ranges for protons and silicon ions. Values calculated using SRIM 2000 [42].

medium before stopping is referred to as the range, R, and is given by

$$R(E_0) = \int_0^{E_0} \left(\frac{dE}{dx}\right)^{-1} dE. \tag{3.2}$$

Table 3.1 shows some examples of ranges for protons and silicon in solids. As the ion slows it will begin to lose energy more rapidly near the end of its path, which is called the "Bragg peak", as can be seen in Figure 3.3. Once the ion has reached an energy of approximately $1/(2z^2)$ MeV, where z is the charge of the ion, it will begin to capture electrons [39]. The rate of energy loss will be less for the ion as it is becomes screened by the captured electrons and this corresponds to the sharp drop in the energy loss in the Bragg peak.

3.2.2 Interactions Involving Neutrons

Neutrons will only be involved in nuclear interactions. As stated in the last section, nuclear interaction can be either inelastic or elastic, depending on the energy of the particle. Of course neutrons will not be affected by the coulomb force of the nucleus, or surrounding electrons, which means that they can penetrate the nucleus at virtually any energy. The lack of coulomb interactions between neutrons and the medium allows them to penetrate deep into those materials. This property has given rise to the extensive field of neutron scattering (see Ref. [40] for example).

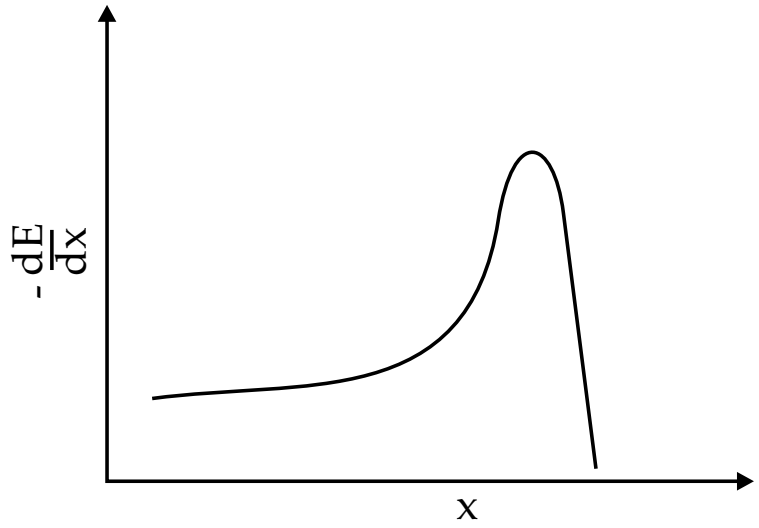


Figure 3.3: The Bragg curve showing that an incident ion will lose energy most rapidly near the end of its path.

3.2.3 Interactions Involving Photons

After the incident particle collides with either the target nuclei or target electrons, there will be a forward cascade of radiation. In the case of incident photon radiation this is not exactly the case. If a material is sufficiently thick and a photon is incident on a medium it will most likely interact with an electron in the medium. A photon can interact with a medium in a number of ways, as will be explained in the next section, but once it has interacted it is unlikely that it will be emitted again in the same direction. This fact leads to the "perfect geometry" approximation, which states that once a photon in a narrow beam of such photons interacts with the medium it will be removed from the beam. This approximation is widely used for dosimetry[†] calculations [43, 44] and will be used throughout the remainder of this thesis.

The intensity of a beam of photons passing through a medium is described by

$$I(x) = I(0)e^{-\mu x}, \tag{3.3}$$

where $I(x)$ is the intensity of the beam at distance x from the point it entered the medium, $I(0)$ is the intensity of the beam before it enters the medium, and μ is a parameter describ-

[†]Dosimetry is the method of determining the amount of energy deposited within a substance.

ing the probability of losing a photon from the beam in a unit distance. The inverse of μ is the mean path length of a photon in an infinite medium.

From equation 3.3, it can be seen that the mathematical definition of μ, the linear mass attenuation coefficient, is

$$\mu = \frac{1}{N}\frac{dN}{dx}, \tag{3.4}$$

where N is the number of un-collided photons. In practice, the mass attenuation coefficient is the sum of the linear absorption and linear scattering coefficients, μ_a and μ_s, which correspond to the fraction of beam energy absorbed by the medium and scattered by the medium respectively. The quantity of interest when considering radiation effects is the linear absorption coefficient. The processes which contribute to the linear absorption coefficient are the photo-electric effect, incoherent Compton scattering, and pair production. The total linear absorption coefficient μ_a is given as

$$\mu_a = \mu^{phot} + \mu_a^{comp} + \mu^{pair}, \tag{3.5}$$

where μ^{phot}, μ_a^{comp}, and μ^{pair} are the photo-electric, Compton absorption, and pair production mass attenuation coefficients respectively. Figure 3.4 shows the linear absorption and scattering coefficients for photons in air. The coefficients in this plot have been divided by the atomic density of the absorbing medium[‡] and are referred to as linear mass attenuation coefficients. It can be seen that the coefficients pertaining to different processes dominate at different energies. At the lowest energies the photo-electric effect dominates while pair production dominates at high energies. Figure 3.4 also shows that the scattering coefficient consists entirely of the Compton scattering coefficient. The scattering coefficient describes the energy scattered out of the material, whereas the absorption coefficient describes the energy absorbed in the material. Lower energy photons will have lower momentum transfers and thus will contribute less energy to the material [45].

[‡]Dividing the attenuation coefficient by the atomic density is done so that the attenuation coefficient is independent of the physical state of the medium (i.e. the mass attenuation coefficient for water in liquid form and vapor form would be the same for photons of the same energy.

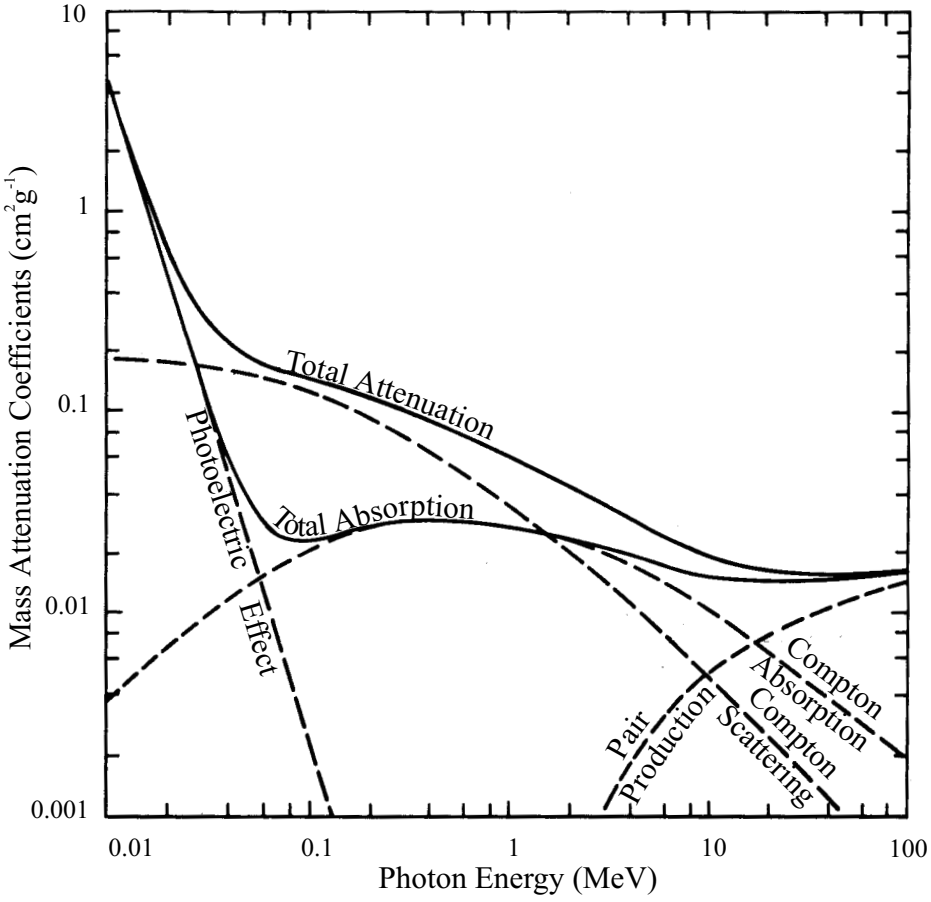


Figure 3.4: Mass attenuation coefficients for photons in air. Taken from Ref. [37]

3.3 Introduction to Semiconductor Devices

In order to understand the effects of radiation on semiconductor-based microelectronic devices, the physics of semiconducting materials is reviewed. A semiconducting material is a material made up of atoms often found in the carbon family of elements[§].

Solids are typically divided into three classes: insulators, conductors, and semiconductors. These classes refer to the conduction properties, or more precisely, the band gap of the material. The band gap, or separation between the top of valence energy band and the bottom of conduction band, varies from material to material. For the case of an insulator the band gap is quite large, several units of eV, which prevents electrons from "jumping" from the valence band to the conduction band. The case of a metal is the opposite to that of an insulator. There is no bandgap in metals and thus the bands overlap. In a metal most or all of the electrons are in the conduction band. Electrons in a metal are described as being shared by all of the ions in the lattice. Metals are excellent conductors. The most complicated, and arguably interesting, of the three classes of solids is the semiconductor. The band gap in a semiconductor is around 1 eV. Three common semiconductors, silicon (Si), gallium arsenide (GaAs), and germanium (Ge), have band gaps (at room temperature) of 1.12 eV, 1.42 eV, and 0.66 eV respectively. Thermal energy can be used to excite a moderate number of electrons (holes) in the conduction (valence) band in a semiconductor. Electrons or holes that have been excited into conduction are called carriers. This property lends itself well to the use of semiconducting materials in electronic devices. The following section describes how semiconducting materials can be manipulated to provide electronic devices.

3.3.1 Carrier Concentration and Doping in Semiconductors

An intrinsic, or pure, semiconductor will contain as many electrons as holes in the conduction band, independent of temperature. Therefore, as the semiconductor is electrically neutral, the number of holes per unit volume, or carrier concentration will be the same as the number of electrons per unit volume. For silicon at room temperature (300 K) the carrier concentration is 1.45×10^{10} cm^{-3}.

[§]They can also be made up of molecules containing atoms from more than one elemental family, such as gallium arsenide.

In order to control the behaviour of semiconductors, impurities can be added to them. The addition of impurities is called doping and will change the balance of electrons and holes within the material. Doped semiconductors exist in two forms, negatively doped and positively doped. A negatively doped (or n-type) semiconductor will have a larger concentration of electron carriers and is therefore referred to as having electrons as the majority carriers. The holes in an n-type semiconductor are the minority carriers. A positively doped (or p-type) semiconductor will have holes as the majority carriers. The process of adding dopants to a semiconductor is beyond the scope of this work, but as an example for silicon, negative dopants (donors) would be taken from the column, in the periodic table, to the right of that containing silicon, such as phosphorus or arsenide. Positive dopants (acceptors) would be taken from the column to the left, such as boron or indium. In terms of the band model of a semiconductor, the addition of a dopant will create a level, either an acceptor level or a donor level, which will sit either just above the valence band or just below the conduction band respectively. The typical energy difference between the conduction band and a donor level or the valence band and an acceptor level is on the order of tens of meV, which is on the order of room temperature energy [47]. Since the semiconductor material will still be neutral after doping, the number of carriers for an extrinsic semiconductor will obey

$$N_A + p = N_D + n, \tag{3.6}$$

where N_A is the acceptor density, N_D is the donor density, and n and p are the negative and positive carrier densities.

3.3.2 Conductivity and Recombination

The current density associated with the carriers (majority and minority) is given by,

$$\vec{J} = e(n\mu_n + p\mu_p)\vec{E}, \tag{3.7}$$

where μ_n and μ_p are the negative and positive carrier mobilities, and $\vec{E}$ is the applied electric field. From this expression and Ohm's law, it can be seen that the conductivity, σ, is given by,

$$\sigma = e(n\mu_n + p\mu_p). \tag{3.8}$$

The lifetime of a carrier is the amount of time (on average) it will be available for conduction prior to recombining with an opposite carrier. Carriers can recombine via band-to-band recombination which occurs when an electron in the conduction band combines spontaneously with a hole in the valence band. A more prevalent method by which carrier recombination occurs is when impurities (not necessarily dopants in elementally adjacent columns to the semiconductor) act as "traps" or "recombination centers". Carrier traps occur when an impurity induces a level below the conduction band or above the valence band, as in the case of dopants. In the case of dopants the levels were situated near to the conduction and valence bands and at room temperature the levels were usually vacant. Impurity levels of this type are called shallow, whereas levels situated closer to the center of the forbidden gap are called deep. Deep levels, when they occur will be filled for longer periods, thus increasing the probability that a carrier trapped in one will encounter an opposite carrier. The net effect of deep recombination centers is a reduction in the mean carrier lifetime. Impurities of these type can affect the electrical properties and performance of electronic devices.

3.4 Metal Oxide Semiconductor Field Effect Transistors

The most common use for semiconductors is the transistor. There exist various types of transistors which can be organized into two groups, bipolar and unipolar. Bipolar transistors, such as bipolar junction transistors, or BJTs, are made up of two PN junctions[¶]. Both majority and minority carriers are used in BJT operation. Another characteristic of BJTs is that they are current controlled. A small current into a terminal connected to the central region controls the behaviour of the output terminal. Unipolar transistors, such as field effect transistors (FETs), only utilize the majority carriers for their operation.

A field effect transistor is a device where the current flow though it is controlled by an applied electric field. In a MOSFET (Figure 3.5), the controlling field is produced when a voltage is applied between the gate terminal and the source. The insulator between the gate and the substrate is usually an oxide such as SiO_2 . Metal oxide semiconductor FETs belong to a broader family of devices called insulated gate FETs, which use a wide variety

[¶]A PN junction is a device made by interfacing a piece of p-type semiconductor with a piece of n-type semiconductor.

of insulators to isolate the gate from the rest of the device.

There are two types of MOSFETs, depletion, or D-MOSFETs, and enhancement, or E-MOSFETs. Each of these categories can be further divided into n-channel and p-channel devices, depending on the nature of the majority carriers used for operation.

Depletion MOSFETs are fabricated such that a lightly doped layer of the desired channel material is included between the source and drain of the device. The operation of an n-channel D-MOSFET is shown in Figure 3.5. When no voltage, or a small negative voltage is applied to the gate, positive charges will become attracted to the Si/SiO_2 interface and the electrons will be repelled. There will, however, still be a non-zero current that flows from the drain to the source (I_D), if V_{GS} is non-zero. A sufficient negative gate voltage will cause a condition where the gate-induced depletion will become sufficiently large that no current will flow between the drain and source. Each curve corresponds to a different gate voltage. When the gate voltage increases to larger positive values, the conducting channel will become filled with a larger number of majority carriers and a significant current will flow when V_{DS} is applied.

Enhancement MOSFETs are fabricated without the addition of the conducting channel and thus the region near to the oxide layer, between the source and drain, must be inverted such that it behaves as a conducting channel. An enhancement mode MOSFET will draw no current when the gate to substrate voltage is zero. A threshold voltage (V_{th}) must be achieved in order for current to flow between the drain and source.

3.4.1 Logic Gates and Memories

Transistors have many uses, such as amplifiers and switches. This thesis deals with logic devices; those which have two well defined states, "ON" and "OFF". In terms of an enhancement mode FET, an ON state refers to the case when V_{th} has been exceeded and majority carriers fill the conducting channel. The same transistor can be turned OFF by reducing the gate voltage below V_{th}.

A complementary MOSFET (CMOS) device is composed of n-channel MOS (NMOS) and p-channel MOS (PMOS) transistors in such a fashion that when one device is turned ON the other is OFF. This can be achieved by having both transistors share a common gate bias voltage. An example of a logic inverter is shown schematically in Figure 3.6

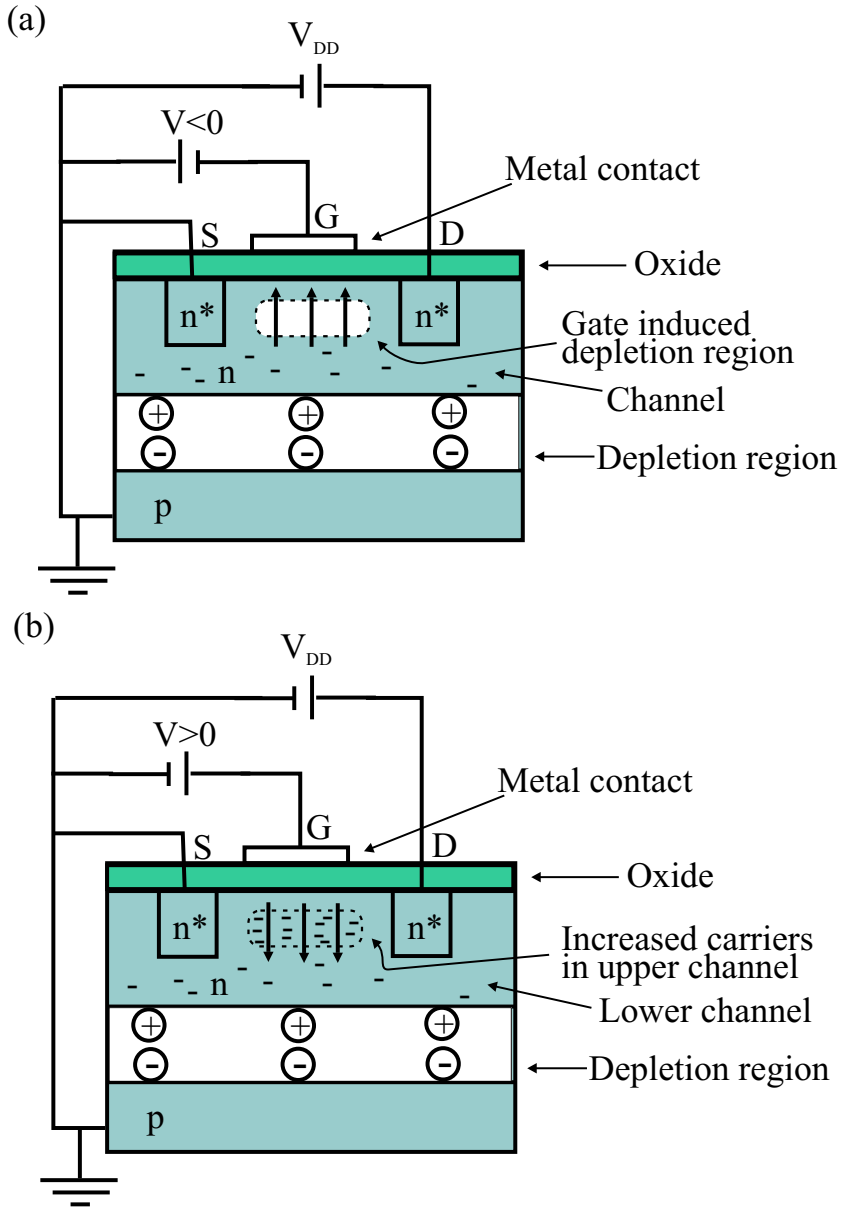


Figure 3.5: N-channel depletion MOSFET where the gate voltage is (a) less than zero and (b) greater then zero. The arrows drawn in the channel denote the electric field induced by the gate voltage. This transistor is configured for grounded source operation.

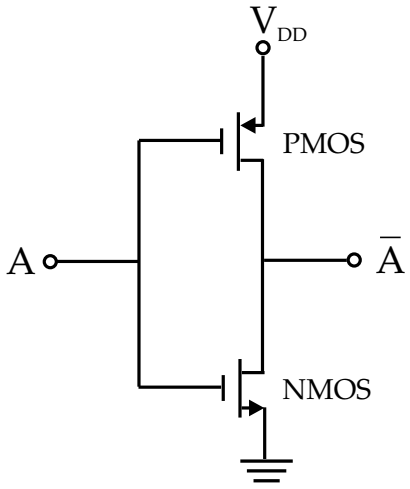


Figure 3.6: Schematic of a CMOS inverter.

and how it might look physically in Figure 3.7[‖]. For the NMOS transistor to operate the gate voltage must be set to a positive value, greater than its threshold value. This will in turn cause the PMOS transistor to shut OFF, thus current is only drawn through the two transistors during the brief switching period. Additional logic gates, such as "AND" and "OR" gates, can be made in a similar manner.

An important logic building block is the latch. A latch is a circuit that will maintain a particular state until an input to the circuit changes. Figure 3.8 shows a data latch, or D-latch made of logic gates (a round bubble on an input (output) indicates a negated input (output)). The ENABLE input determines whether the circuit will change its output (Q), and inverted output ($\overline{Q}$) with the DATA input. If there is a voltage on the ENABLE input, Q will follow the DATA input. If the ENABLE input is grounded, Q will maintain its state regardless of the state of the DATA input. A latch is a fundamental memory cell that stores a single bit. Several latches can be connected together to store a string of bits, such a register, where data is loaded and unloaded to or from the register in a particular order. For example, eight bits can be serially "shifted" in or out of a register. Digital systems also require the ability to save and retrieve data as required. In order to do this an addressing mechanism must be used, where an address is the location of a memory cell, or bit. Such

[‖]In Figure 3.7 the n^+ and p^+ regions are heavily doped with the corresponding type of carriers. The region between the NMOS and the PMOS transistors is filled with p^+ material to prevent the flow of leakage current between them. The entire device is deposited on a piece of bulk positively doped silicon.

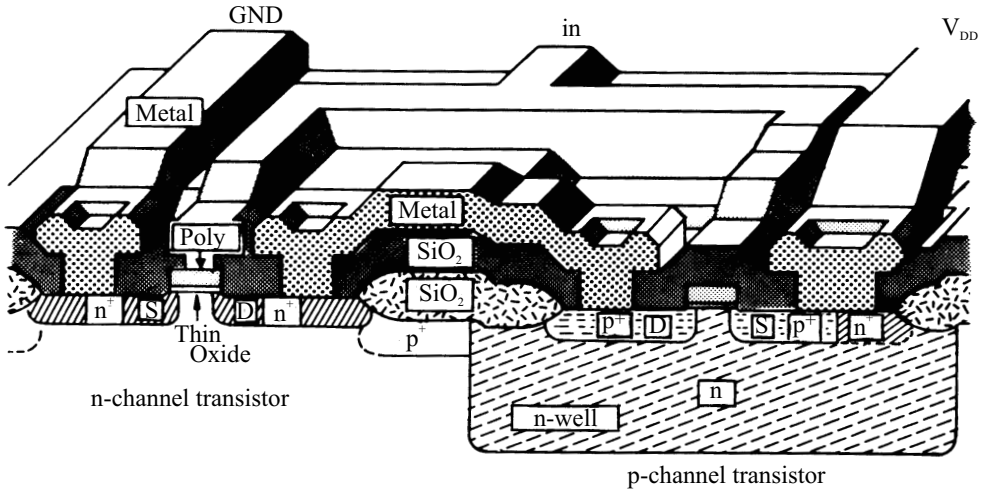


Figure 3.7: Cut-away of a CMOS inverter.[46]

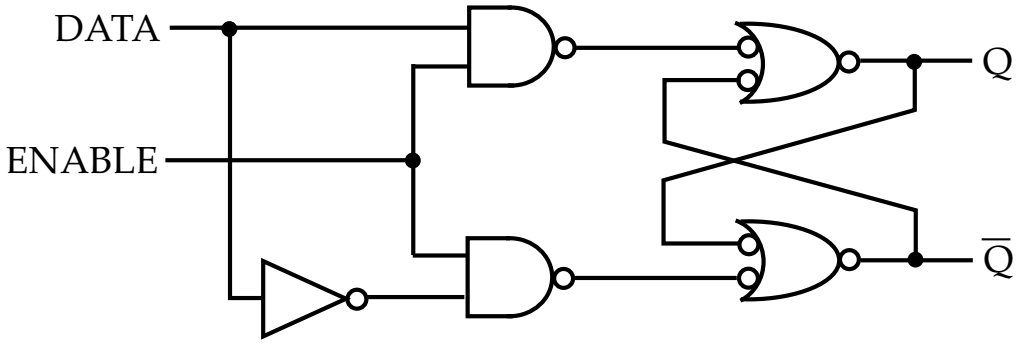


Figure 3.8: Schematic of a D-latch.

memories are called random access memories (RAM) as data can be randomly written or read as required.

Complimentary MOS inverters can be connected together to make up a static RAM (SRAM) cell for the storage of a single bit**. An SRAM cell will hold its state until a new bit of information is stored on it or an interruption in power is experienced. As will be seen in the sections below radiation induced effects can also cause the change the state of an SRAM cell. Static RAM cells are used for memories within systems and also provide the basic building block for circuits in programmable logic devices.

3.5 Programmable Logic Devices and Application Specific Integrated Circuits

It is not feasible to design complex circuitry at the transistor level as modern circuits often contain millions of transistors. Transistors can be combined to create slightly more complex circuit blocks, such as an SRAM cells and basic logic gates. These elemental blocks can then be combined in even higher levels of abstraction culminating in the broad class of devices called programmable logic devices (PLDs). A specific class of PLDs is capable of being programmed after they have been embedded in a system, using electronic signals from an external source. Two types of commonly used re-programmable PLDs are FPGAs and CPLDs.

A Xilinx FPGA works by using SRAM cells to define interconnect paths between an array of logic blocks and the circuits within these blocks, thus making up a functioning circuit (Figure 3.9). A block of RAM contains the configuration bits that define the circuit and the

appropriate logic [50, 51]. A CPLD contains a block of SRAM cells defining the interconnects, as in the case of an FPGA, but is made up of larger, more complex logic blocks (Figure 3.10). There are variations between both CPLDs and FPGAs manufactured by different companies, but the fundamental difference between the types of devices is the logic block complexity. The differences between CPLDs and FPGAs will be revisited when radiation effects on electronic devices are discussed.

Re-programmable logic devices offer the advantages that they are inexpensive, readily

**SRAM cells can also be made of NMOS and PMOS transistors.

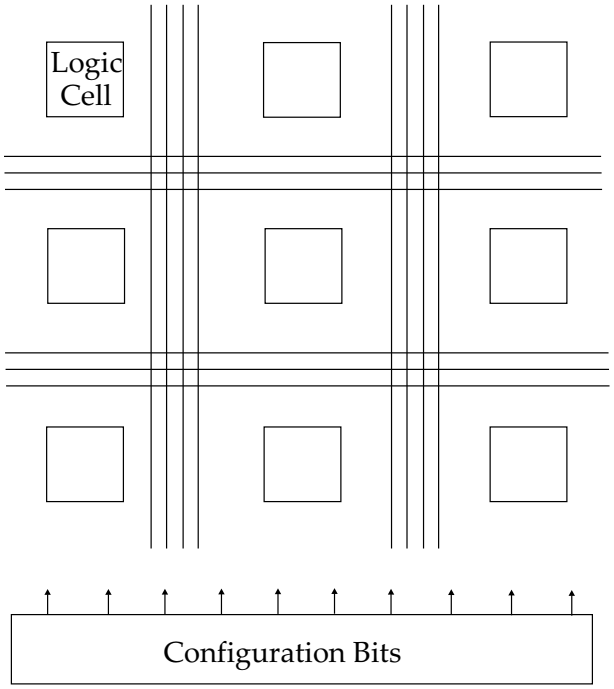


Figure 3.9: Schematic of a generic field programmable gate array (from Ref [51]).

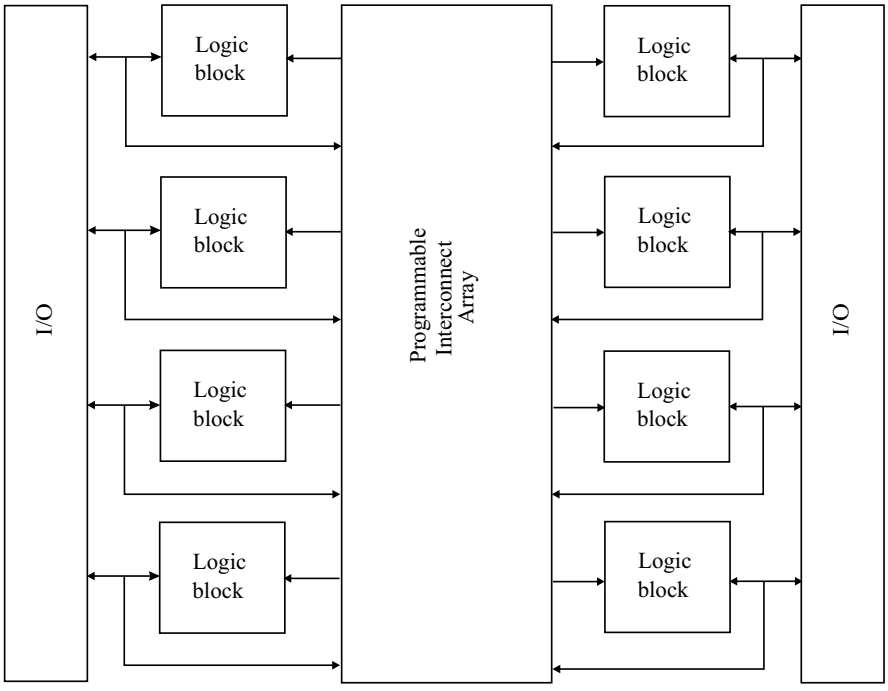


Figure 3.10: Schematic of a generic complex programmable logic device. (from Ref [52]).

available and can be reconfigured *in situ*. While they are suitable for most digital applications that will be encountered, they will not apply to all situations. Sometimes it may be necessary to realize a design too large or too complex or too fast for an FPGA or CPLD[††]. A more pressing concern may be that the device will be required to operate in locations, like those that could be encountered for military, space, or particle physics applications, where there can be extreme temperatures and high levels of radiation. One solution to these issues is the use of circuits that are manufactured specifically for the required application, or application specific integrated circuits (ASICs). Application specific integrated circuits have the advantage that the designer has more control over the design. These devices do not contain all of the additional circuitry required to program logic devices. The cost of an ASIC implementation of a circuit will tend to be higher than an FPGA or CPLD, at least initially, because of non-recurring engineering costs. In reality ASICs and re-programmable logic devices are typically both used during the design process. Re-programmable devices can be used to prototype the design prior to the commitment of producing the design in an ASIC. This prototyping process was used for the design of the SCAC device.

3.6 Effects of Ionizing Radiation on MOSFET-Based Devices

Total ionizing dose will cause cumulative degradation in MOSFET devices. Field effect transistors containing insulating oxides are, in general, susceptible to the effects of ionizing radiation. The reason is simply that that the oxide provides a medium in which superfluous charge caused by penetrating charged particles and photons can become trapped and lead to changes in device behaviour. In bipolar transistors ionizing radiation does not present such a potential problem as there are no insulating layers within them for charge to be trapped within. With the reduction in transistor size, and packing density, bipolar transistors will start to become more affected as oxides are used to separate transistors in devices [53].

The effects of ionizing radiation on a MOSFET are complicated and will be described

[††]This concern is becoming less of an issue. As of the time of this writing Xilinx Inc. has introduced the Virtex-II Pro^{TM} Platform FPGA that incorporates the functionality of a standard re-programmable logic device with the addition of up to 4 IBM PowerPC^{TM} microprocessors. Altera Inc. offers a similar product in the Excalibur^{TM} embedded processor.

in this section. It should also be mentioned that the nature and extent of TID-produced effects will depend on the temperature, bias voltage, device size, rate, and other variables. The effects of TID due to the gate oxide and field oxide (the oxide used to isolate the transistors from each other) are different. The TID effects due to the gate oxide will be examined first as they are easier to understand.

Control of the current available for conduction in a MOSFET is done using the gate-insulator-(semiconducting) channel part of the device. This is often referred to as the MOS capacitor. Reliable operation of a MOSFET requires stable behaviour of the MOS capacitor.

Some of the charge deposited into the oxide layer of the device may become trapped and contribute to changes in the net electric field that exists between the gate electrode and the silicon substrate. As the electrons are several orders of magnitude more mobile than the holes [54], they are quickly forced out of the oxide leaving the holes behind. The remaining holes then give the oxide a net positive charge. Over time the holes will drift in a complicated manner with a direction dictated by the fields, external and internal, within the oxide [55]. Some of the positive charge will become trapped in the bulk oxide and near the Si-SiO_2 interface.

The following example outlines the process for an n-channel MOSFET with a positive gate voltage (relative to the substrate). In Figure 3.11 the MOS capacitor portion of a MOSFET is shown. A sudden burst of ionizing radiation (from an electron accelerator for example) penetrates the device causing the production of many electron-hole pairs. During the short time that follows, on the order of picoseconds, initial recombination occurs reducing the number of electrons and holes free to move in the gate oxide. The electrons which remain after the initial recombination are more mobile than the holes produced and are accelerated toward the gate electrode and are collected there. Under the influence of the field produced between the gate and the device substrate, the holes drift toward the Si-SiO_2 interface, where they become trapped. This process can take days or even longer. Figure 3.12 shows how this could affect an n-channel enhancement mode MOSFET. After the process above occurs the charges trapped at the Si-SiO_2 interface shift the threshold (or inversion) voltage V_t more negative causing the device to become depletion mode. Some amount of current will flow through the channel with no gate voltage applied and

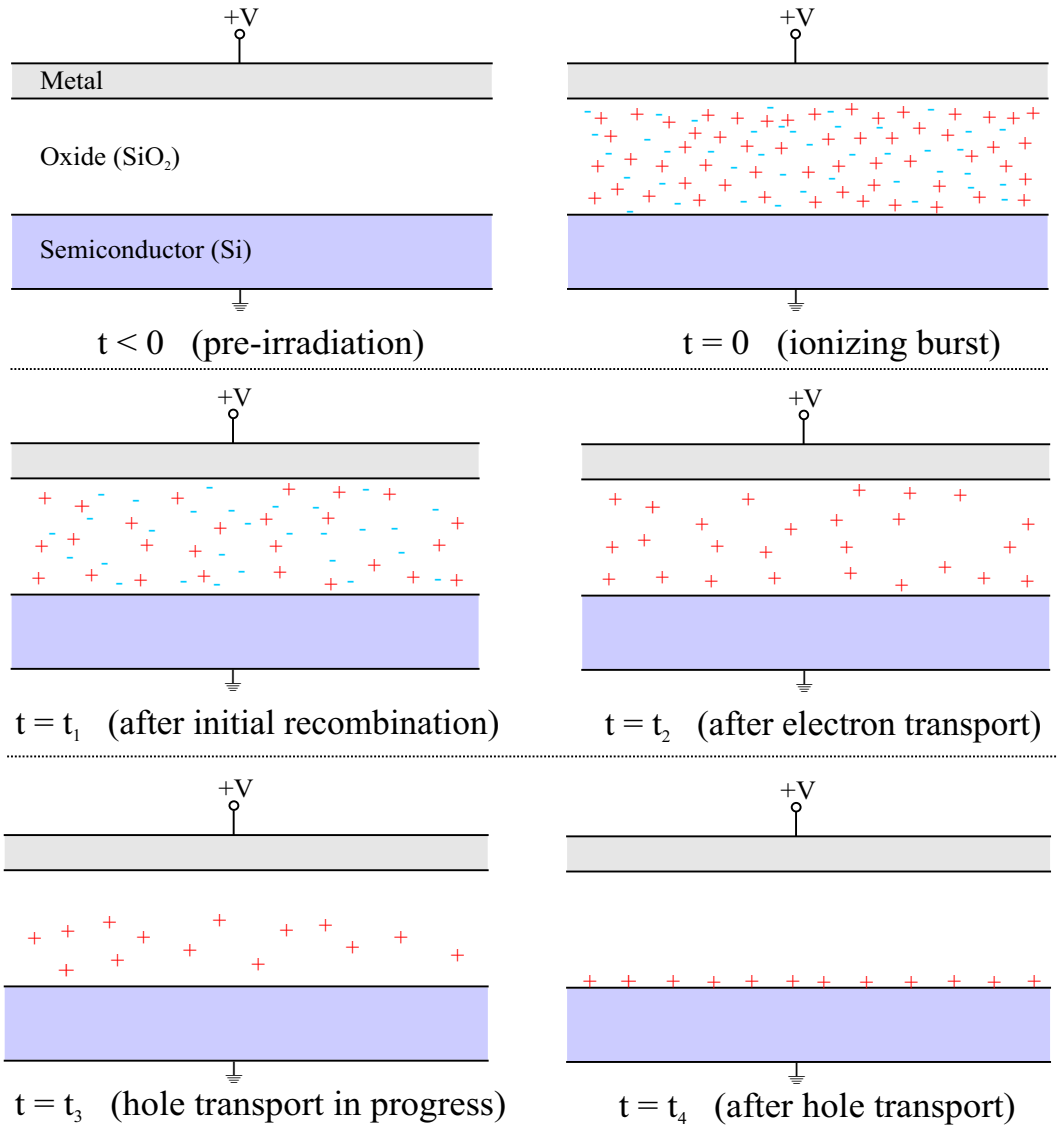


Figure 3.11: The process of charge transport in a MOS capacitor following a burst of ionizing radiation. See text for description (from Ref [53]).

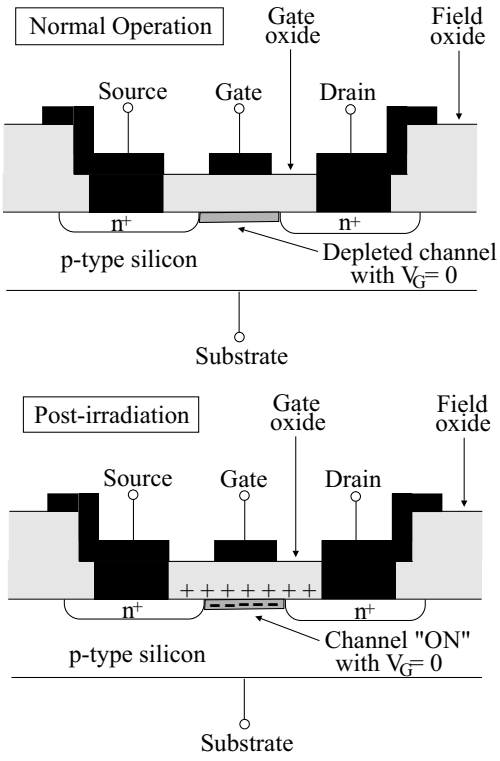


Figure 3.12: Effect of ionizing radiation on an n-channel enhancement mode MOSFET (from Ref [53]). The channel is depleted of majority carriers while the gate voltage is OFF. After absorption of TID trapped charges in SiO_2 start to cause the accumulation of majority carriers in the channel.

is seen as leakage current. One of the key features of the radiation damage process is the charge trapping near the Si-SiO_2 interface. This is illustrated in Figure 3.13. The trapping of charges at this interface is complicated and involves imperfections introduced during fabrication, as well as the chemistry of the oxygen bonds which are left unpaired at the SiO_2 surface boundary. This figure also shows that electrons present in the channel can tunnel into the oxide layer and recombine with holes, thus removing a part of the effect caused by the trapped charge. This will be discussed further in Chapter 4.

Another key factor in the amount of damage caused by ionizing radiation is that of recombination efficiency. If a charged particle, or photon, deposits energy such that the distance between electron-hole pairs is small there will be a large probability of recombination occurring. As the separation distance becomes larger the efficiency for recom-

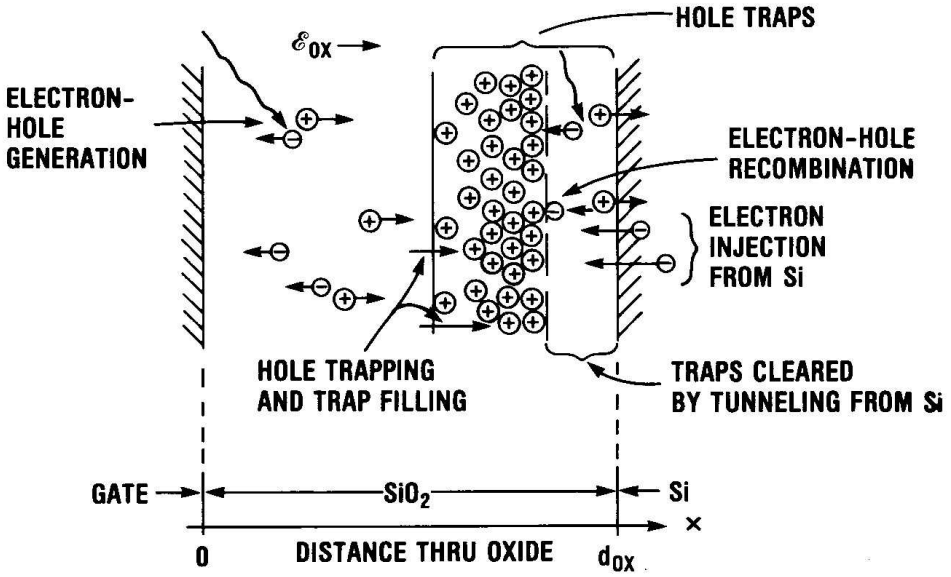


Figure 3.13: Schematic of hole trapping mechanism at a semiconductor-insulator interface (from Ref. [53]).

bination decreases. Figure 3.14 show plots of the recombination efficiency versus gate substrate field strength for a variety of particles. The type of ionizing radiation is not only a concern when considering device operation in a particular radiation environment; it is also a serious concern when choosing irradiation sources and facilities that can best represent the degree of TID damage that will be caused by the real radiation environment.

The charge trapping occurs at the Si-SiO_2 interface and will affect n-channel and p-channel devices differently. In n-channel MOSFETs the interface traps compensate for the positive charge trapped in the bulk oxide and cause V_{th} to shift to larger voltages. The reason for this is complicated and believed to be related to the interaction of holes with hydrogen contained in the layers near the interface [56]. Figure 3.15 shows that the interface effect will dominate at higher doses, which will eventually cause the device to turn OFF. The increase in V_{th} above the value prior to irradiation is called "super recovery" [57]. No such effect occurs for p-channel MOSFETs (Figure 3.15) as holes are transported away from the interface.

The dose rate of the applied radiation has an effect on the degree of damage a device

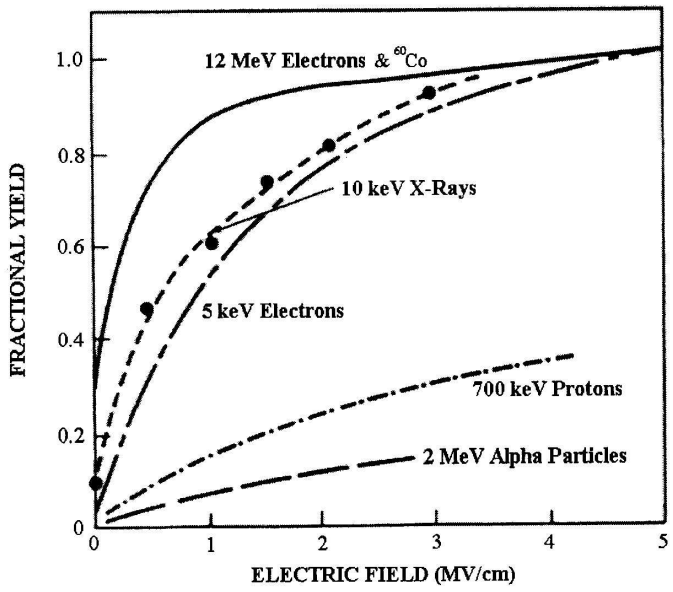


Figure 3.14: Fraction of hole electron pairs which do not recombine in SiO_2 (from Ref. [53]).

will suffer. It has been found that the number of charge traps near the Si-SiO_2 interface increases with lower dose rates [58]. This is because the recombination rate of the holes within the oxide will be comparable, or greater, than the accumulation of interface traps. The net effect of the low dose rate is that the NMOS threshold voltage will not decrease, but rather begin to increase toward the OFF state.

The previous discussion was used to give an understandable description of the effects of TID on MOSFET devices, but it does not fully describe the situation where many transistors are situated in relatively close proximity, as would be the case with CMOS devices. In recent microelectronic devices the gate oxide can be as much as 30 times thinner than the field oxide that exists between the individual transistors [53]. As the gate oxide becomes thinner there will be less charge trapped in it and thus the effect on the device due to the gate oxide will be reduced.

The geometry of the transistors becomes important as leakage current can flow between the source and drain in a transistor. This is depicted for an n-channel MOSFET in Figure 3.16. Positive charge becomes trapped in the thick field oxide and draws negative charge to the edges of the transistor which lead to leakage currents between the source

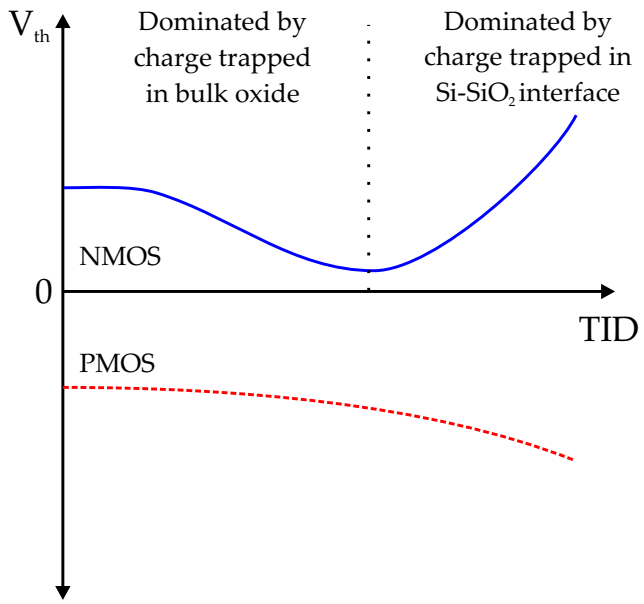


Figure 3.15: The shifts in V_{th} caused by TID for n-channel and p-channel MOSFETS.

and drain. This effect is only of concern for NMOS transistors as negative charge will not be trapped in the same manner in the field oxide. Leakage can occur between the source and drain of a single transistor or between neighbouring transistors [58, 59].

While these effects are reasonably well understood at the transistor level and physically interesting, detailed comparisons between the effects observed during this work and the models describing the effects in this section can only be inferred. The reason for this is that this thesis describes the effects of radiation on relatively large systems comprised of several millions of transistors. Any effects resulting from photon, or charged particle, irradiation will show up as an overall effect.

Xilinx and Altera programmable logic devices, such as FPGAs and CPLDs are dominated by CMOS-based SRAM switches, where the transistors are generally in static mode (i.e. not in the process of changing states). The effect of radiation on the leakage current is therefore of significant interest. As the radiation begins to induce leakage currents in the NMOS transistors there will be a sharp rise in the power supply current drawn by the device. This increase will then slow as the interface traps begin to dominate and V_{th} begins to shift in the positive direction. The device will eventually fail as super recovery

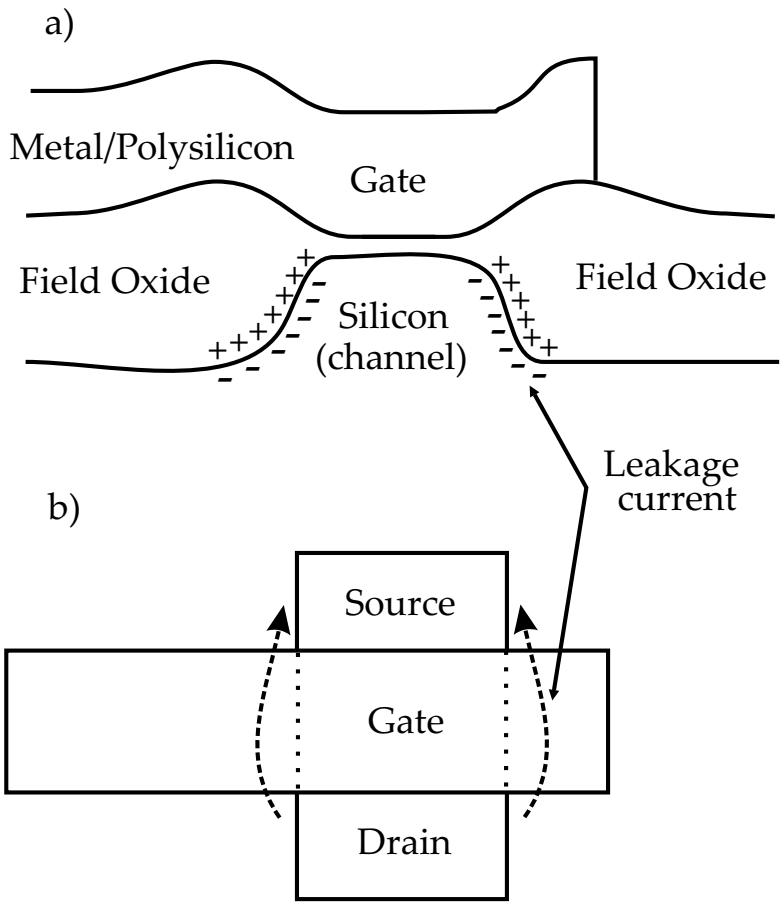


Figure 3.16: Leakage current between source and drain in an NMOS transistor. The cross-sectional view down the channel (a) shows trapped charge in the field oxide and the region of charges available for leakage current. The top down view (b) shows the resulting current between the source and drain (from Ref. [60]).

begins to turn off the NMOS transistors [58].

3.7 Single-Event Effects on MOSFETs

An SEE is a disturbance to an electronic device caused by the passage of a single particle, or pulse of radiation. Single-event effects can be grouped into three general categories, soft effects, hard effects, and effects that permanently damage the device. Within each category there are further differences between the radiation effects that can disrupt an electronic system. These differences can depend on the type of radiation, the device design, and the process used when the device was fabricated.

3.7.1 Transient and Hard Single-Event Effects

Charged particles will deposit charge when passing through a material and that charge, if it occurs near a transistor that has a bias applied to it (an active element) can be collected into the active element and cause a change of state of the primitive circuit containing the element. A cell in an SRAM, for example, can have its state changed from a stored LOW bit to a stored HIGH bit, or vice versa. This process is referred to as a single-event upset (SEU).

Figure 3.17 shows the basic SEU process due to an ion strike. An ion penetrates the device near a sensitive circuit node, depositing energy that is converted to electron-hole pairs within the silicon. Some of the charge deposited will diffuse through the substrate, a small portion of which will be collected on a node. A much larger amount of charge will be "funneled" onto the node, if it is close to the ion strike. Charge funneling is driven by the distortion of the field lines within the device caused by the passage of the ion. Depending on the terminal-substrate voltage, electrons or holes will be forced toward the active node. If sufficient charge is collected, the critical charge, the device will experience a spurious pulse, which can affect the operation of the circuit containing the device [61, 62, 63, 64]. The sensitivity of the device to SEUs depends on the characteristics of the incident radiation, as well as on the characteristics of the nodes within the device itself. The ionization state and energy of an ion traversing, or passing near, a sensitive node in an

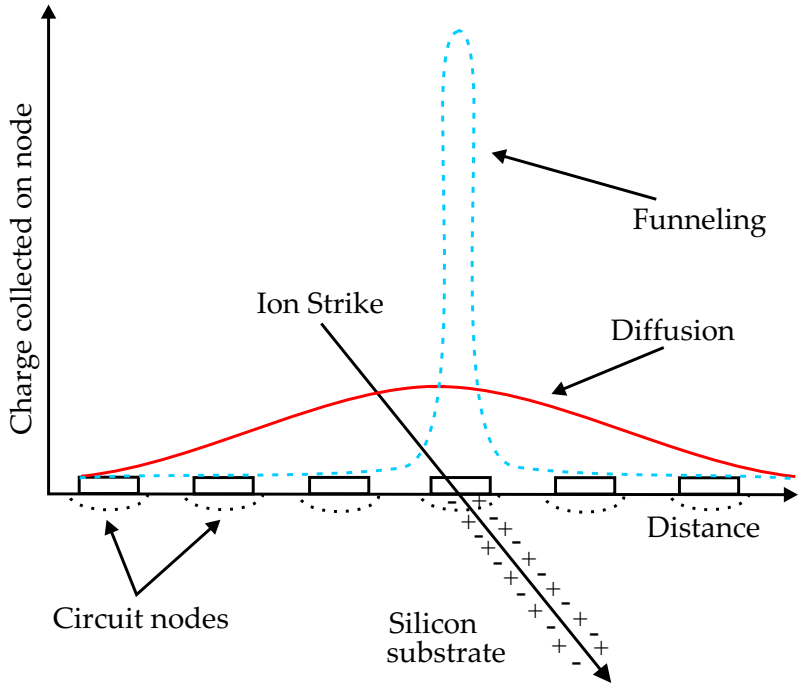


Figure 3.17: Charge collection within an electronic device plotted as a function of location, following an ion strike. The contributions due to diffusion and charge funneling are shown (based on Ref. [62])

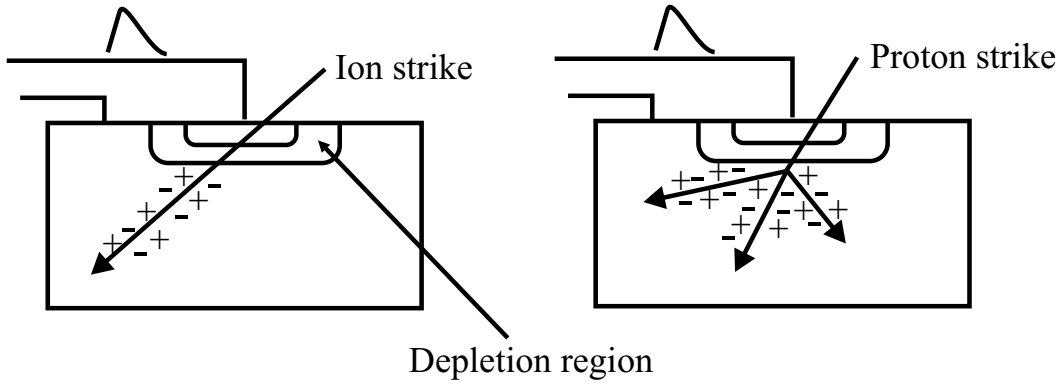


Figure 3.18: Process of charge generation for heavy ion and proton incident on a FET node. The heavy ion produces sufficient charge by direct ionization to cause an upset while the proton will tend to initiate a nuclear reaction to produce sufficient charge.

electronic device will largely determine whether an SEU will occur or not (equation 3.1). If an ion stops near a node the situation is enhanced due to the fact that the vast majority of the particle's energy will be deposited near to its stopping location (see Figure 3.3). A high energy muon or proton will deposit much less energy, due to ionization, than an alpha particle with the same energy (Figure 3.18) due to the difference in dE/dx. Heavy ions will tend to deposit sufficient energy that, once converted to charge, can cause an SEU in most modern devices [65][‡‡]. Protons on the other hand will generally cause less ionization and not cause SEUs directly. Protons will initiate SEUs in the same way that neutrons will, via the products of nuclear interactions between the incident particles and the host material – usually silicon.

The SEUs described above will in many cases be transient and only affect the circuit temporarily before they are cleared. For example, such an SEU in an SRAM cell will be cleared the next time the cell is written to. It is also possible for an SEU to occur in combinational logic. An SEU occurring in combinational logic may propagate through the circuitry and could cause spurious errors. If, however, an SEU were to occur in a transistor within the switch matrix of an FPGA, the situation would not be transient. A reconfiguration of the device would be required in order that the device would return

[‡‡]Modern devices refer to those devices where the smallest lithographic feature (often referred to as the feature size) is less than 1 μm in dimension. These are referred to as sub-micron devices, while a subclass of devices, deep sub-micron, have feature sizes less than 0.5 μm .

to normal operation. Upsets of this type are referred to as hard SEUs and require some intervention to return the system back to an operating state.

Unlike TID effects soft and hard SEEs do not appear as permanent system degradation, such as increased power supply current drawn by the device. An SEU might appear as an unexpected change in a bit stored in a RAM for example. A common technique used to observe SEUs in memory cells is to write a pattern to a block of memory, irradiate the block, and then read back the contents of the memory. An SEU will correspond to a change in a bit within the pattern. If an SEU occurs in combinational logic it may propagate to a vital part of the circuit and cause errors in the circuit behaviour, or it may propagate to a state machine that is not active and not be detected at all [66].

The probability of a proton-induced SEU occurring, or the proton-induced SEU cross-section (having units of area), can be measured once a method for observing SEUs has been devised. One such method used for the research described in this thesis was to continuously cycle a set of sequential numbers through a FIFO and watch for the numbers to go out of sequence. Two important parameters obtained from induced SEU cross-section data can be used to quantify SEE effects, which is important when radiation qualifying a device. The threshold energy (Figure 3.19) is the proton energy at which the cross-section sharply increases to its maximum value. It is defined as the energy that the SEU cross-section is at 50% of its maximum value. The maximum value of the SEU cross-section is referred to as the saturation cross-section and is the value of the cross-section for protons of infinite energy. The shape of the proton-induced SEU cross-section in Figure 3.19 can be best understood by considering the active elements within the device. An active cell will upset if a critical amount of charge is collected into it. If the nuclear fragments coming from a proton-^{28}Si collision do not deposit sufficient charge to cause an upset the value of the cross-section will be zero. Once the proton energy is sufficient to scatter nuclear fragments through active elements within the device upsets will begin to occur. Once the proton energy is such that the fragments from proton-^{28}Si interactions are sufficient to cause the deposition of the critical charge within active cells in the device, the cross-section will rapidly reach a maximum. The threshold energy is generally a function of the device sensitivity to SEUs.

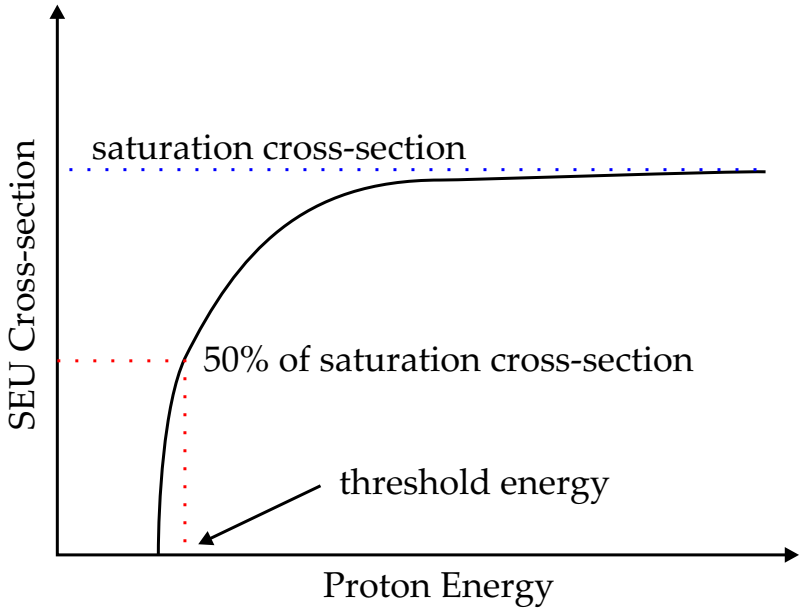


Figure 3.19: Sketch of a generic proton-induced SEU cross-section showing the threshold energy and saturation cross-section.

3.7.2 Damaging Single-Event Effects

Permanent damage can also be inflicted upon MOSFETs by energetic particles. The most common effect of this type is called single-event latch-up (SEL). Single-event latch-up can occur in CMOS circuitry if the device is not designed to avoid such effects. Figure 3.20 shows an equivalent circuit for a latch-up condition in a CMOS inverter. In Figure 3.20 the negatively doped substrate and positively doped well provide the base for two parasitic bipolar devices. The highly doped p^+ and n^+ regions complete the NPN and PNP circuits where the base of one shares the collector of the other. The result is that a low impedance path from V_{CC} to ground forms a latch-up condition [67, 68, 65]. If latch-up occurs, the effect is analogous to a short to ground within the device. Such an effect would cause a sudden increase in the drawn power-supply current. The power to the device would need to be cycled to clear the condition, but permanent thermal damage might result regardless. There are other destructive SEEs that can cause permanent damage as well, such as single-event gate rupture (SEGR) and burn-out. These types of damaging effects are typically associated with power MOSFETs but will likely become an issue for low power MOSFETS

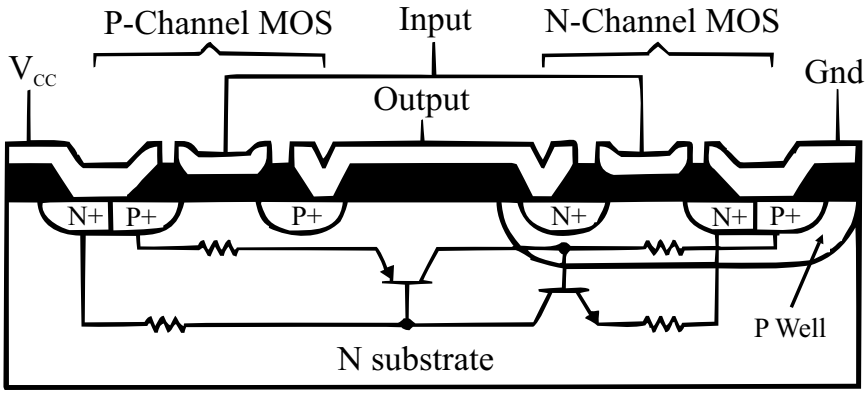


Figure 3.20: Diagram of the equivalent circuit for a latch-up event occurring in a CMOS inverter (from Ref. [67]).

as the device size decreases and packing density increases [69, 70]. The devices tested during the work described in this thesis were not of a type where permanent SEEs, other than SEL, should become an issue.

3.8 Displacement Damage

Displacement damage occurs when collisions between incident ions and lattice ions cause the relocation of the scattered lattice ions within the bulk medium [71, 72, 73]. As illustrated in Figure 3.21 the potential wells and barriers within the lattice will cause the scattered lattice ions to become located interstitially (between the regular lattice sites) within the lattice. Interstitial positions can become deep trapping centers and in turn affect the carriers and their mobility within the material. The effect is most noticible when the minority carriers are examined as their concentration is relatively close to the displacement concentration. These effects are a serious concern for bipolar transistors where the base control depends on minority carriers. As MOSFET devices rely solely on majority carriers displacement damage does not become a concern until the number of displacements approaches the number of majority carriers. Displacement damage would cause a reduction in carrier lifetime within the conducting channel, which would change the impedance of

the channel. This could lead to changes in device timing and the distortion of signals passing through the channel. Displacement damage in MOS devices should not be a concern at the LHC but a study was performed on one of the prototype devices examined to ensure that this was the case.

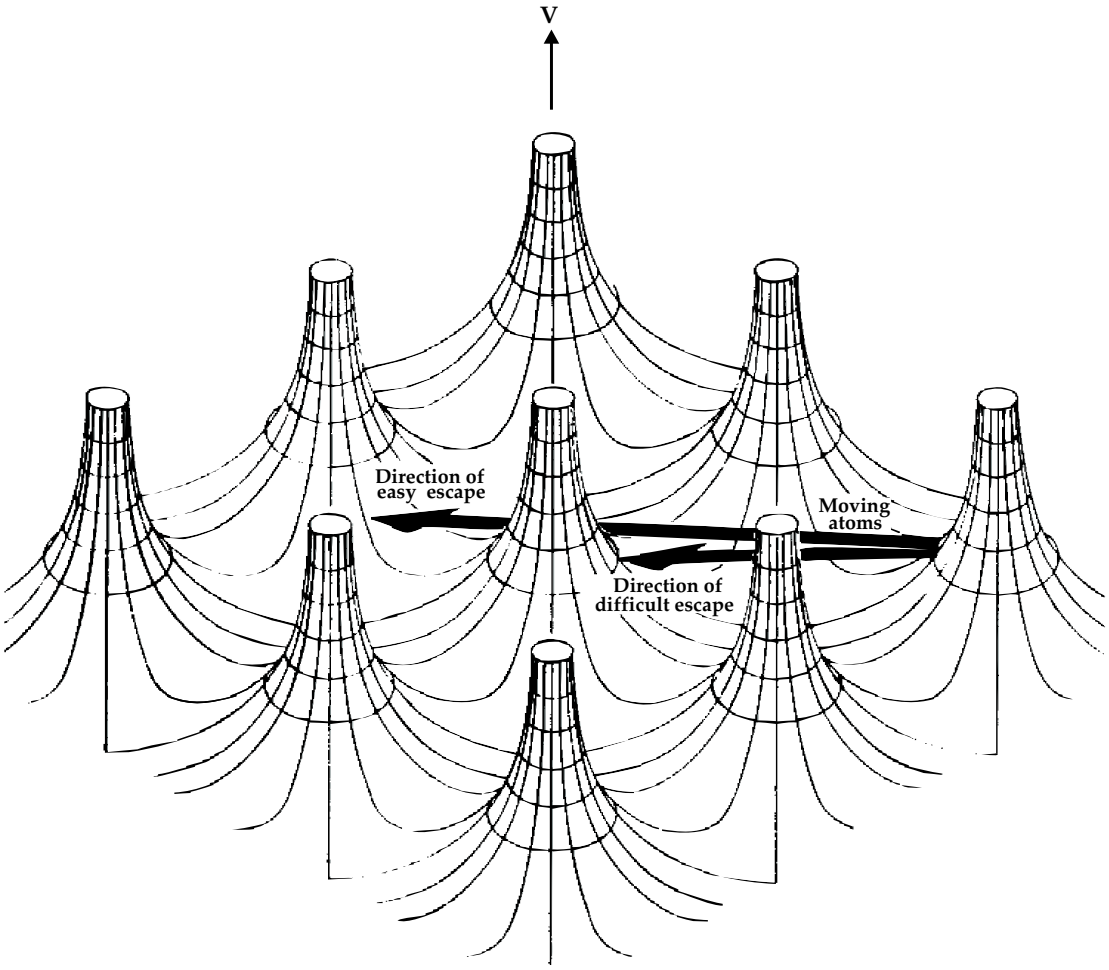


Figure 3.21: Cartoon of atomic displacement process. The surface corresponds to the potential barriers and wells existing within the lattice. A scattered atom will most likely become located between atoms of the lattice (from Ref. [74]).

Chapter 4

Radiation Hardness and Tolerance

4.1 Introduction

Since the 1960s there has been a need to operate electronics in areas where radiation could not be avoided, such as those near nuclear reactors, nuclear weapon test sites, and space. It became clear that steps would need to be taken to find methods and designs that permit electronic devices to operate in such environments [75, 76]. The particular approach so taken to ensure that a device or circuit is "radiation tolerant" depends on a number factors such as the type of radiation field that will be encountered and the operation specifications of the device or circuit. This chapter outlines some of the "radiation hardening" approaches that can be taken, with emphasis placed on techniques employed in the design of the radiation hardened DMILL and deep sub-micron SCAC prototypes.

4.2 Device Hardening Techniques

There is a wide variety of radiation hardening techniques which vary greatly in their level of sophistication. Perhaps the simplest and most obvious technique is shielding. To avoid the effects of most radiation a material (preferably consisting of high-Z elements) can be placed between the radiation source and the sensitive system* [77]. This approach becomes less useful when, as in the case of a particle physics experiment, the shielding material becomes a source of energy absorption and further radioactivity, or in the case of

*Neutrons can be shielded in a similar manner with the use of low-Z materials.

space missions when the shielding material becomes too heavy or cumbersome to transport.

4.2.1 Process Control

First and foremost, with all other things being equal, it is extremely important to ensure that the materials used in device fabrication are as pure as possible [78, 79]. While the use of impurities as dopants is required in the semiconductor material, such impurities can reduce the radiation hardness of a device if they are present in the oxide. Impurities can act as trapping centers for holes moving through the oxide. This is especially true near the Si-SiO_2 interface where a trapping environment already exists due to the unmatched bonds there. In bipolar technologies process control is especially important as reduction of minority carriers will adversely affect the device operation.

4.2.2 Device Scaling

Device scaling is one of the most common methods used to harden a device against the effects of ionizing radiation. Electrons will tunnel into the SiO_2 from the semiconductor channel and combine with holes near the interface (Figure 3.13). This process will clear charge trapping sites near the Si-SiO_2 interface. As the SiO_2 layer becomes thinner it will eventually approach the tunneling distance (a few nm) of electrons into the material. The benefit of increased TID hardness of the MOS capacitor has to be considered against the adverse effect of increased leakage current across the field oxide that separates transistors. This problem has been observed when the local isolation (LOCOS) fabrication process is used. The oxide deposition for this method is such that the oxide layer begins to diffuse into the region between the transistors allowing charge buildup and increased leakage current. Fabrication processes have been developed to counter this problem [80].

Scaling has led to VLSI (very large scale integration) devices that employ a variety of techniques that enable their manufacture, such as epitaxial substrates[†] which help to alleviate potential SEL conditions [59]. A price must be paid as scale reduction can make

[†]Substrates are traditionally bulk silicon wafers whereas epitaxial substrates are "grown" or deposited. They are thus much thinner.

devices more susceptible to SEUs or even introduce single-event gate rupture as a concern. The deep sub-micron prototype utilizes this technique.

4.2.3 Edgeless Transistors and Guard Rings

Current leakage can occur due to fields induced by charges trapped in the field oxides within a MOSFET device, as was described in Section 3.6. The parasitic path between the source and drain can be eliminated to a large degree using a particular layout geometry (Figure 4.1). These novel transistors are called edgeless transistors (they are also referred to in the literature as enclosed layout transistors). The relationship between the width and length of the conducting channel greatly influence the source to drain leakage current. Simulations and measurements have shown that the edgeless transistors shown in Figure 4.1 reduce the leakage currents, as compared with a "standard design" [60]. A disadvantage of the use of enclosed transistors is that they take up more space than "standard transistors". Transistors of this type were utilized in the the deep sub-micron device.

Edgeless transistors work well to reduce the source to drain leakage current within the transistor but do not address the issue of leakage current between devices. Guard rings are used to reduce the inter-transistor leakage currents. They are rings of semiconducting material that surround the the device channels. N-type channels are surrounded with p-type guard rings and p-type channels are surrounded by n-type material. The guard rings work by cutting off possible parasitic paths between transistors [59].

4.2.4 Substrate on Insulator Transistors

The problem of SEUs has not been addressed in the previous sections examining radiation hardening techniques. If the thick semiconductor substrate is replaced with a smaller substrate that sits on top of a thick insulating layer a degree of hardness against SEEs can be achieved. This solution is called substrate on insulator, or SOI, design and works by preventing the charge generated during an ion strike from collecting back onto a sensitive node. The charge track is mostly contained inside the insulator and the long plasma trail that exists in the semiconducting substrate of traditional designs is no longer present to

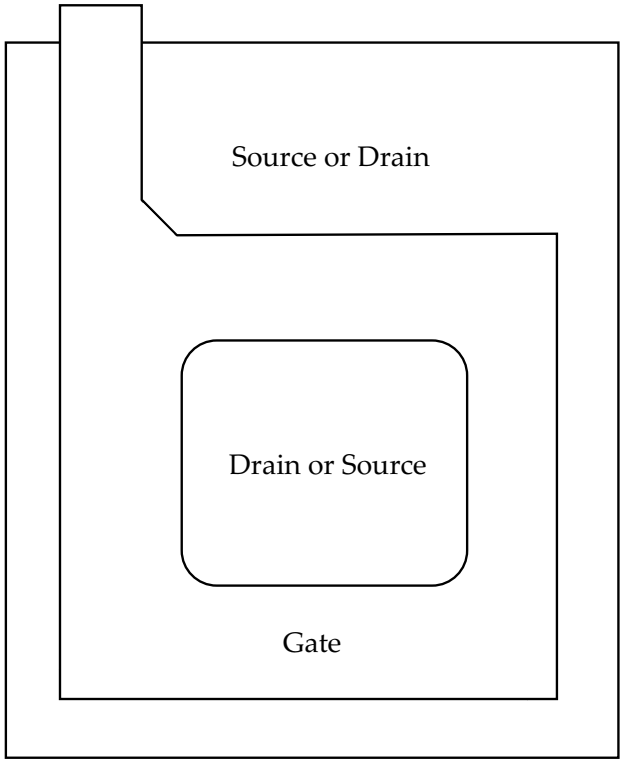


Figure 4.1: Schematic of the enclosed transistor design described in Ref. [60].

the same degree. Additional approaches to alleviating the problem of SEUs are outlined in the following section on circuit design use in the mitigation of radiation effects.

4.3 Impact of Circuit Design on Radiation Tolerance

While it is clear that the primary reasons for device failure in the presence of radiation pertain to the device type, design, and fabrication, some situations arise where the design at the circuit level can have an impact as well. This is the case when SEEs or transient effects are the predominant source of system failures or instabilities. A good example of this concept is described in Ref [81]. In this example a simple portion of an electronic design is examined (Figure 4.2a and b). Both circuits perform the same task with the circuit in Figure 4.2b being optimized for speed. With the increase in speed comes an additional state variable and thus it could be possible for both outputs in the optimized version to be high (or low) causing unknown problems in the circuit. In most circumstances this example would not present a concern for designers, but it is conceivable that an external factor, such as an SEU causing particle, could alter the state of a D flip-flop. Details such as this need to be considered.

Conversely it is the case that circuit design can be used to aid in safeguarding a circuit against radiation induced disruptions. Certainly an examination of the specifics of a circuit design can prevent situations such as that discussed above. This can be time consuming and in fact impractical with the size of modern VLSI circuits. This problem can be overcome with the use of hardware description languages (HDLs), such as VHDL, and libraries meant for use in radiation tolerant circuit design. One such library is the `cmos6sf25` standard cell library developed at CERN (see Ref [82] for example). A particular example of a design hardening object that may be contained in a radiation tolerant design library is an SRAM memory cell that utilizes feedback resistors [83, 58]. This cell is shown in Figure 4.3. The cell is made up of 6 transistors: 4 for the two inverters and 2 N-FETs for the pass gates, and two resistors. The resistors act to delay the passage of incorrect data resulting from an ion strike allowing the cell to stabilize to its original state. This technique has the unfortunate side-effect of reducing the speed performance of the SRAM cell.

In addition to circuit layout optimization, other mitigation techniques can be em-

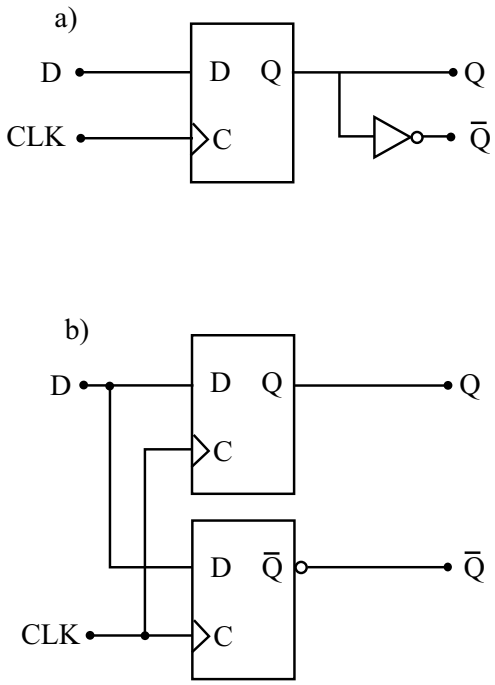


Figure 4.2: Circuit illustrating the effect of circuit design on radiation hardness assurance. The circuits in a) and b) will perform the same task with the circuit in b) being optimized for speed.

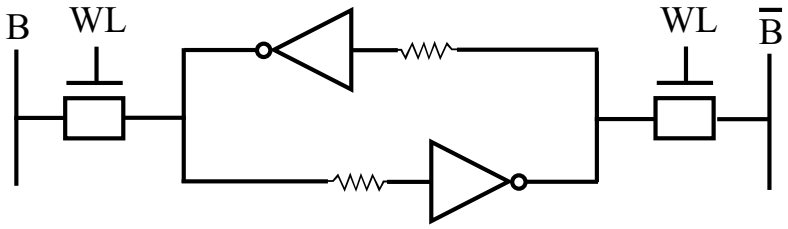


Figure 4.3: A radiation hardened SRAM cell utilizing feedback resistors.

ployed at the circuit design level (see Ref. [84] for example). These techniques are referred to as error detection and correction, or EDAC. One common and effective EDAC technique that can be employed is redundancy, specifically triple redundancy. Any important and/or SEU sensitive parts of a circuit can be layed out in triplicate and a comparison can be performed at a stage beyond the point of concern where any disrupted bits can be corrected. This technique is most effective when the probability of multiple bits being simultaneously affected is low, i.e. the combination of radiation levels (SEU capable particle flux) and device node sensitivity are within certain limits. The concern of multiple-bit upsets can be addressed by ensuring sufficient spatial separation between each of the three circuit copies. The use of parity bits is another safeguard against corrupted data that might come from radiation induced effects. A parity bit is an additional bit added to a digital word that has a value corresponding to whether there is an even or odd number of 1s in the word. A generalization of the use of parity bits are codes called Hamming codes. An n-bit digital word containing a Hamming code will have every 2^nth bit used as a parity bit, thus breaking down the data into subsets of information. The details of these codes are beyond the scope of this thesis but details can be found in Refs [85, 65].

Design modification can be an effective method to safeguard against non-destructive SEEs, but it comes at a cost. The use of specialized radiation tolerant libraries will tend to drive up the cost of design and can make precise timing and other optimizations difficult. The use of other mitigation techniques also come at a cost, where additional circuitry is required to allow parity bits and comparison logic, all of which may also be susceptible to radiation effects. In reality a combination of process hardening and mitigation techniques will be used in developing a circuit for use in a radiation environment. The deep sub-micron device ultimately chosen for the final design of the SCAC described in this thesis utilized all of the techniques described in this chapter with the exception of SOI fabrication. The DMILL SCAC prototype utilized all of the device hardening techniques described here, with the exception EDAC and triple redundancy, as well as additional proprietary device hardening techniques. A design library specific to the DMILL technology was used for the circuit design but no additional SEU mitigation techniques were included in the DMILL design. The reason for the lack of SEU mitigation was the large die size, cost, and speed. No SEU mitigation techniques were employed in any of the FPGA

or CPLD devices.

Circuit level design can be used to protect against SEU errors, but system level design can also be used. System level SEU mitigation corresponds to protection that occurs outside of the device. An example of system level mitigation would be the use of three identical devices performing the same task and having their outputs compared prior to being used. The RODs in the ATLAS LAr readout system will compare the addresses coming from the two SCACs on each FEB. Any SEUs that are not corrected in EDAC circuits within the device would be detected at the system level.

Chapter 5

Irradiation Facilities

5.1 Introduction

An integral part of the radiation tolerance test procedure is the choice of irradiation facility. The facility must be able to provide a radiation environment that reasonably approximates that where the device will reside. In addition it is important for a test facility to provide accurately measured and reproducible radiation levels. Four such facilities were used for the radiation tolerance testing of the SCAC prototypes and three of them are described in this chapter.

5.2 Cobalt Irradiation Cave

The photon irradiation performed on one of the re-programmable SCAC prototypes was done in an open room ^{60}Co irradiation facility. Cobalt-60 is a source of mono-energetic* photons and has a half-life of 5.27 years. The test facility is located behind a chemistry laboratory in the basement of the chemistry building at the University of Alberta. The activity of the ^{60}Co source was determined to be about 52 Ci (Appendix C describes radi-

*There are actually two energies, 1.33 MeV and 1.17 MeV, associated with ^{60}Co decays but there is no loss of generality by assuming an average photon energy of 1.25 MeV, since the two decay rates are equal.

ation related units, such as the Ci) at the time of the tests described in this thesis.

The ^{60}Co facility is illustrated in Figure 5.1 and enables open room irradiations making it a perfect choice for testing large devices. The main irradiation chamber is an open space approximately 1.5×1.5 m^2 with a 3 m ceiling. The chamber is connected by a 3 m open walkway that is slightly less than 1 m in width. Between the walkway and an outer control room, which is protected by concrete shielding, is a 0.5 cm thick steel door. Inside the steel door is an interlock door made of steel grating to prevent entry into the irradiation area during exposure of the source. Two mirrors are mounted at each end of the concrete walkway to allow experimenters to view the source area and ensure that the source is not out prior to entering the area. The control room is separated from the source by 1 m of concrete. A radiation survey meter was used to confirm that the radiation levels in the control room were not above background in the same building. The control room contains a source injection rod, key locks for the source, and all of the mechanisms for the interlock control. A large steel sliding door sits between the radiation facility and the chemistry laboratory it is located behind. The door is padlocked to prevent unauthorized entry.

The source is attached to the end of the injection rod, which protrudes in to the control room. It is housed by a large steel tank when not being used (Figure 5.2) with a lead block moved in front of the hole that the source emerges from. This is an added precaution to reduce the radiation levels in the cave when experimenters must enter.

When the source is pushed into the test area it is slid along a flat rail. At full insertion the source sits at the midpoint of the rail. Any devices can then be aligned with the source, which is roughly the size and shape of a small piece of chalk. For the irradiation tests described in this thesis, a lead enclosure was built using lead blocks of dimension 5 cm by 10 cm by 15 cm to protect the other components on the board and reduce the amount of backscattered radiation near the device being tested. The enclosure is 56 cm in width, 46 cm in depth, and 55 cm in height. It can be seen in the vicinity of the source containment tank in Figure 5.3. An aluminum box was placed inside of the lead enclosure. The box was used to reduce the low energy photons coming from interactions between the primary photons and the surrounding lead.

Fricke radio-chemical dosimetry was used during all of the gamma irradiations done in the ^{60}Co facility. This technique is described in Ref. [86].

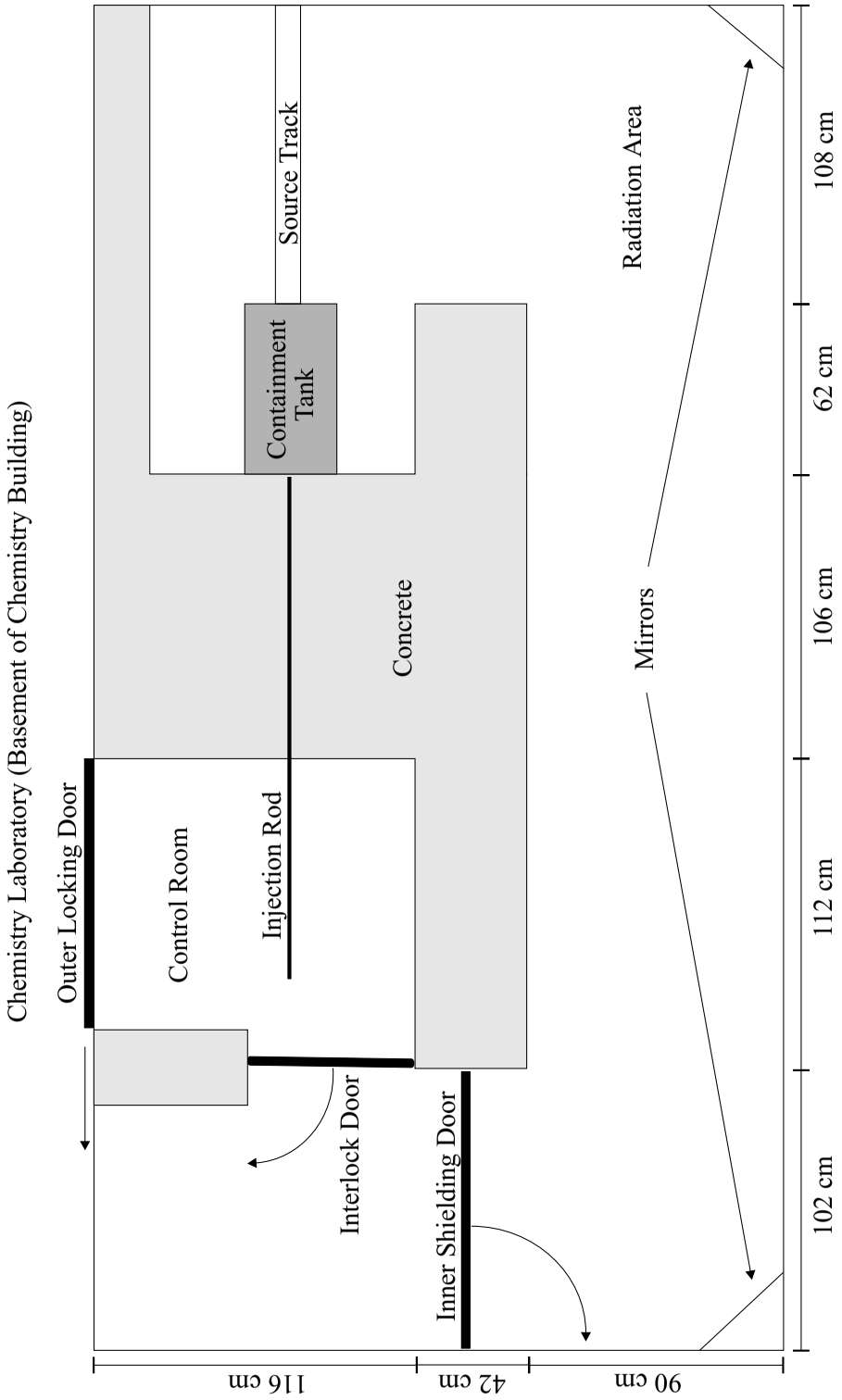


Figure 5.1: Overhead view of ^{60}Co irradiation facility. The illustration shows the source containment tank (dark grey), concrete shielding (light grey), the test area, and control room.

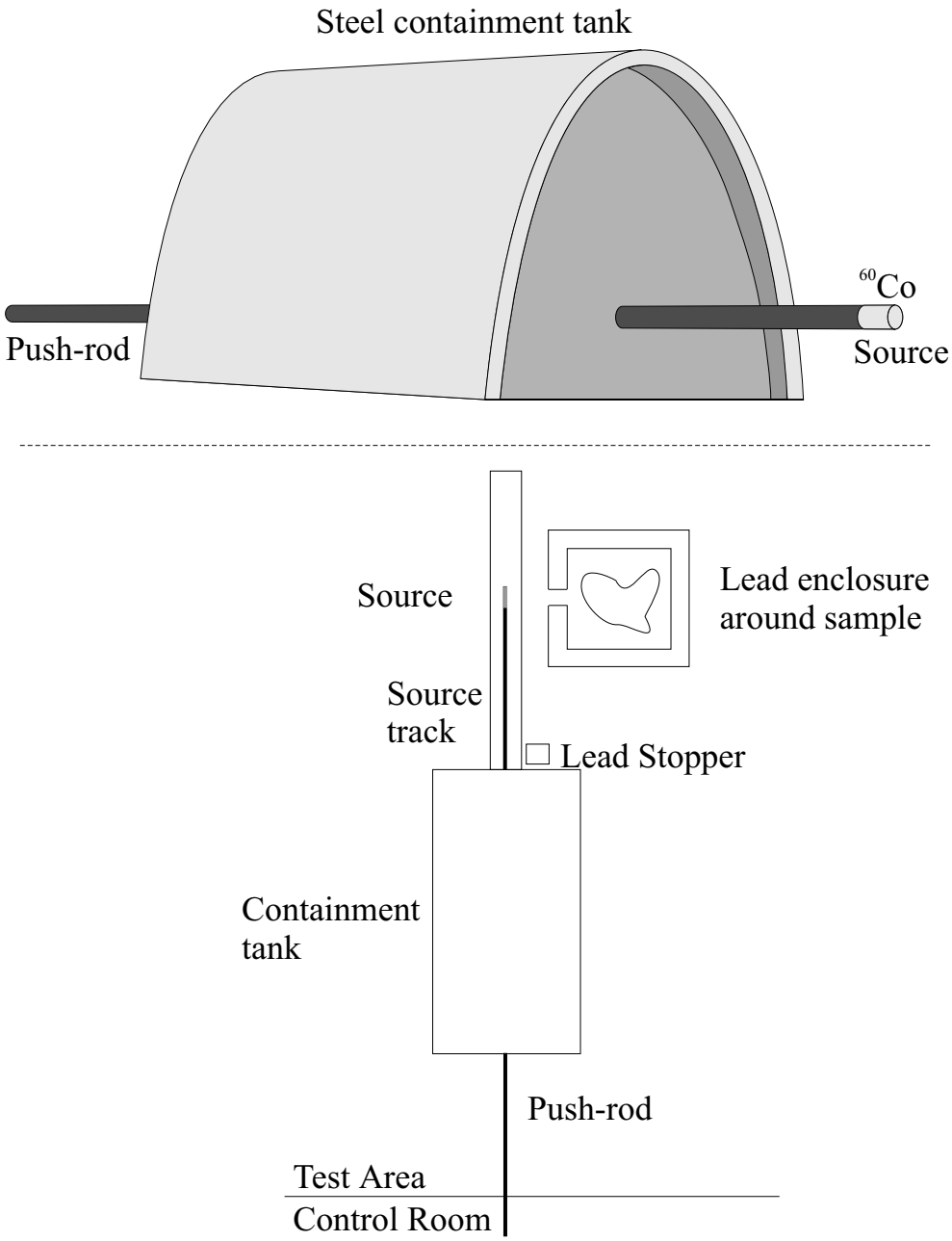


Figure 5.2: Side view and top view of the steel containment tank used to house the ^{60}Co source.

Figure 5.3: Photograph of ^{60}Co facility showing the containment tank on the left and the lead sample enclosure on the right.

Figure 5.4: Photograph of the x-ray housing showing the high voltage cables, coolant hoses, port window, and test table.

5.3 X-Ray Accelerator Facility

The x-ray accelerator laboratory was built and used for the majority of the TID tests performed and is located in the basement of the Centre for Subatomic Research (CSR), at the University of Alberta. The device is an industrial constant potential x-ray generator capable of producing electrons with energies between 50 keV and 320 keV. Figure 5.4 shows the x-ray tube situated in the test room. The device can be operated using two focus settings. These settings determine the geometry of the x-ray beam. Both settings give a downward diverging cone emanating from the x-ray port window. The large focus gives a cone of

larger diameter and allows larger beam currents to be used. The maximum beam current which can be achieved, on the large focus setting at 320 kV_P (peak amplitude kilo-voltage) is approximately 10 mA.

The x-ray machine is controlled by an electronic control system which is located outside of the shielded x-ray test room. In order to ensure that the radiation level near the x-ray facility was within safety standards, the tube was placed within a large shielding box (Figure 5.5) made of 2 cm thick plywood sandwiched between a 0.3 cm thick steel skin. Between the inner shielded box and the door leading to the x-ray control system was a solid concrete block wall 41 cm thick.

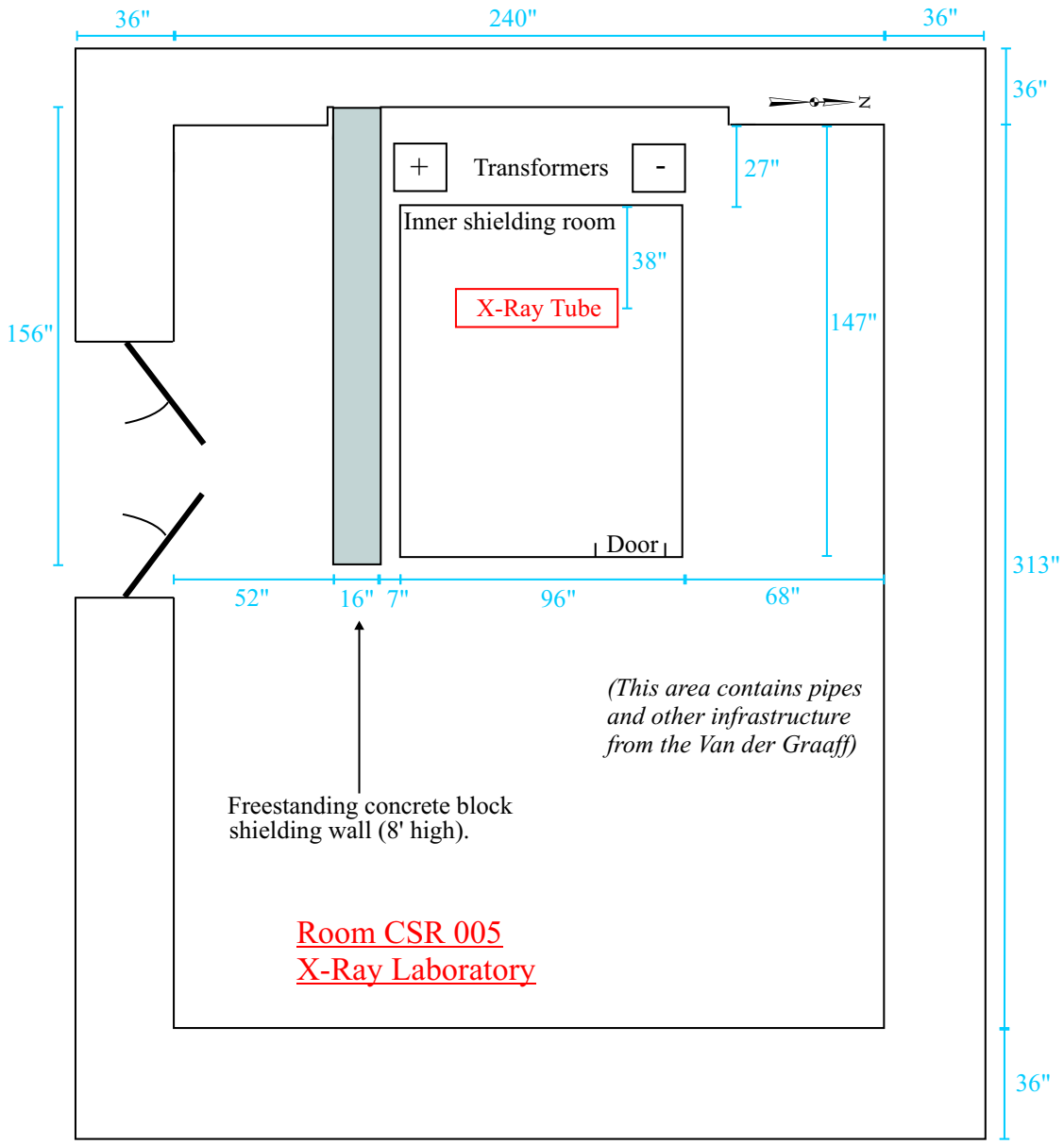
The x-ray tube can be mounted in two orientations, facing down or facing out at 90^o from the downward direction. The tube was mounted facing down for all tests. Two collar clamps were used to hold the x-ray tube in place on two large iron posts. A table was set in fixed position below the x-ray tube and all samples were clamped down to the table. Dosimetry was performed with an ionization chamber. Details of the dosimetry can be found in Appendix D.

5.4 Proton Irradiation Facility

The proton irradiation facility (PIF) at TRIUMF was used as a proton source. The PIF is located on the University of British Columbia campus in Vancouver. The PIF can provide two proton beams that cover an energy range between 10 MeV and 500 MeV. Figure 5.6 shows the layout of the beams within the test facility. The protons of the lower-energy beam (beam-line 2C) had an energy range between 10 MeV and 120 MeV. The higher energy beam (beam-line 1B) could provide protons with energy between 180 MeV and 500 MeV.

5.4.1 Beam-line 2C

Five of the six tests performed at the PIF used proton beam-line 2C. Four of these tests were performed with the device situated at the position of the "sample frame" in Figure 5.7 approximately 1.5 m from the point where the beam passes through a lead scat-



Notes

- Inner shielding room is 8' high and is made from 1 5/8" plywood and 2 X 1/16" stainless steel skin.
- Inner room is grounded.
- All cables run from SE corner of room to door.
- Drain from cooling system located in same region
- Electronic controls for device reside outside of main door.

Figure 5.5: Overhead view diagram of x-ray laboratory. Drawn to scale.

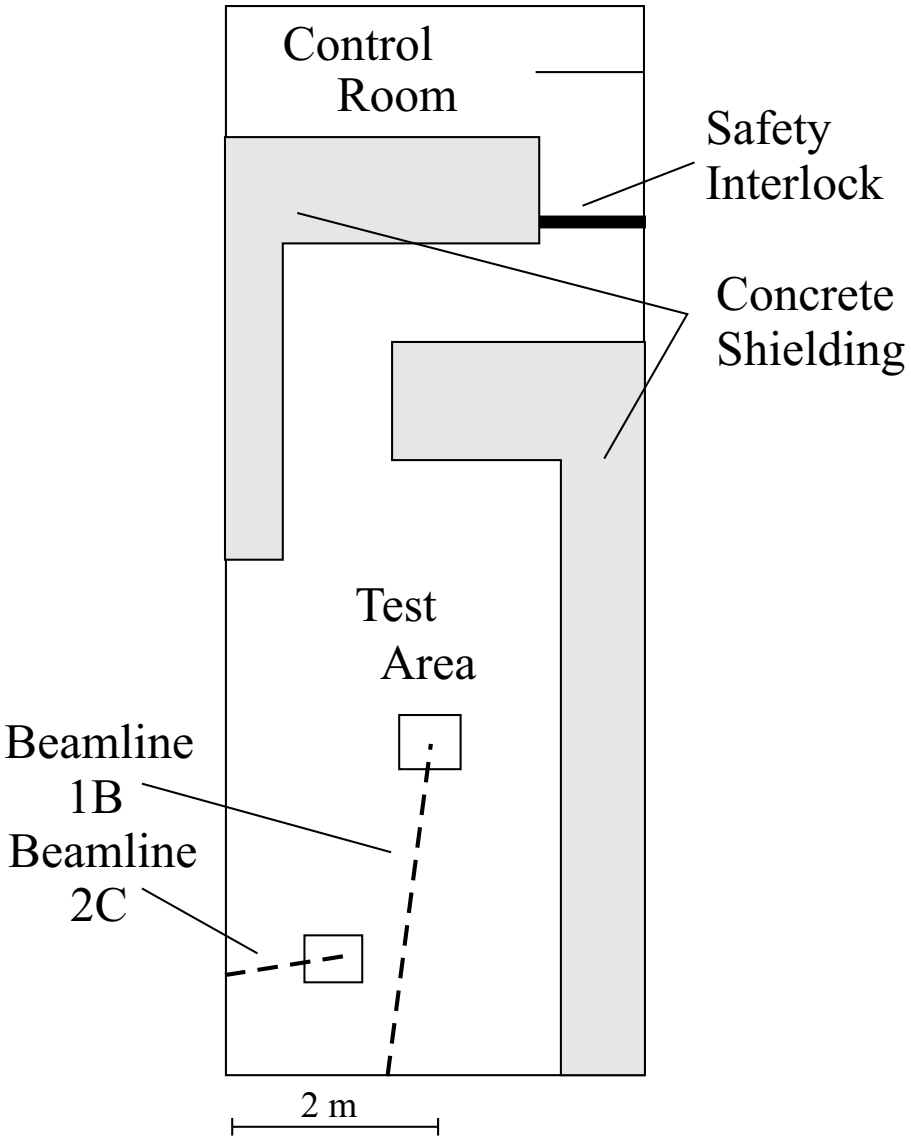


Figure 5.6: Test area at TRIUMF Proton Irradiation Facility showing the proton beams, control room and shielding.

terer. This position will henceforth be referred to as "standard position". Patients who are irradiated to alleviate eye tumors are done so at the standard position of beam-line 2C and hence careful dosimetry has been performed there on a regular basis[†]. The fifth test carried out in beam-line 2C was done 32 cm away from the lead scatterer so that a higher proton beam intensity could be achieved as the beam diverged with distance from the scatterer.

The proton energy range of beam-line 2C could be obtained using two primary extraction energies, 60 MeV and 120 MeV, and a lucite degrader to obtain energies below the primary ones. The proton flux which could be obtained was between 10^5 proton·cm^{-2}·s^{-1} and 4×10^7 proton·cm^{-2}·s^{-1}, with 10^9 proton·cm^{-2}·s^{-1} possible in the high intensity position. The two extraction energies, and their intensities, were controlled by the cyclotron operator. Changes to the beam of this type took on the order of 30 minutes. In order to enter the test area, a dipole magnet had to be turned off to ensure the proton beam did not enter the area. In addition, a safety interlock door was used and thus the turn around time for entering the test area was a few minutes.

Figure 5.7 shows the details of the beam path from the point of entering the test area to the target device. As the beam entered the test area it passed through a thin scattering foil in front of the first collimator to spread the beam to a size comparable with the sample. The second collimator was used to clip the tails of the scattered proton beam and a third, variable, collimator was used to set the beam size for the target device. The maximum beam diameter was 5.0 cm. A remotely controlled lucite rotating wedge degrader, that varied thickness with rotation angle, was used to reduce the beam energy. The wedge varied in thickness from 0 mm to 40 mm corresponding to range shifter settings of 0 to 3800. Changes in beam energy using the degrader took approximately one minute. The beam intensity was measured using an air ionization chamber [89].

The uniformity of the beam flux over an irradiation area of roughly the size of the 1 cm diameter was about 5% (Figure 5.8) in the standard position and about 3% over an area of about 3 mm in the high intensity position[‡] (Figure 5.9). The uniformity plots (Figures 5.8-5.10) were made using sheets of dosimetric material that changed color as a function of

[†]The PIF is also operated in conjunction with the British Columbia Cancer Agency as a facility for irradiating eye tumors.

[‡]The 1 cm and 3 mm diameters are of interest as the die of the devices tested in the standard and high intensity positions were about 1 cm and 3 mm respectively.

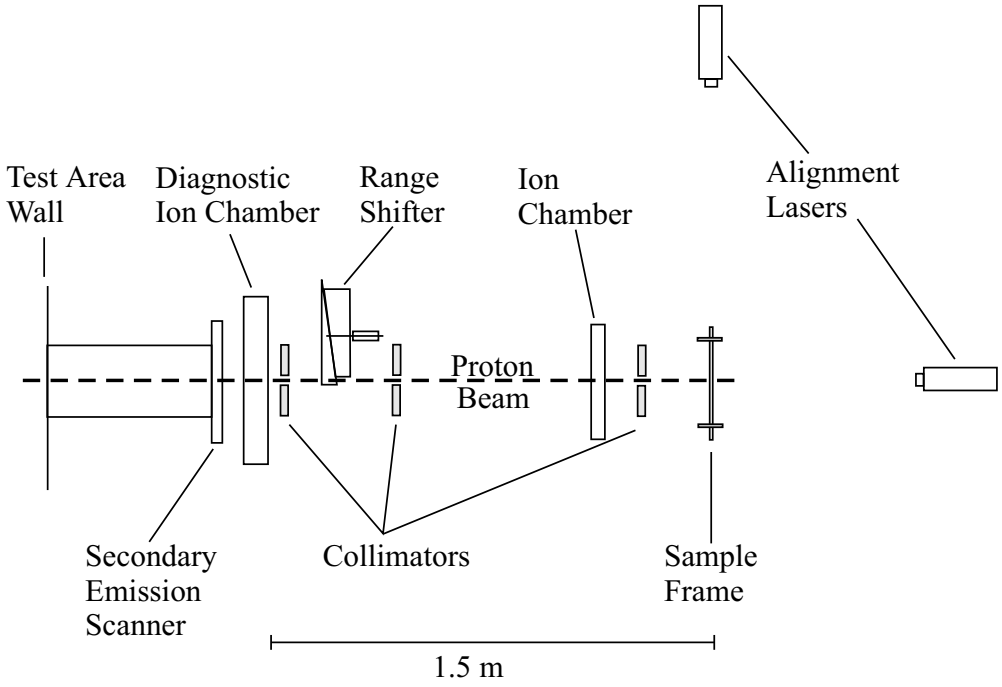


Figure 5.7: Top down view of Beam-line 2C, including all diagnostics, alignment lasers and sample frame (based on Ref. [89]).

Range Shifter Position	Test Energy (MeV)	Dose (10^{-2}rad/SC)	Fluence from chamber (10^{-4}p/cm^2/SC)	Fluence from scint. (10^{-4}p/cm^2/SC)
0	62.9 ± 0.5	0.86	6.5	6.1
200	57.7 ± 0.6	0.80	5.7	5.5
850	48.7 ± 0.8	0.75	4.6	4.5
1650	35.4 ± 1.1	0.69	3.3	3.2
2050	26.9 ± 1.5	0.67	2.6	2.4
2300	20.0 ± 1.8	0.69	2.2	1.8
2500	13.5 ± 2.6	0.74	1.7	1.3
2600	8.2 ± 3.5	0.48	0.7	0.8
0	105.0 ± 0.7	0.82	9.1	8.0
200	101.5 ± 0.8	0.80	8.8	7.7
1000	94.7 ± 0.9	0.80	8.0	6.9
2000	85.5 ± 1.0	0.77	7.2	6.3
3000	75.6 ± 1.1	0.75	6.3	5.5
3800	66.8 ± 1.2	0.74	5.7	4.9

Table 5.1: TRIUMF Proton Irradiation Facility calibration values. The energies greater than 62.9 MeV were obtained with the 116 MeV primary beam, while all other energies were obtained using the 70 MeV primary beam energy setting. The dose and fluence are both per scaler count. Data provided by Ewart Blackmore of TRIUMF [90].

absorbed dose. The sheets were then scanned and converted to the corresponding uniformity plots.

The proton intensity was measured with an ionization chamber, which was calibrated for water equivalent dose at the position of the device. The corresponding proton fluence was calculated using energy-loss tables from Refs. [41] and SRIM [42]. A scintillator telescope was also used to calibrate the ion chamber at low protons fluxes [89].

All energies and energy width values were determined using SRIM [42] and an incident energy spread of 1 MeV. Table 5.1 lists all of the energy and dosimetry values used during the tests. The values quoted for uncertainties in the energy settings have been converted from the FWHM values, provided by the PIF documentation, to standard Gaussian errors (standard deviations).

The total ionizing dose was measured in real time using an ionization chamber.

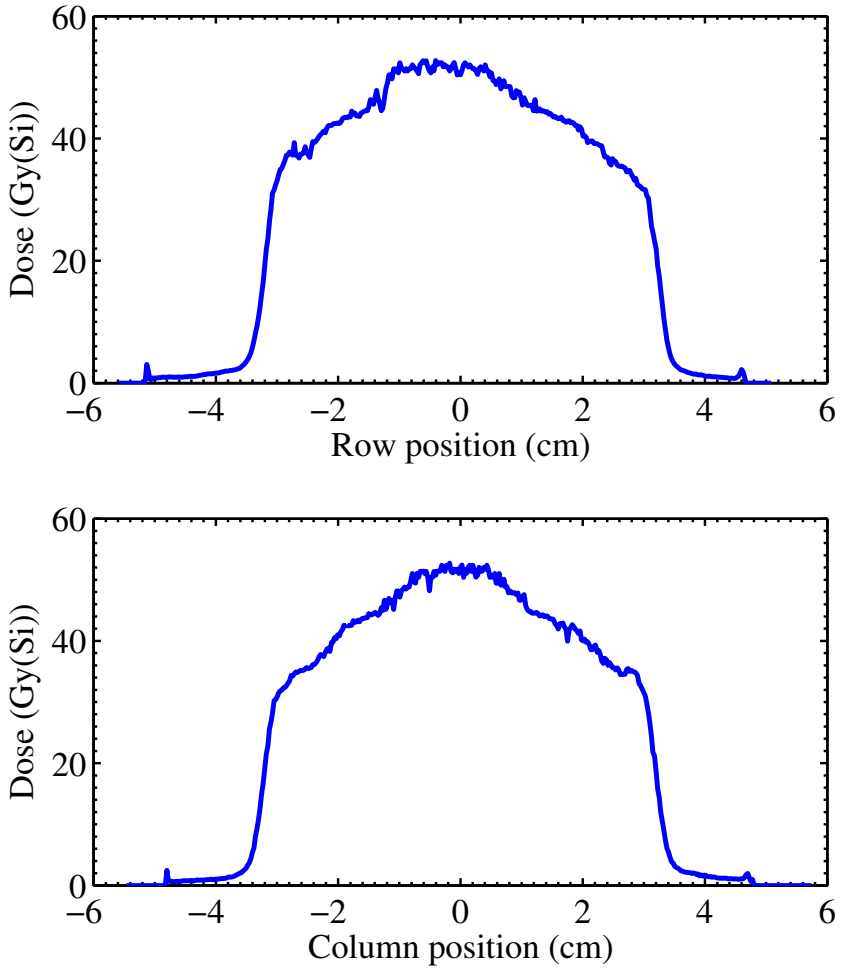


Figure 5.8: Dose profile for beam-line 2C, in standard position at the proton irradiation facility [90]

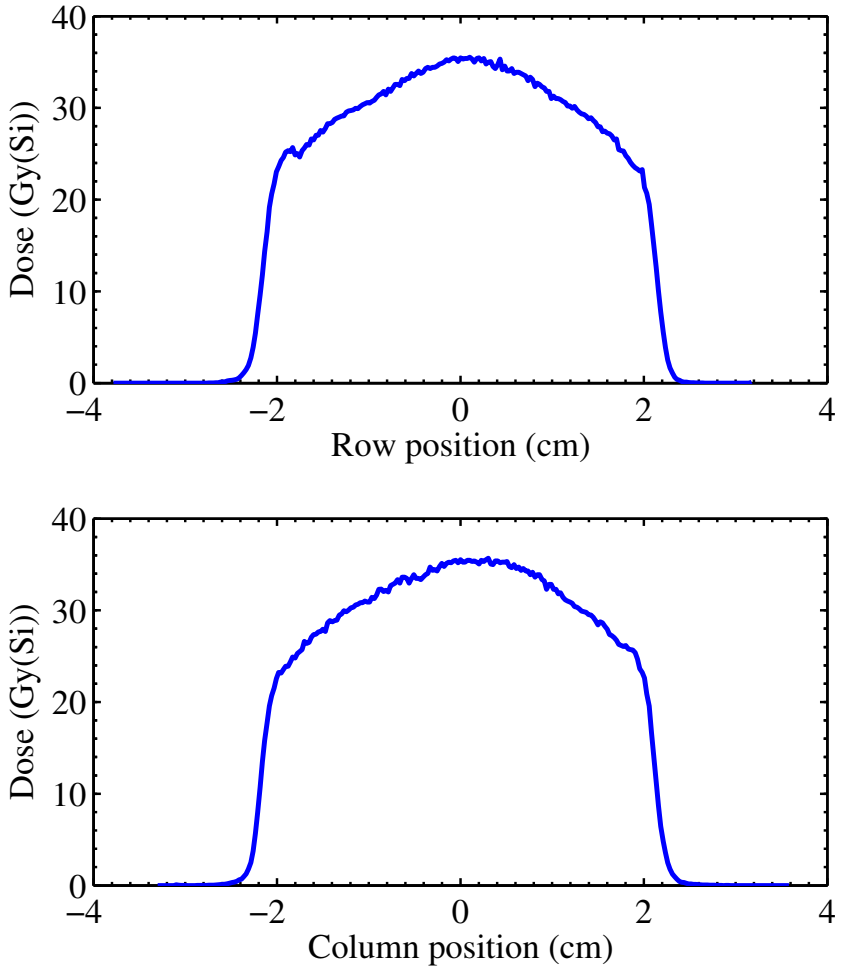


Figure 5.9: Dose profile for beam-line 2C in high intensity position at the proton irradiation facility [90]

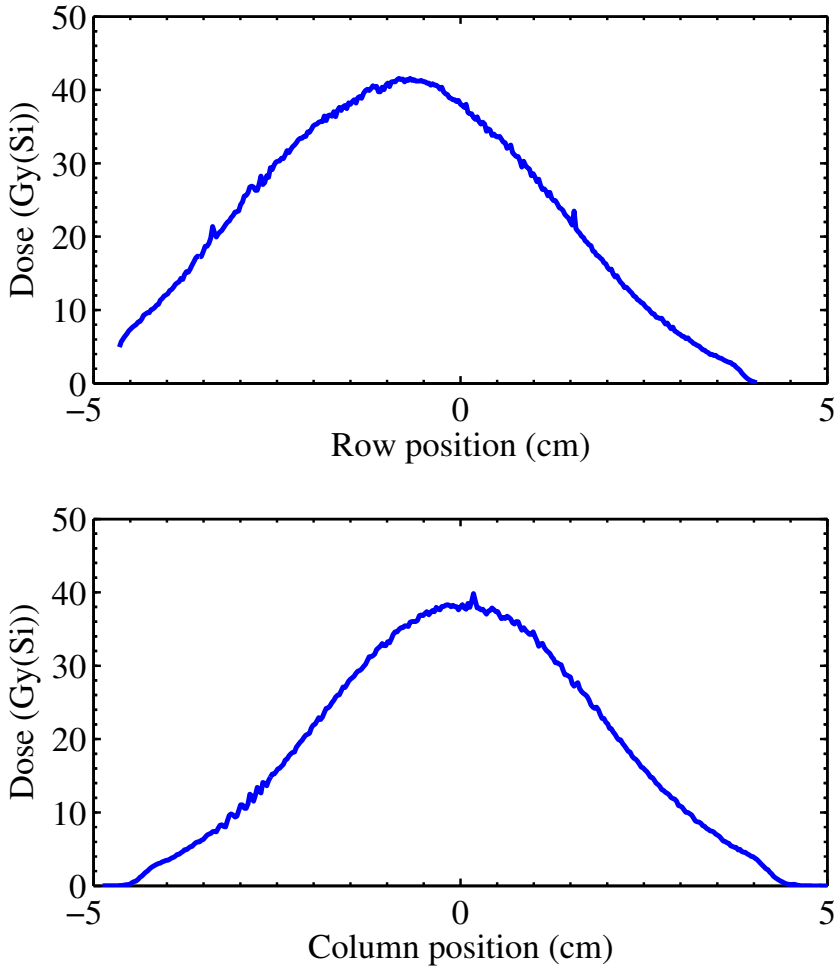


Figure 5.10: Dose profile for beam-line 1B at the proton irradiation facility [90]

5.4.2 Beam-line 1B

One of the six tests performed at the PIF utilized beam-line 1B. The protons encountered a lead scatterer about 1.3 m upstream from the position of the devices under study. The dosimetry was performed using a Faraday cup and checked against the ion chamber described in the previous section and agreement was within 1% for 200 MeV protons. The beam uniformity over a 3 mm diameter was approximately 5% (Figure 5.10 [90]).

Chapter 6

Descriptions of SCAC Prototypes

The goal of the SCAC prototyping procedure was to provide a device that would operate reliably within the ATLAS detector for ten years. The choice of technology used to implement the SCAC was thus based on a number of factors including cost, performance, and radiation hardness. The combination of the factors listed here led to the prototyping the SCAC circuit in both commercial-off-the-shelf (COTS) devices and application specific integrated circuits (ASICs) as SCAC prototypes.

Commercial-off-the-shelf programmable logic devices were an attractive choice for a number of reasons. A COTS device could provide an inexpensive* and readily available SCAC which could be remotely reconfigured after they had been installed inside the detector. The use of COTS devices was also important during the initial design and testing stages of the SCAC. They allow the circuit to be changed during development of the SCAC prototype circuits without the risk of having to permanently commit to a particular circuit.

Most commercially available programmable devices are not intrinsically designed to be radiation tolerant, so any candidate devices had to be tested in radiation environments as outlined in Section 2.7. Radiation tolerance testing of the COTS devices allowed a method to be developed and experience to be gained in such testing. It was also desir-

*During early development and planning of the ATLAS detector a COTS device was actually significantly more expensive than ASIC fabrication. The price of certain COTS, such as the Xilinx SPARTAN series, have dropped by an order of magnitude.

able to use the COTS prototypes to gain insight into the failure mechanisms of the SCAC circuit.

While there are some advantages to the use of programmable logic devices in the LAr readout system, the results presented in this thesis show that their use would be too risky. Thus ASICs were designed. An ASIC is a device in which a circuit for a particular application is permanently "built" into a chip; an Intel Pentium processor is a good example.

6.1 Commercial-Off-The-Shelf Devices Examined

Three COTS devices (two Xilinx field programmable gate arrays (FPGAs) and one Altera complex programmable logic device (CPLD)) were configured with the SCAC circuit and irradiated with protons and photons between January 1999 and September 2002.

6.1.1 Xilinx XC4036XLA Field Programmable Gate Array

Six Xilinx XC4036XLA-09HQ240C FPGAs were tested. This SRAM-based FPGA is fabricated in a 5 metal layer 0.35 μm CMOS process. The device is composed of an array of 36 by 36 user configurable logic blocks, which are configured by switches. The configuration logic blocks offer up to either 41,000 bits of RAM or 36,000 logic gates. A typical range of usable gates for a mixed logic and RAM configuration would be between 22,000 and 65,000 total gates, assuming that between 20% and 30% of the logic blocks are used for RAM. The FPGA operates at 3.3 V and is housed in an HQ240C package. This is a 240-pin plastic-molded surface-mount quad flat-pack. The body thickness is 3.4 mm and there is an embedded metal heat sink at the bottom of the package. The speed code[†] of this device was -09 [91].

The circuit that the XC4036XLA was configured with for the radiation tests occupied roughly 90% of the configuration switches and the user circuitry with a mix of about 50% sequential and combinational logic, and 50% for RAM.

[†]The speed code for a particular device is an arbitrary measure of the speed at which a particular circuit within the device would perform. It should only be used to compare devices of the same technology from the same manufacturer. Speed codes are not appropriate when comparing devices manufactured by different companies.

6.1.2 Xilinx Spartan II XC2S150 Field Programmable Gate Array

Four Xilinx XC2S150-5PQ208C SRAM-based FPGAs were studied. The XC2S150 is fabricated using a 0.18 μm 6 metal layer CMOS process. It is composed of an array of 24 by 36 user configurable logic blocks, which are configured by an underlying matrix of transistor switches. A typical configuration utilizes about 150,000 gates in a mix of logic and RAM. The speed grade of the device was -5 which corresponded to global clock input to output delay of no more than 5.5 ns. The logic core operates at 2.5 V and 3.3 V LVTTL (low voltage transistor-transistor logic) was used for the I/O. The XC2S150E was packaged in a 208 pin quad flat pack.

The SCAC circuit used 26% of the flip-flops and 54% of the look-up tables in the configurable logic blocks. The block RAM in the XC2S150 was not used.

6.1.3 Altera EPF10K50 Complex Programmable Logic Device

Eight Altera EPF10K50EQC240-1 CPLDs were studied. The EPF10K50 is fabricated in a 0.22 μm CMOS process and consists of 10 embedded array blocks for implementing megafunctions and 2,880 logic elements for general logic functions. Continuous horizontal and vertical routing channels provide connections between the embedded array blocks and the I/O elements [92]. The device typically offers 50,000 gates of logic and RAM. The device operates at 2.5 V and 3.3 V LVTTL was used for the I/O. The device was packaged in a 240-pin quad-flat-pack package.

The SCAC circuit occupied 80% of the embedded array blocks and 63% of the logic elements.

6.2 Application Specific Integrated Circuits Examined

Two ASIC approaches were taken for the development of SCAC prototypes. A circuit design for the SCAC was developed at the University of Alberta with consultation from CEA (Commissariat a l'Energie Atomique)/DAM (Direction Des Millitaires) [18, 93] and implemented in a radiation-hardened process, while another design of the SCAC circuit, utilizing circuit-level upset mitigation techniques, was developed at Nevis Laboratories of Columbia University with consultation from CERN and Dr. Douglas Gingrich of the University of Alberta [17]. The Nevis/Alberta design was implemented in an ASIC that

used a deep sub-micron process, which utilized some radiation hardening techniques, such as enclosed transistors and guard rings.

6.2.1 Durci Mixte Isolant Logico Lineaire Application Specific Integrated Circuit

One of the two ASICs used the radiation hardened DMILL (Durci Mixte Isolant Logico Lineaire) technology. This technology was originally developed by CEA/DAM in France. The technology is now produced by ATMEL [94].

The DMILL process utilizes a SIMOX (Separation of Implantation of Oxygen) buried oxide and an SOI (silicon on insulator) substrate, which significantly reduces the sensitivity of the circuits to transient irradiation effects, such as parasitic currents and single event transient upsets, caused by single ionizing particles [95, 96, 94]. A trench technique is used to prevent the latch-up inherent in CMOS technology. These, along with other proprietary techniques, combine to provide devices that are hardened to tolerate 10^{14}neutron/cm^2 and a total integrated dose of $>$1 MGy(Si) [94]. The RAM in the DMILL technology is not proven against the single event transient errors.

The radiation hardness of the DMILL technology makes it an attractive option over other technologies. The design rules of the technology, however, come with some disadvantages. The minimum lithography size for the DMILL technology is 0.8 μm, which allows for about one million transistors per square centimeter.

The SCAC design was implemented in DMILL, simulated using MODELSIM and layed out using CEA resources. Forty devices were fabricated in June of 2001 and arrived at the University of Alberta on July 3, 2001. The die size of the devices was 7.526 mm by 10.526 mm giving a die area of 79.2 mm^2. The parts were packaged by Edgeteck in a 144-pin flat-pack package (CQFP144).

Three circuits of the DMILL design were not taken from the tested design libraries and radiation hardness had to be determined for these circuits. The three circuits were a dual-ported RAM that was developed for the Alberta high-energy physics group by CEA, a "power-on" reset (POR) circuit developed by Laboratorie de l'Accelerator Lineaire (LAL), and input buffers that were used to provide pseudo-LVDS (low voltage differential signals) communication. The input buffers had been used in another chip to be used in ATLAS, the switched capacitor array chip, which was found to be radiation tolerant. The

POR circuit and dual-ported RAM were possible circuits that could be sensitive to the effects of radiation and would require radiation testing.

The POR circuit was included as a means to ensure that after an initial power-up or power cycle the device would start in a well defined state. Once the power to the device core had reached a particular voltage level the POR circuit would issue a reset pulse. One concern was that any malfunction of the POR could cause spurious resets of the SCAC circuit. The POR circuit was thus designed such that a jumper could be used to include or remove the POR circuit from the circuit.

The dual-ported RAM was designed by the engineers at CEA but was never tested under irradiation of any type. The DMILL process rules were used in the design of the RAM, but as it had never been tested ATMEL would not guarantee radiation hardness.

6.2.2 Deep Sub-micron Application Specific Integrated Circuit

The second SCAC design was carried out at Nevis Laboratories. The design was implemented in a deep submicron CMOS process [17]. The CERN `cmos6sf25` standard cell library for a 0.25 μm process was used for the design. Radiation hardness against TID effects was achieved using edgeless transistors and guard rings. A dual-ported RAM was developed to operate at 40 MHz and LVDS (low voltage differential signal) I/O drivers had to be designed for the DSM device. Mitigation techniques, such as triple redundancy with majority voting and Hamming codes, were employed to alleviate the concern of SEUs in the SRAM cells and registers. The device had a die size of 2.7×2.7 mm^2.

The SCAC was submitted for prototyping on February 28, 2001 and the bare die were received in July, 2001. A second prototype, mainly required to add electro-static discharge (ESD) protection to the I/O blocks, was submitted in November 2001. Packaged parts were received April 5, 2002 and radiation qualification tests were performed on the devices at the University of Alberta. A third prototype was submitted for fabrication in February 2003.

Chapter 7

Tests for Total Ionizing Dose Effects

The radiation qualification procedure required that tests were performed to ensure that any candidate SCAC device would function as the design for the circuit specified, i.e. without failing or drawing excessive amounts of current when the device was exposed to radiation levels similar to those expected in ATLAS. Total ionizing dose testing and single event effect testing, with the device operating to full capacity, were required to satisfy the ATLAS LAr electronics radiation tolerance criteria. In addition to the required TID and SEE tests, a neutron irradiation was performed on the DSM prototype to examine any effects of displacement damage. The majority of this and the following chapter focuses on the TID and SEE tests performed on the SCAC prototypes.

Total ionizing dose tests were performed on all of the prototype SCAC devices, with the exception of the XC4036XLA FPGA which has been tested previously [86]. Total ionizing dose tests were carried out using the ^{60}Co and x-ray facilities described in Chapter 5. The ^{60}Co facility was in place and operational before the commissioning of the x-ray facility and hence TID tests performed prior to 2001 utilized the ^{60}Co facility, while latter tests utilized the x-ray facility. The dose rate provided by the x-ray facility was significantly higher than that of the ^{60}Co facility, which made it an attractive approach for the tests. Tests that would have required weeks of irradiation could be performed in hours. The TID tests were performed following the basic procedure outlined in Ref. [97]. The device under test (DUT) remained under bias voltage during the irradiation period and there were no breaks in the irradiation period longer than one hour. Dosimetry was performed during and after the irradiations in the case of the the x-ray tests, and only after the irradiations for the ^{60}Co tests, where to perform the dosimetry required access to the radiation

area. For each test the entire test system was set in place and run for up to 24 hours prior to exposure to radiation to ensure stability.

7.1 Test Procedure and Monitoring for All Tests

The procedure for performing the TID and SEE tests was the same for all devices with slight variations in the test systems. The programmable logic devices were configured with the SCAC circuit that will be used in ATLAS. The circuit consisted of a pipeline implemented in a series of dual-ported FIFO memories containing sequential capacitor addresses. Movement of the addresses between the FIFOs was controlled by a set of Mealy finite state machines*. The circuit was operated at 40 MHz and periodically (between 15 Hz and 15 kHz) sent trigger pulses to exercise some of the Mealy machines within the circuit. Additional "watch-dog" circuitry monitored the sequence of addresses in the circuit. If an error occurred in the pipeline or in a state machine, the addresses in the pipeline would go out of sequence, which would then be detected by the watch-dog circuit. A bit in a status register in the device would then be set. If an error occurred in the diagnostic circuits, it would result in a false error and again a bit in the status register would be set. It should be noted here that the circuitry of the DSM ASIC was significantly different than that described here for the other 4 prototypes but the basic FIFO structure described here still applies. The DSM circuit had additional circuitry for EDAC and triple redundancy.

A data acquisition (DAQ) computer was used to monitor the status register directly for the XC4036XLA and EPF10K50 devices, or via an intermediate FPGA for the other devices. There were three versions of monitoring software used for the radiation tests. Each version provided a means by which to monitor the status of the DUT and record data, as well as to remotely send commands to the DUT. In the case of the programmable logic devices, the monitoring software was also used to send the configuration bit-stream to the DUT. While the basic function of the monitoring software was common to all of the tests, significant changes to the monitor code were made on two occasions. The first change in monitor software was made due to the large and convoluted nature of the earliest code used. The software used for the XC4036XLA and EPF10K50 test systems was

*A Mealy state machine is a sequential circuit whose output depends on both the input to the circuit and the current state of the circuit.

a modified version of that described in Ref. [86]. This version of the monitor code was developed during the early stages of the radiation testing performed at the University of Alberta and had been altered on many occasions to accommodate changes to the overall test system and methods. It was found that the large size of the code was beginning to cause problems with respect to timing, which was a concern when communicating with a remote device. It was also desired to reduce the complexity of the monitor code such that it would be more easily managed. The second incarnation of the monitoring code was used for the tests of the EPF10K50 and DMILL prototypes and is described in detail in Appendix E. The third version of the monitoring code was that used for the DSM test system. This code was developed by the researchers at Nevis Laboratories and rewritten at the University of Alberta to accommodate changes made to the system hardware and to allow communication via the DAQ computer parallel port with the test system.

The monitoring code was designed to reset the values stored in RAM and registers whenever an error was detected. If a bit was set in the status register, the monitoring program issued a reset. If a circuit reset could clear an error, it was believed to have occurred in the logic cells (or circuit) of the device rather than in the configuration switches. If a reset would not clear the error, it was believed to have occurred in the configuration switches, which would not be affected by a reset. Errors were logged by the monitor program.

The reset caused a fresh set of sequential addresses to be loaded into the FIFOs and the state machines were re-initialized. In the case of the programmable logic devices the monitor code also configured the DUT by sending a stream of bits to the device that defined the circuit to be used. If three successive resets (within a time frame of one second) did not restore the circuit to an operating condition where no errors were detected, the device was reconfigured.

The DUT was always mounted in a chip carrier with a snap-down lid on a small printed circuit (PC) test board (Figure 7.1), except for the DSM device which was mounted in a different socket. In addition to the DUT and socket, the PC boards, with the exception of the DSM test board, contained a 40 MHz oscillator, switches, connectors, LEDs, and a small number of passive components. Power supplies were used to provide power to the DUT and any other active components on the test board. External triggers were provided

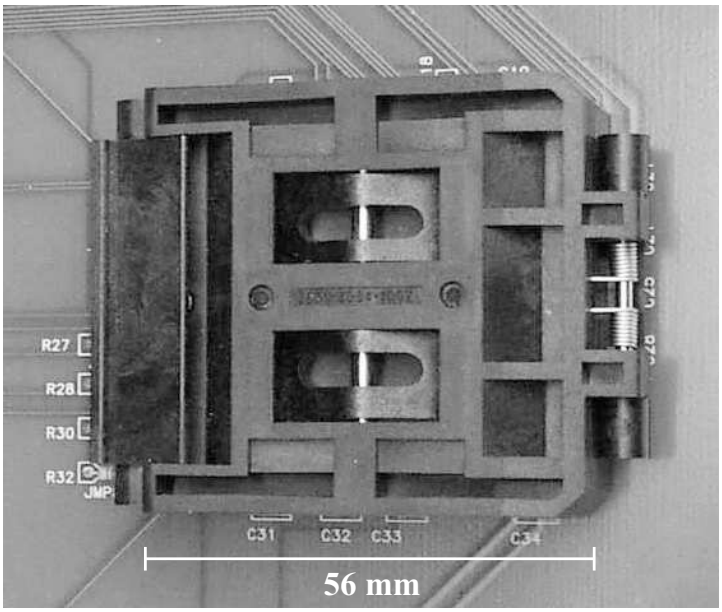


Figure 7.1: Top down view of the snap-down socket used to mount the prototype devices for the radiation tests.

to the XC4036XLA and EPF10K50 prototypes using an external pulse generator, while the other systems were provided triggers generated in software or in the circuitry of monitor programmable logic devices. The basic test arrangement used for all of the tests had the DUT and the test board in the radiation area with the DAQ computer and power supplies located remotely in a "safe area". There were variations in this basic setup and these will be discussed where the particular details are relevant.

7.2 Test Procedure and Setup for TID Tests

There were two TID test configurations used and both were independent of the radiation source used for the tests. The first configuration is pictured in Figure 7.2 and was used for the TID tests of the EPF10K50 prototype. The test board and the pulser were located in the test area. A 3 m coaxial cable was connected from the pulser to the test board. The DAQ computer was connected to the DUT via a 13 m parallel cable and was used to monitor the internal status register of the DUT. Two power supplies were used to provide three different supply voltages. A voltage of 2.5 V was applied to the core (user configured

logic) of the DUT, a voltage of 3.3 V was applied to the I/O blocks and a voltage of 5.0 V was applied to the test board components. A second configuration was used for the TID tests of the XC2S150, DMILL, and DSM systems (Figure 7.3). The main difference between the two configurations was the addition of an intermediate monitor board that contained an FPGA and simulated the functionality of the ATLAS LAr FEB. The monitor board also contained voltage regulators that were used to maintain power to other devices. The same monitor board was used for the XC2S150 and DMILL systems (Figure E.1) and communication between the test and monitor boards used LVDS for communication. In LVDS communication, two signals, rather than one signal and a "fixed" ground, are used in the communication which means that noise will affect both of the signals in the same manner. This will preserve the information transmitted along the cables. The test board was altered for the XC2S150 and DMILL devices in such a manner that the DUT was spatially separated from the other components on the board (Figure 7.4). For the XC2S150 tests the logic core and I/O blocks were powered directly from power supplies to allow individual current monitoring, while the components on the test board were powered from the monitor board. A power supply was used to provide 6 V to the monitor board. The DMILL system was essentially the same with the exception that power was provided directly to the test board, output buffers, input buffers, DUT core and RAM, and monitor board. No power was provided by the monitor board. All 5 of the currents were monitored during the x-ray irradiation periods.

The system used for the DSM SCAC prototype was different than the DSM and XC4036XLA system in that it used a different monitor board in addition to a different test board. The boards used for the DSM test system are shown in Figure 7.5. The test board contained only the DUT and a few passive components. The monitor board contained 3 voltage regulators that were used to power the DUT on the test board and would shut off if a latch-up event occurred. A ribbon cable was used for communication between an FPGA on the monitor board, which was used to simulate the functionality of the FEB, to the DAQ computer. Two ribbon cables allowed communication, using LVDS signals, between the DUT and the monitor FPGA. The TID test configuration used for the DSM TID tests was the same as that in Figure 7.3 but the current to the entire device was monitored, rather than both the I/O and core. A digital multi-meter (DMM) connected to a DAQ

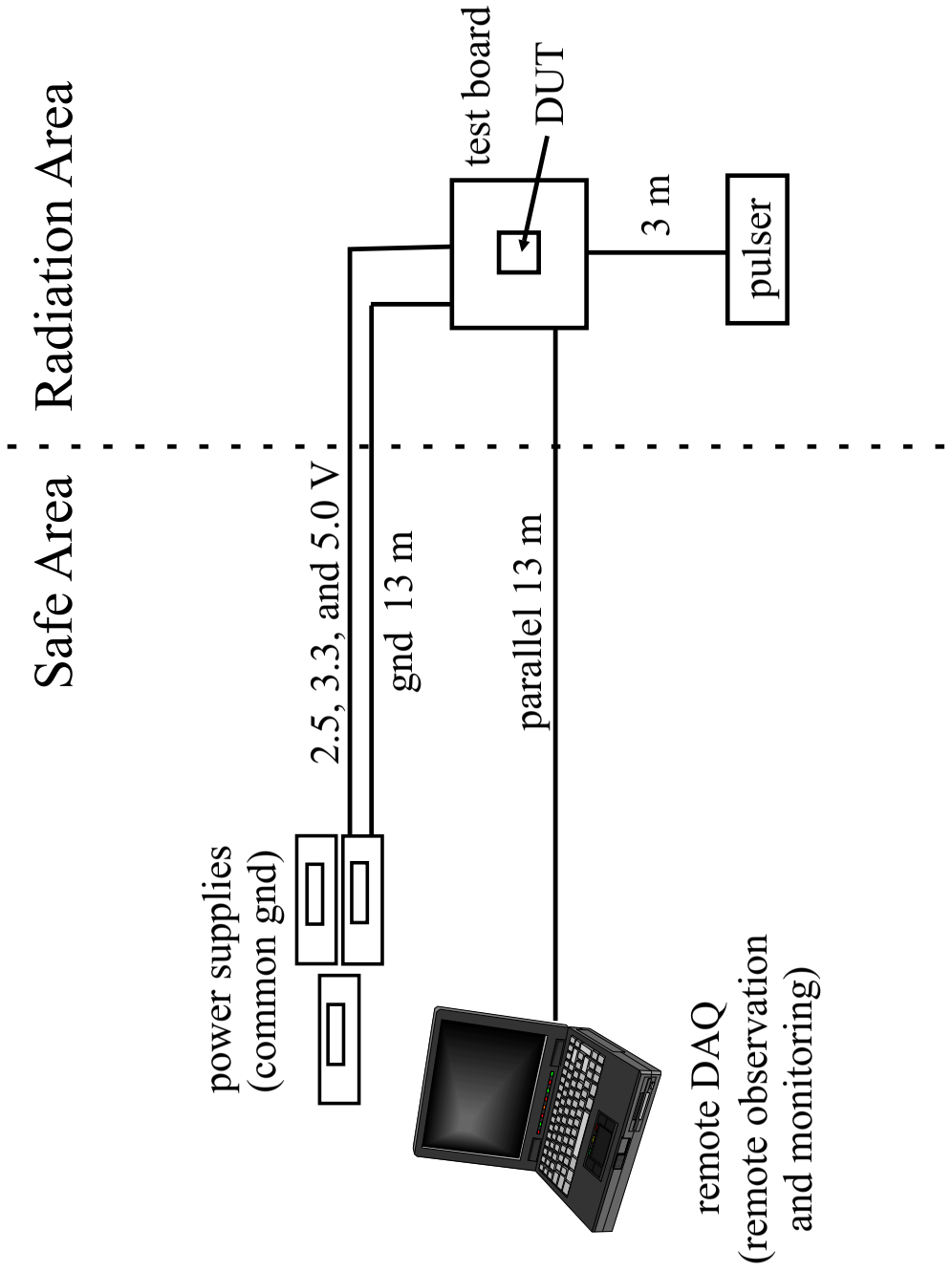


Figure 7.2: Test setup used for the ^{60}Co and x-ray irradiations of the EPF10K50 prototype SCAC.

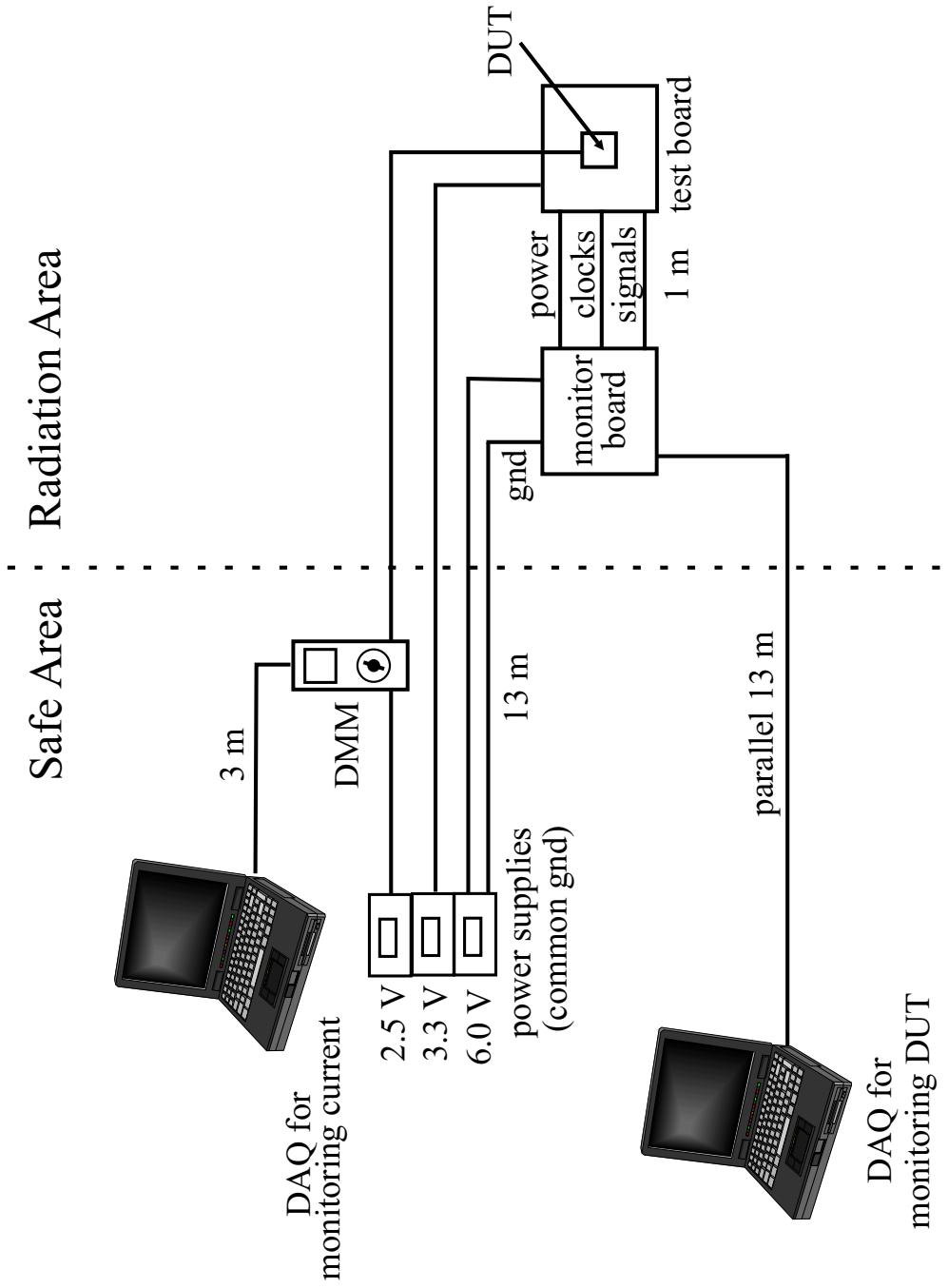


Figure 7.3: Test setup used for the ^{60}Co and x-ray irradiations of the XC2S150, DMILL, and DSM prototypes. (There were slight variations between the systems used to test the different prototypes.)

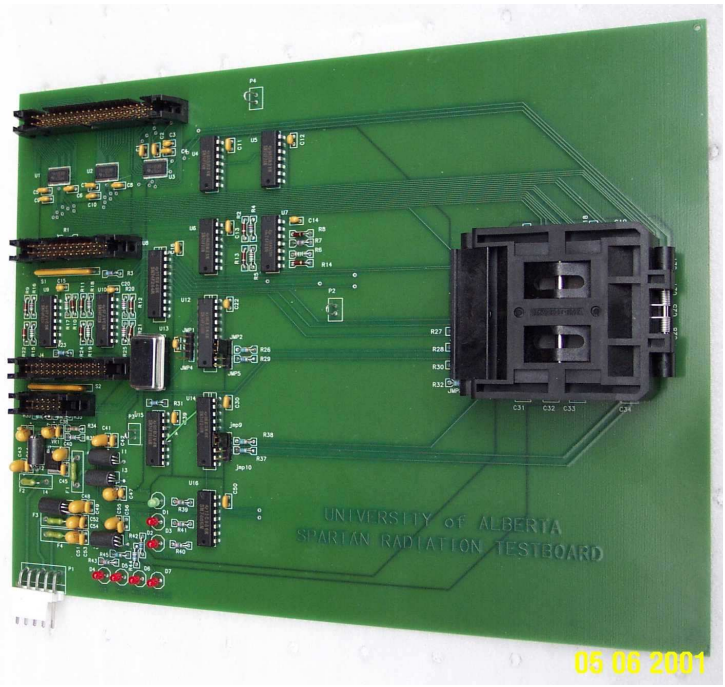


Figure 7.4: Test board used for XC2S150 tests showing separation of DUT from other components.

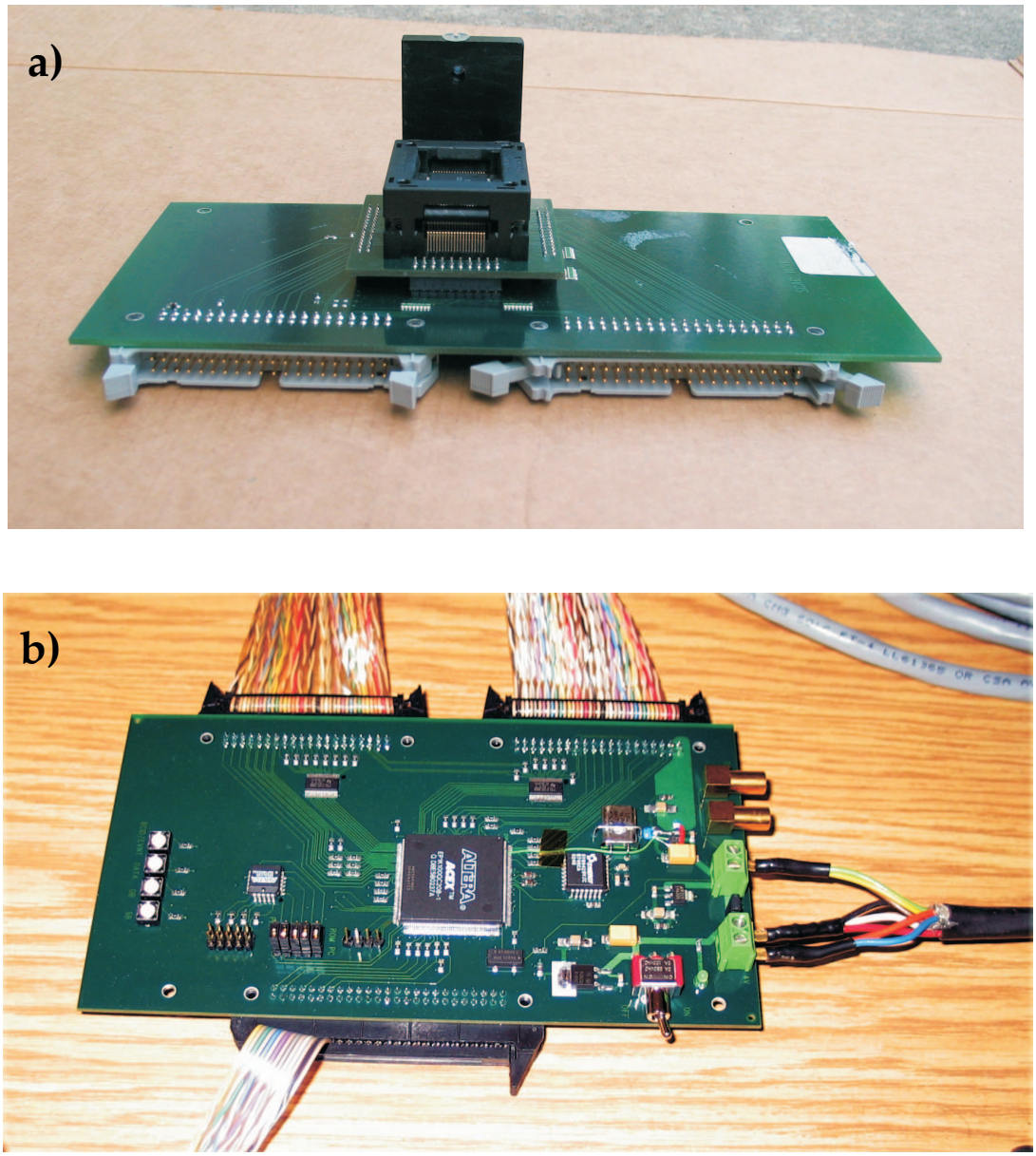


Figure 7.5: Photographs of the test PC used for the DSM system ((a)test board, and (b) monitor board). The photograph of the monitor board shows a parallel cable attached on the top edge and two ribbon cables attached on the bottom edge. Power was supplied through the wires on the left edge.

computer was used to log the current drawn by the DUT for the DSM test. The currents for the tests of the other prototypes were logged manually.

7.2.1 Test Board Mounting for TID Tests

The majority of the TID tests were performed in the x-ray facility but 3 tests of the EPF10K50 were performed in the ^{60}Co facility. The tests were performed in the same manner, as described above, but the test boards were mounted differently in each facility. For the ^{60}Co tests the board was mounted vertically in front of the source (Figure 7.6). The board was slid down into rails mounted on the inside of an aluminum box, which was used to attenuate the low energy photons coming from interactions between the primary photons and the lead blocks that shielded the test board. The aluminum box was set inside the lead enclosure, which had an aperture machined into one of the lead blocks to allow the collimation of the photons coming from the source onto the DUT. The aluminum box also provided a support structure and a place to hold the board and dosimeters. A Plexiglas sheet was placed on top of the lead enclosure and lead blocks were placed on top of this prior to testing. The Plexiglas was used as a platform for the top lead blocks to prevent them from falling into the enclosure.

For the x-ray tests the PC board was slid along aluminum rails in a plywood box (Figure 7.7). The aluminum rails were placed as close to the top of the box as possible so that the DUT would be near to the radiation source. The board was slid in inverted so that the bottom of the DUT faced upward so that photons could enter the DUT from the back rather than through the complicated socket. The box was then clamped into place directly under the window of the x-ray tube. A hole of the same area as the DUT was cut in the plywood on the top of the box containing the DUT. A large lead block, with a hole of the same size as that in the plywood machined into it, was placed on top of the box to shield all of the test board except the DUT. The table supporting the test apparatus was fixed to the floor to ensure all devices were tested in precisely the same position.

All irradiations, with the exception of those performed on the DSM prototype, were done such that the photons passed in from the back of the chip. This was done to ensure that the radiation field at the die was as uniform as possible as the front of the snap-down socket containing the DUTs (Figure 7.1) had a complicated geometry. The top of the socket

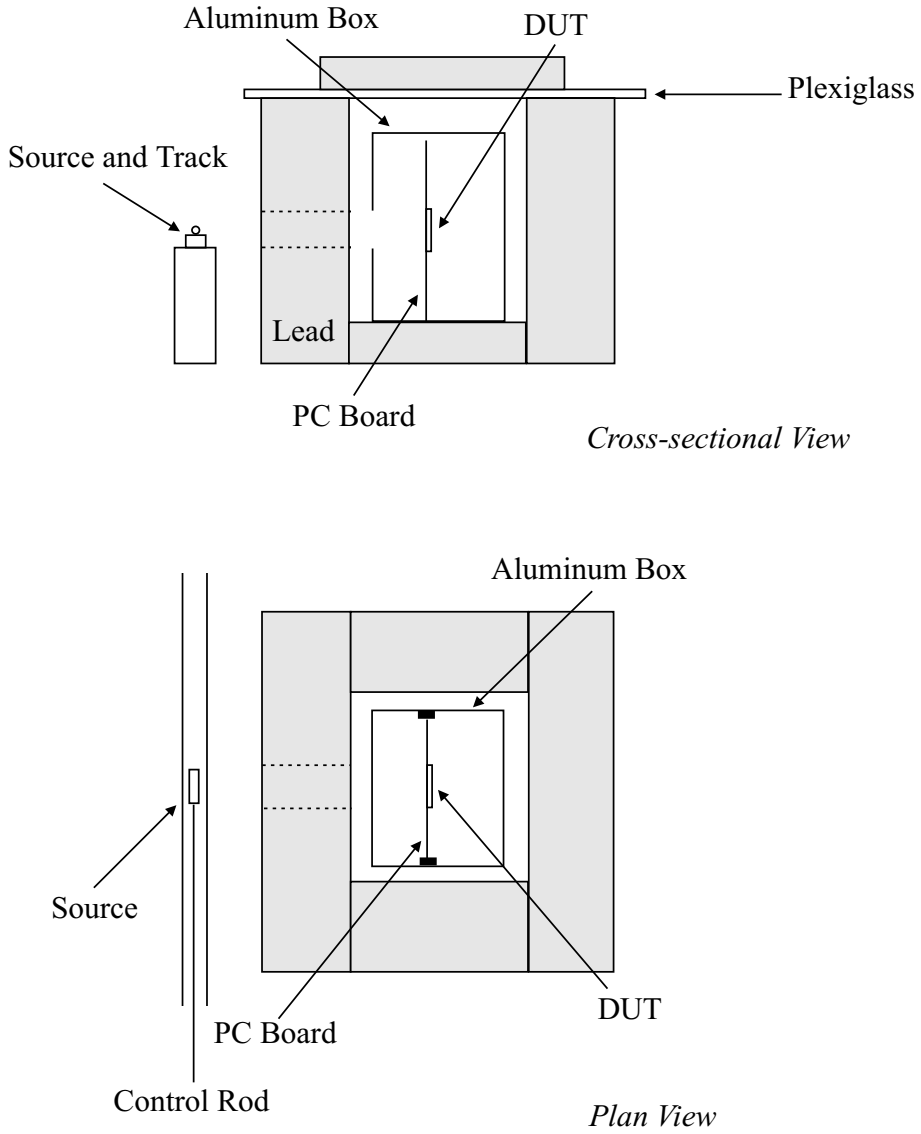


Figure 7.6: Setup of Altera EPF10K50 tests in the ^{60}Co facility showing the test box, source, and lead shielding. The dotted lines illustrate the aperture in the lead shielding which collimated the photons onto the DUT.

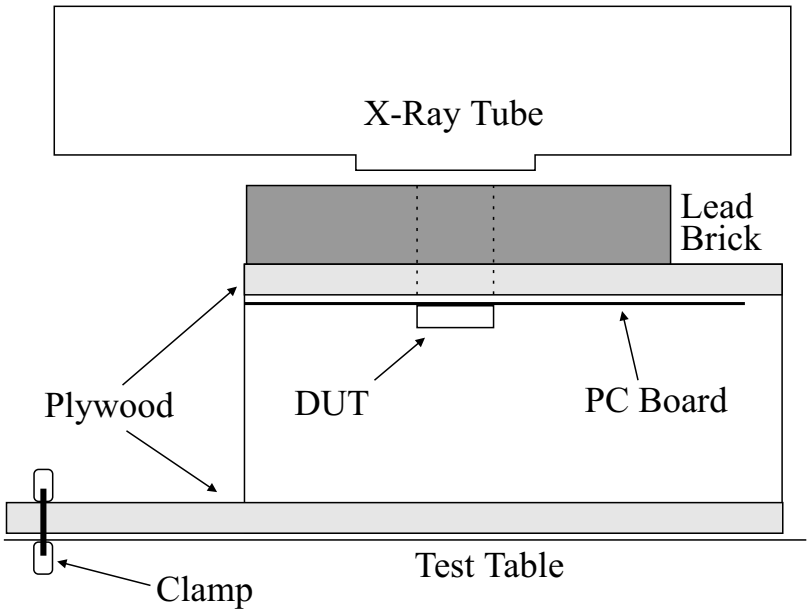


Figure 7.7: Setup of the Altera EPF10K50 tests in the x-ray facility showing the test box, x-ray tube, lead shielding, and test table. The dotted lines represent the column of cut away material between the x-ray tube and the DUT.

used to hold the DSM chip was open (Figure 7.5a) and posed no radiation field uniformity concerns.

7.3 Total Ionizing Dose Test Results

Seven EPF10K50 SCAC prototypes were tested between March, 2001 and December, 2001. Specific dates of the irradiation periods, as well as the types of tests performed on each device, are tabulated in Appendix B. Three EPF10K50 devices were irradiated in the ^{60}Co irradiation facility and four devices were irradiated in the x-ray irradiation facility. Four XC2S150 prototype devices were tested in the x-ray irradiation facility between December, 2001 and March, 2003.

7.3.1 TID Tests of the EPF10K50 Prototype Using the ^{60}Co Facility

Three devices were irradiated in the ^{60}Co facility (DUTs #3, #4, and #6)[†]. An average total ionizing dose of (2530 $\pm$ 410) Gy(SiO_2) was absorbed during the tests. The doses for each test are listed in Table 7.1. The power supply current did not increase for either the logic core or I/O circuitry during the three ^{60}Co tests. Two of the three tests (those on DUTs #4 and #6) were stopped as unrecoverable errors were detected. The ^{60}Co test of DUT #3 was stopped prior to any errors being detected. This test was stopped as a dose much larger than expected for similar devices [86] was absorbed and a test of the device functionality, outside the radiation area, was desired. Unrecoverable errors were observed upon reconfiguration of the device. The two devices which failed during testing could not be reconfigured without continuous errors either.

7.3.2 TID Tests of the EPF10K50 Prototype Using the X-ray Facility

Four devices were irradiated in the x-ray irradiation facility (DUT #0, DUT #1, DUT #2, and DUT #5). The devices were irradiated until they had either received a dose of 2 kGy(SiO_2) or ceased to function as this was roughly four times that expected for similar devices. The EPF10K50 irradiated with x-rays absorbed a mean dose of (832 $\pm$ 90) Gy(SiO_2) on average prior to an increase in power supply current provided to the core circuitry. Table 7.1 contains the doses at which the power supply current began to increase and the total doses absorbed for the devices and Figure 7.8 shows the current during irradiation. The uncertainty in the time when the current began to rise has been added in quadrature to the uncertainty in the dose calculation. Two of the four devices (DUT #0 and DUT #1) operated until they had absorbed the target dose of four times that absorbed by similar devices, while one (DUT #5) began producing unrecoverable errors sooner. Irradiation of the last device (DUT #2) was stopped early so the device could be tested. The effects of radiation observed as changes in power supply currents, were described by: the dose at which the current had risen by 10% of its baseline value, and the point where the current stopped increasing while under irradiation. The significance of the former measure was that an increase in current greater than 10% ensured that the change in the measured

[†]The numbering scheme was completely arbitrary and not related to any codes printed on the devices during packaging.

Facility	DUT #	Dose (Core) Gy(SiO_2)	Dose (Total) Gy(SiO_2)
^{60}Co	3	N/A	2720 ± 440
	4	N/A	2390 ± 390
	6	N/A	2480 ± 400
x-ray	1	1460 ± 265	5080 ± 810
	5	682 ± 127	1480 ± 230
	0	1007 ± 237	4160 ± 660
	2	936 ± 181	2500 ± 400

Table 7.1: The dose at which the logic core power supply current increased from the baseline value for the EPF10K50 parts. There was no change in current during the ^{60}Co irradiations.

power supply current was greater than the uncertainty in the measurements. The latter measure was chosen as it was suspected that once the power supply current ceased to increase further, after an initial increase, the circuit had begun to fail. This hypothesis is discussed further in section 7.4.

The low value of the absorbed dose for DUT #5 is about 2.4 standard deviations from the mean of the values for the other three devices. Assuming simple Gaussian errors, the probability that this would occur is about 2% and thus the data were included for all calculations.

There was no measurable change in the power supply current for the I/O blocks during any of the tests. As in the case of the ^{60}Co tests, following the termination of the irradiation period the devices could not be reconfigured, or else they reconfigured with continuous errors resulting. After irradiation the power supply current would jump by as much as 1.5 A and slowly settle to lower, although higher than baseline, values over the period of a day or so.

There was a significant difference in the response of current to irradiation between the two methods of irradiation. The lack of current increase during the ^{60}Co tests was not understood. The devices failed to operate after the test period, which indicated that the devices were damaged by the radiation.

The lack of current increase in the I/O part of the device could have been due to coupling between the power supplies. A double power supply was used to provide power

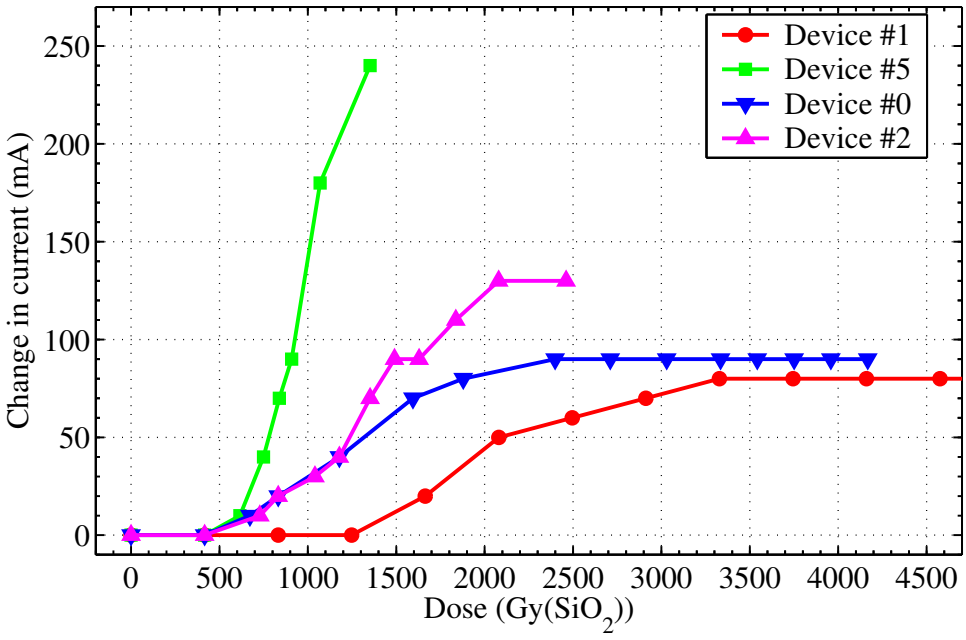


Figure 7.8: Change in power supply current for the logic core versus absorbed dose for the EPF10K50 SCAC prototype.

to I/O part of the circuit and the test board, while a single power supply was used to provide power to the logic core of the device. It is possible that current from one supply could have leaked back into another supply, which could mask the effect of the irradiation on the part of the corresponding circuit. When the voltage for the I/O power was turned completely down on the power supply, but not the other supplies, the meter still read a measurable, non-zero, voltage. When the voltages on the other supplies were turned to zero, the I/O voltage could be completely turned off.

While an increase in power supply current was expected (Refs. [84, 58]), the leveling off in current observed in the x-ray tests without an eventual failure was not. It is proposed that the device stopped functioning, in whole or in part, at the point where the increase in current stopped. If the device operation was halted, changes in any registers containing error information would also halt. To explore this possibility one of the tests (that on DUT #2) was terminated just after the power supply current had levelled off so that the device operation could be examined. It was found that the behaviour at this point

in the irradiation[‡] device behaved in the same manner as those that had been irradiated much longer after the current had levelled off. The device would not configure, and the power supply current jumped by approximately 1 A during the attempted reconfiguration.

The two devices irradiated in the ^{60}Co facility prior to the x-ray tests were examined on the test bench on November 5, 2001 to observe any possible annealing effects. The device irradiated between May and June had remained at room temperature for approximately 6 months, while the device irradiated during September had remained at room temperature for approximately 1 month. After configuration[§] the power supply currents, both logic core and I/O, had the same values as those during the irradiations. Both devices configured and began producing continuous errors from the SCA readout circuitry after about 5 minutes. Both devices behaved almost identically during this test. Both devices could be reconfigured after the errors were observed but began erroring immediately after. It appears that limited annealing occurred at room temperature. After the first month there was little improvement in the device operation.

7.3.3 TID Tests of the XC2S150

The results of the x-ray irradiations of the XC2S150 prototypes are shown in Figures 7.9 and 7.10, which show the power supply currents measured during each irradiation. Table 7.2 gives the doses at which the core and I/O currents began to increase. The average values for these doses were (331 $\pm$ 29) Gy(SiO_2) for the core and (395 $\pm$ 34) Gy(SiO_2) for the I/O blocks. The uncertainty is again that in the time when the current began to rise added in quadrature to the uncertainty in the dose calculation. The four TID tests of the XC2S150 were terminated at the point where unrecoverable errors were being detected. The second column in Table 7.3 lists the total dose at which the first error occurred. The average time for the occurance of the first error was (523 $\pm$ 45) Gy(SiO_2). The third column in the table gives the dose at which the device would no longer function. The average dose at which the XC2S150 would not function was (560 $\pm$ 48) Gy(SiO_2). The XC2S150 results show that while they absorbed less dose prior to experiencing a rise in power sup-

[‡]Whenever the operation of a device was examined the radiation was turned off.

[§]Configuration refers to the configuration of the device for the first time after the application of power to the device. Reconfiguration refers to any configuration that occurs after the initial configuration.

DUT #	Dose (Core) $Gy(SiO_2)$	Dose (I/O) $Gy(SiO_2)$
3	341 ± 59	396 ± 68
10	350 ± 60	410 ± 71
13	317 ± 55	375 ± 64
14	320 ± 55	401 ± 68

Table 7.2: The dose at which the logic core and I/O circuitry power supply current increased from the baseline value for the XC2S150 parts.

DUT #	Dose of First Error $Gy(SiO_2)$	Dose of Failure $Gy(SiO_2)$
3	623 ± 106	625 ± 107
10	481 ± 82	1010 ± 170
13	521 ± 89	532 ± 91
14	506 ± 86	519 ± 89

Table 7.3: Doses at which the XC2S150 devices began producing errors and when they ceased to function.

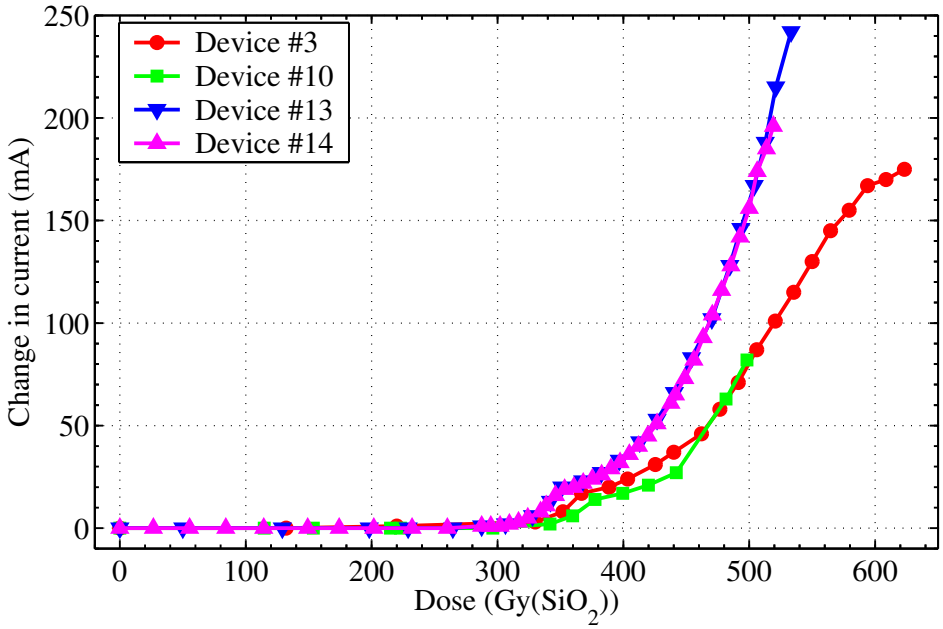


Figure 7.9: Change in power supply current for the logic core versus absorbed dose for the XC2S150 SCAC prototype.

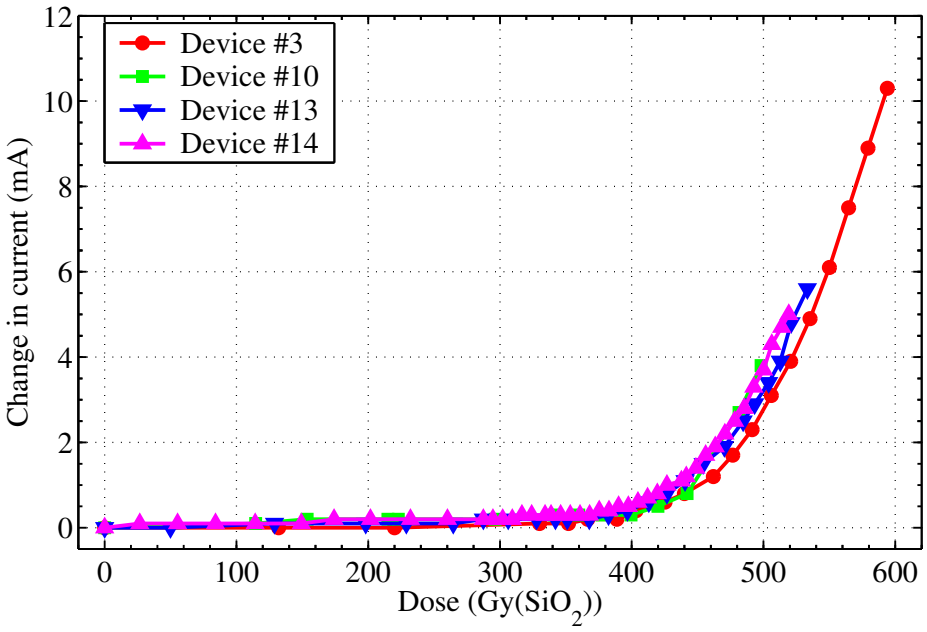


Figure 7.10: Change in power supply current for the I/O blocks versus absorbed dose for the XC2S150 SCAC prototype.

ply current, the device to device variations were much less than the EPF10K50 devices. In addition, the response of the I/O circuitry to the effects of radiation was consistent with that of the core circuitry.

7.3.4 TID Tests of the DMILL Radiation Hardened ASIC

A limited amount of TID testing was performed on the DMILL prototype SCAC. Four DMILL devices were irradiated between August and September, 2001. One device (DUT #4) was irradiated to a total ionizing dose of (1.8 $\pm$ 0.4) kGy(SiO_2) using the x-ray facility. An additional TID of (400 $\pm$ 20) Gy(Si)[¶] was absorbed by DUT #4 during irradiations of 68 MeV protons at the PIF bringing the total absorbed dose up to (2.2 $\pm$ 0.4) kGy(SiO_2) for that device. Table 7.4 lists the total doses absorbed the 4 DMILL devices irradiated with 68 MeV protons at the PIF. Device #9 had absorbed an undetermined amount of dose greater than 800 Gy(Si) as some testing was performed where the monitor counts from the PIF readout were not recorded. No increases in current drawn by the device or

[¶]The dosimetry provided by the PIF staff was for Si rather than SiO_2.

DUT #	Total Absorbed Dose Gy(Si)
4	400 ± 20
5	600 ± 30
7	340 ± 20
9	>880

Table 7.4: Total ionizing dose absorbed by the DMILL prototype during proton irradiations at the PIF. Device #9 had absorbed an undetermined amount of dose greater than 800 Gy(Si) as some testing was performed where the monitor counts from the PIF readout were not recorded.

radiation related failures were observed during or after the irradiation periods.

7.3.5 TID Tests of the DSM ASIC

Twenty-four DSM prototypes were irradiated with x-rays and protons between May and October, 2002. The evolution of the power supply current for the tests can be seen in Figures 7.13 and 7.12. The tests on devices #5, #7, #12, and #27 were performed in the 491 MeV beam-line 1B, while all of the other proton tests were performed in the high intensity position of beam-line 2C. The current readings were made at the rate of 1 Hz and fluctuated by about 0.05 mA (compared to typical readings of approximately 120 mA – Figure 7.11), which made the plots difficult to read. To account for this, the data in Figures 7.12 and 7.13 were fit with polynomials, which are the curves on the plots. The total change in current over the irradiation period for each DUT was made by averaging the first and last 60 measurements and taking their difference. The change in current for two of the x-ray irradiated devices were not plotted (DUT #93 and DUT #71) as they were irradiated to significantly higher doses and if plotted on the same scale as the other devices they would show little detail. The behaviour of the two devices was similar to that of the devices plotted in Figure 7.12, but extend to a much larger dose. Tables 7.5 and 7.6 contain the changes in power supply current drawn by the DSM devices after irradiation in the x-ray facility and PIF respectively. The average current drop per unit dose for the devices irradiated with x-rays was 0.4 mA/kGy(SiO_2) , while a value of 0.14 mA/kGy(SiO_2) was measured for the devices irradiated with protons. Two of the devices (DUT #81 and DUT #87) irradiated with x-rays were pre-stressed at elevated temperature prior to irradi-

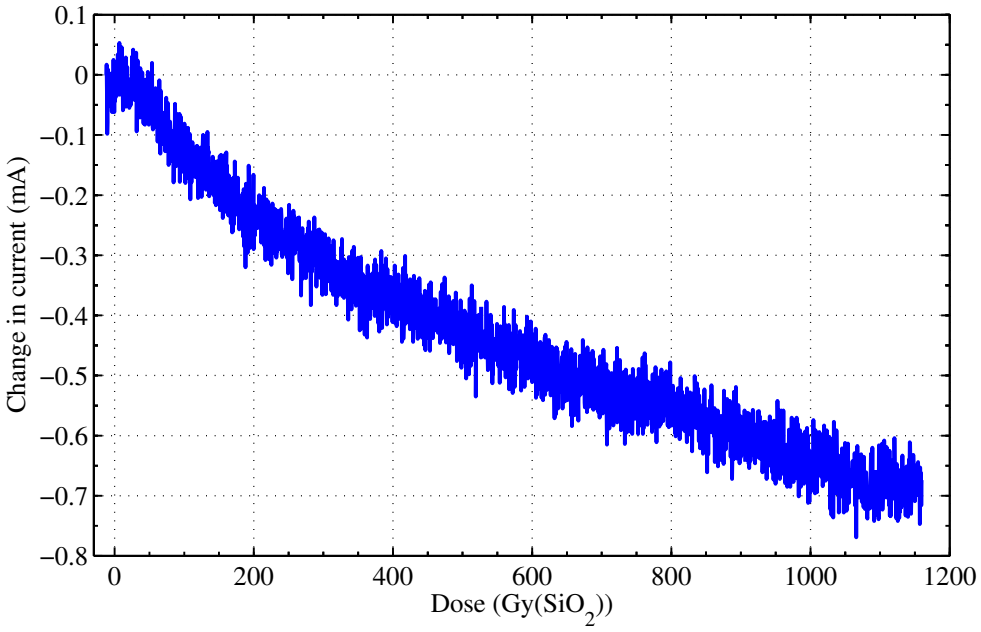


Figure 7.11: Power supply current draw by DUT #32 during X-ray irradiation.

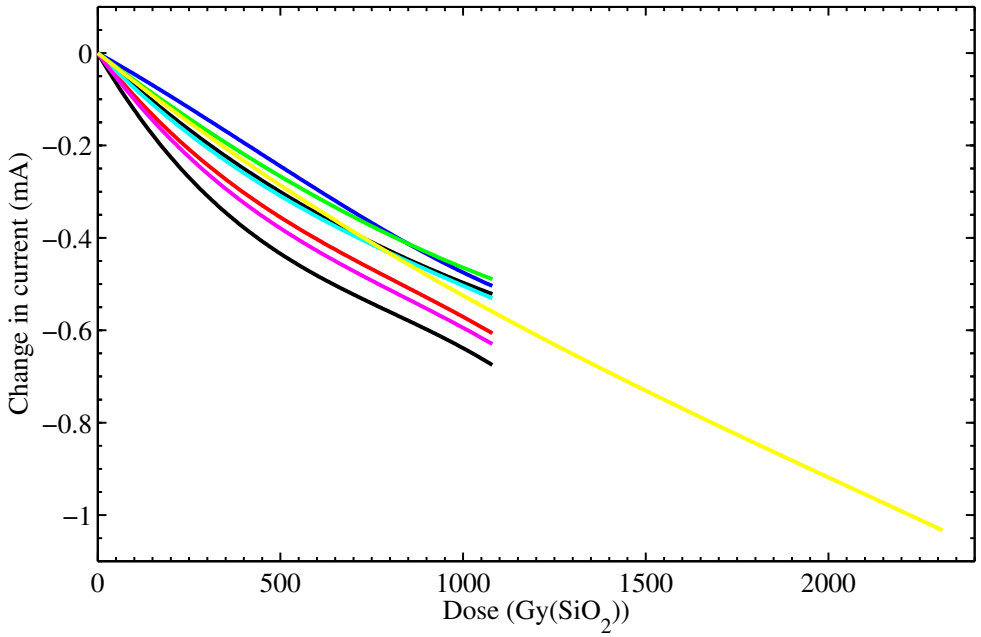


Figure 7.12: Evolution of the power supply current drawn by the DSM SCAC prototype during x-ray irradiation. From top to bottom (of the line segment ends) the devices corresponding to the curves are 58, 10, 81, 69, 87, 56, 155, and 32.

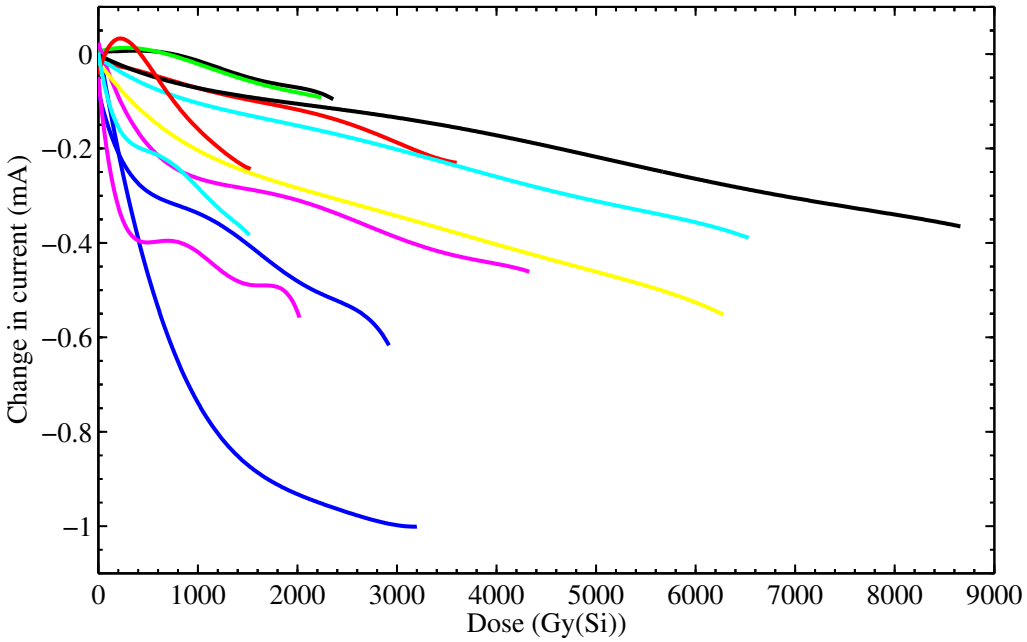


Figure 7.13: Evolution of the power supply current drawn by the DSM SCAC prototype during proton irradiation. From top to bottom (of the line segment ends) the devices corresponding to the curves are 14, 13, 49, 50, 17, 9, 51, 5, 12, 27, 38, and 34.

DUT #	TID kGy(SiO_2)	Current Change mA	%	Stress
69	1.14 $\pm$0.16	-0.5	-0.4	168 hr at 100^{o}C
56	1.14 $\pm$0.16	-0.6	-0.4	186 hr at 100^{o}C
155	1.14 $\pm$0.16	-0.6	-0.4	192 hr at 102^{o}C
58	1.14 $\pm$0.16	-0.5	-0.4	183 hr at 22^{o}C
10	1.14 $\pm$0.16	-0.6	-0.4	24 hr at 22^{o}C
32	1.14 $\pm$0.16	-0.7	-0.5	168 hr at 22^{o}C
81	1.14 $\pm$0.16	-0.5	-0.3	168 hr at 125^{o}C*
87	2.28 $\pm$0.32	-1.0	-0.7	168 hr at 125^{o}C*
82	0.38 $\pm$0.05	-0.1	-0.1	thermal test 1
82	0.76 $\pm$0.11	-0.3	-0.1	thermal test 2
93	4.56 $\pm$0.64	-1.2	-0.8	thermal test 3
71	20.00 $\pm$2.75	-4.2	-3.4	thermal test 4

Table 7.5: The effect of TID from x-rays on the DSM prototype SCAC. The tests denoted with * correspond to those where thermal pre-stressing of the device was performed.

ation to simulate accelerated aging of the device [31]. No difference in behaviour during or after irradiation was observed for these devices. Thermal tests, where the temperature during irradiation was monitored, were performed on DUTs #71, #82, and #93, so that the relative effects of radiation and temperature on the devices could be understood [98].

A reduction in drawn current was observed for all devices. About 30% of the reduction can be explained as an effect of the device becoming heated by the radiation [98, 99]. The remainder of the reduction in current might be explained by considering the nature of the DSM device. The enclosed transistors and guard rings prevent leakage currents and the thin oxide prevents bulk oxide charge build-up, but charge will still become trapped at the interface between the oxide layer and the semiconductor. The trapped interface charges will push the threshold voltage lower for the PMOS transistors and higher for the NMOS transistors. The net effect of the threshold voltage shifts will be a smaller voltage "swing" between the ON states of the NMOS and PMOS transistors that make up CMOS devices. The switching time for the device will decrease with the decrease in voltage swing, and both types of transistor will be in the OFF state for a larger portion of the time [99], thus reducing the current drawn. Irradiations to doses of approximately 80 kGy(Si) have not

DUT #	TID kGy(SiO_2)	Current Change mA	%	Annealing Time (no bias applied)
49	10.30 ±1.08	-0.5	-0.3	47 days
50	6.63 ±0.22	-0.4	-0.3	47 days
51	6.63 ±0.22	-0.5	-0.4	47 days
38	4.10 ±0.14	-0.5	-0.3	47 days
17	3.64 ±0.27	-0.2	-0.2	47 days
34	3.22 ±0.24	-1.0	-0.7	47 days
13	2.70 ±0.19	-0.1	-0.1	47 days
14	2.67 ±0.19	-0.1	-0.1	47 days
5	5.90 ±0.30	-0.6	-0.4	none
9	3.09 ±0.15	-0.2	-0.2	none
12	3.09 ±0.15	-0.4	-0.3	none
27	4.12 ±0.21	-0.5	-0.3	none

Table 7.6: The effect of TID from proton irradiations on the DSM prototype SCAC.

shown failures or current change rates of larger magnitude than those described in this chapter [100].

7.4 Discussion of TID Test Results

The ASIC SCAC prototypes were not affected beyond the point where they would not function correctly during or after irradiations to total absorbed doses of up to
(20 ± 5) kGy(SiO_2) for the DSM prototype and (2.2 ± 0.4) kGy(SiO_2) for the DMILL prototype. The COTS prototypes experienced increases in power supply current at much lower doses than those that the ASICs were irradiated to. The EPF10K50 device began to exhibit increases in power supply current to its core circuitry at an average dose of (832 ± 90) Gy(SiO_2) . The power supply current drawn by the core and I/O circuitry of the XC2S150 began to increase at an average dose of (331 ± 29) Gy(SiO_2) and (395 ± 34) Gy(SiO_2) respectively. These values were similar in order of magnitude to those absorbed by two types of Xilinx FPGAs during similar tests in the ^{60}Co facility. The XC4036XL and XC4036XLA devices absorbed (384 ± 15) Gy(SiO_2) and (155 ± 30) Gy(SiO_2)

respectively prior to an increase in power supply current [86]. Comparing the average TIDs absorbed by the XC2S150 prototype[‖], prior to an increase in drawn current and the first error, to the SRL_{TID} in the SCAC region (3.94 Gy(SiO_2)), it can be estimated that the device would operate in ATLAS with no increase in current and no errors for 84 yr and 133 yr respectively. The same estimates can be made for the EPF10K50 using the average TID absorbed in the logic core prior to a current increase and the point at which DUT #5 began producing errors. Comparing these doses with the SRL_{TID} in the SCAC region it was estimated that the EPF10K50 would show no increase in drawn current for 380 yr and would not produce errors for 210 yr of operation within ATLAS.

It was not surprising that there were differences in TID tolerance between the ASIC and the COTS devices but the reason for the differences between the various COTS devices is not obvious. There are fundamental differences between CPLDs and FPGAs, such as the complexity of the programmable logic blocks (Chapter 3). For example, the EPF10K50 CPLD had large areas of the logic blocks dedicated to implementing large mega-functions (Chapter 6), while the XC2S150 was composed of a greater number of smaller functional blocks. The layout of the circuitry could lead to differences in radiation hardness [101] between the two devices. The layout can have a significant impact on leakage paths between transistors for example. The difference in radiation hardness between the two FPGAs from the same company could possibly be explained in the same manner. The XC4036XLA and XC2S150 devices are derived from different families and one significant difference between the two is the manner in which the RAM was designed. It is conceivable that with the reduced feature size between the two devices and a different approach to RAM layout, increased leakage current could result. This would explain the lower radiation tolerance for the XC2S150, although it had a smaller feature size.

There was no current change observed in either the I/O blocks or the logic core during ^{60}Co irradiations of the EPF10K50. It appears as there were electrical problems associated with the testing of the device which were never completely understood. All that could be ascertained was that radiation damage had occurred during each of the ^{60}Co tests. The dose at which the damage occurred was not known. During x-ray irradiation no current increase in the I/O circuitry of the device was observed and it is plausible that

[‖]The doses prior to current increases for the logic core were used as they were slightly less on average than those for the I/O logic.

this was also due to an electrical problem. The results of the EPF10K50 showed a larger variation in the manner in which the power supply current changed during irradiation than the XC2S150 device but appeared to be more radiation tolerant, to TID effects, than the XC2S150 or either of the XC4036 FPGAs tested previously.

A slight decrease in power supply current, about 0.4 mA/kGy(SiO_2) in x-rays, was observed for the DSM SCAC prototype device. The average change in current drawn by the device per unit of TID can be compared with the SRL_{TID} to estimate that after 10 years of contiguous operation in ATLAS, the device would draw roughly 15 μA less current than at the start. This slight decrease would not cause problems for the DSM device if it were used in the ATLAS detector. This decrease was interesting, however, as it demonstrated an effect of the use of enclosed transistors.

Chapter 8

Tests for Single-Event Effects

Following the procedures in the ATLAS LAr electronics radiation tolerance policy, candidate devices were tested for soft, hard, and damaging SEEs. Devices were irradiated to study all of these SEEs using the TRIUMF PIF. The proton-induced SEU cross-section was measured for proton energies between 20 MeV and 491 MeV (Section 8.2). This cross-section allowed the upset rate for the devices operating in ATLAS to be estimated. Due to the limited availability of the PIF, not all of the COTS prototypes were tested for SEEs. Several of the DSM devices were tested for displacement effects at the PS/IRRAD2 facility [102] at CERN and the results of those tests are also discussed in this chapter.

8.1 Arrangement for SEE Tests Performed at the PIF

The method used for the SEE tests was basically the same as that used for the TID tests. Bias voltage was applied to the DUTs and they were operated at 40 MHz as they would in ATLAS. The current was monitored during the irradiations such that any TID effects or permanent SEEs, such as latch-up, could be observed. A 1 A fuse was installed between the DUT and the power supply on the XC4036XLA and DMILL test boards. The voltage to the DSM DUT was controlled using voltage regulators on the DSM monitor board.

A major difference between the PIF and photon facilities was that at the PIF the radiation levels dropped off significantly from the location of the beam (Figure 5.8). It was thus possible to allow the placement of a portion of the test system inside the radiation area at the PIF. This was necessary as the distance between the DAQ computer and the DUT was about 30 m, which was too long for reliable communication. Figure 8.1 shows the layout

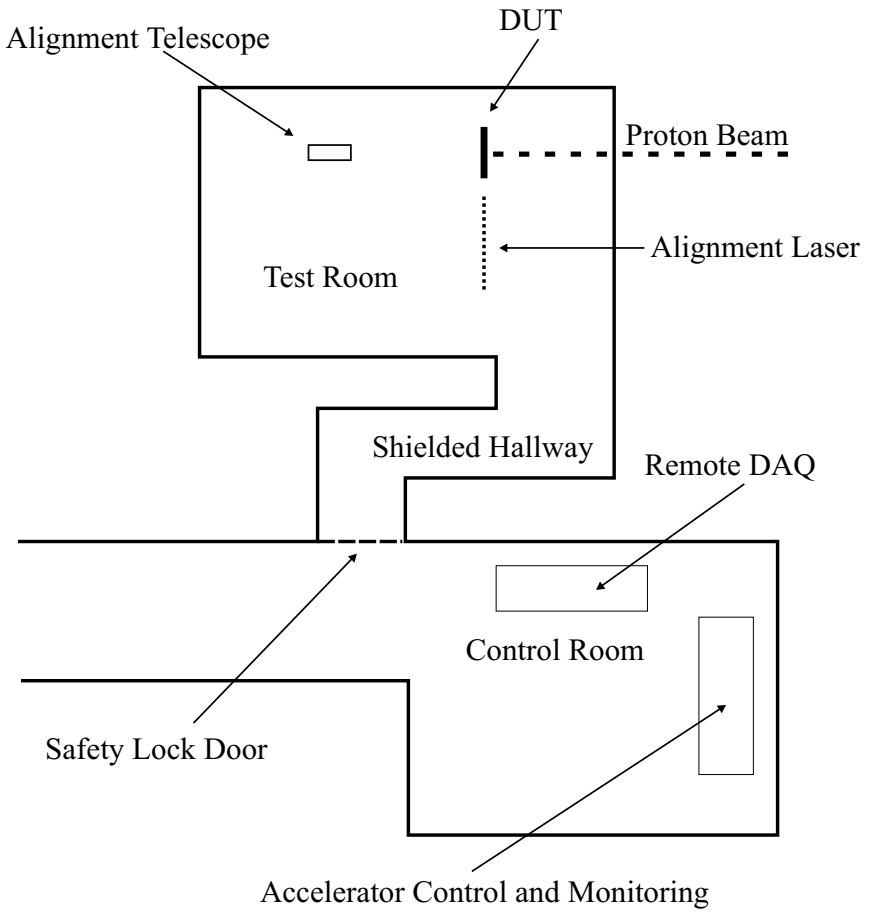


Figure 8.1: Test arrangement at the TRIUMF Proton Irradiation Facility showing the proton beam and device alignment in beam-line BL2C.

of the PIF test area and the relative placement of the test board. The figure also shows the laser and telescope that were used to align the DUT in the proton beam (beam-line 2C).

As with the TID tests, two configurations were used for the PIF tests. The first of these test configurations is depicted in Figure 8.2. This configuration was only used for the XC4026XLA PIF tests. Communication between the DAQ computer in the radiation area and the monitor computer in the control room via an ethernet connection was used as there was concern that 30 m would be too far to reliably transmit signals on a parallel cable. A second configuration was used for the tests of the DMILL and DSM ASIC prototypes and is shown in Figure 8.3. The second configuration was motivated by the desire to have access to the power supplies so that the power to the test system could be cycled

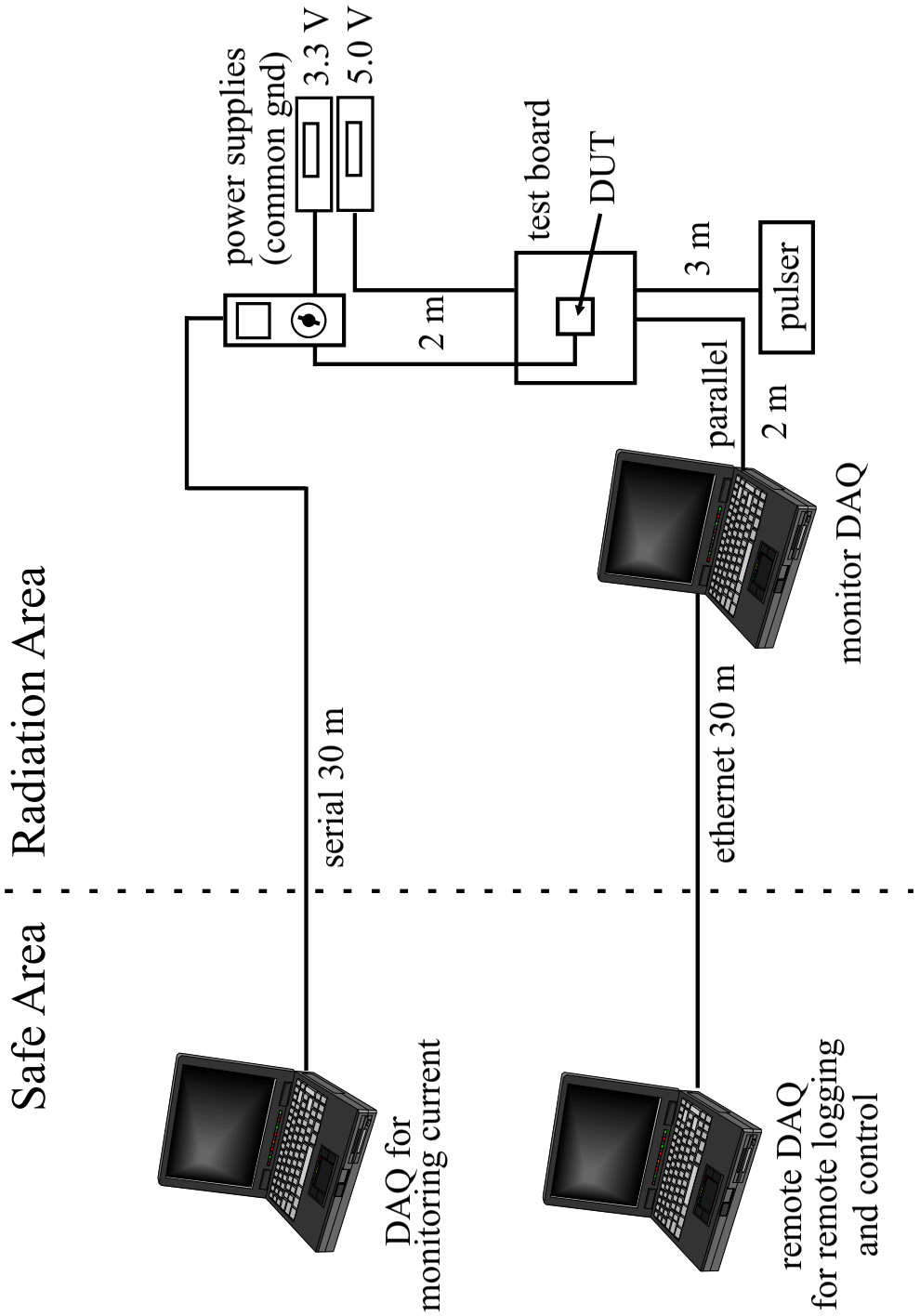


Figure 8.2: Test setup used for the proton irradiations of the XC4036XLA prototype.

if necessary without having to access the radiation area, as would be the case to correct a hard SEE. The system pictured in Figure 8.3 was that used for the DSM tests and slight differences existed between it and the system used for the DMILL test. The DMILL system required additional power supplies and the cable lengths were slightly different. For all of the tests a remote control camera was used to monitor the test area from the control room. The camera was used to monitor the power supply voltages and currents*, as well as to monitor LEDs on the test and monitor boards for the tests.

Each DUT was mounted in the proton beam with its top perpendicular to the beam axis. A laser was used to align the DUT with the point along the beam where calibrations had been carried out. A telescope located behind the movable beam stop was used to center the DUT in the beam. Figures 8.1 and 8.4 show a schematic and photograph of the test board placement in beam-line 2C. Using an adjustable collimator, the beam diameter was set such that the beam completely covered the die of the device (i.e., the beam diameter was set to approximately 25 mm for the XC4036XLA and DMILL devices). This was done to ensure that the flux was uniform over the die of the device. As an additional step to ensure that the proton flux was as uniform as possible for the XC4036XLA device the top of the snap-down socket was removed (Figure 8.5). The socket used on the DSM test board had no material above the DUT so no modification was required. The socket used on the DMILL test board was similar to that used on the XC4036XLA test board (Figure 7.1) but was slightly smaller. A decision was made not to modify the socket; instead the DMILL device was irradiated through the back side of the PC board.

8.2 Proton-Induced SEU Cross-Section of the XC4036XLA Prototype

The XC4036XLA device was irradiated with protons on three separate occasions: June 1999, October 1999, and June 2000. The first two periods were used to determine if the device was susceptible to the effects of proton irradiation, and to develop a reliable test procedure. Increasing amounts of data were taken during each subsequent test period. During the test performed between June 12th and June 14th, 2002, six XC4036XLA pro-

*The power supply currents for the DSM device and monitor board were monitored by a digital multimeter.

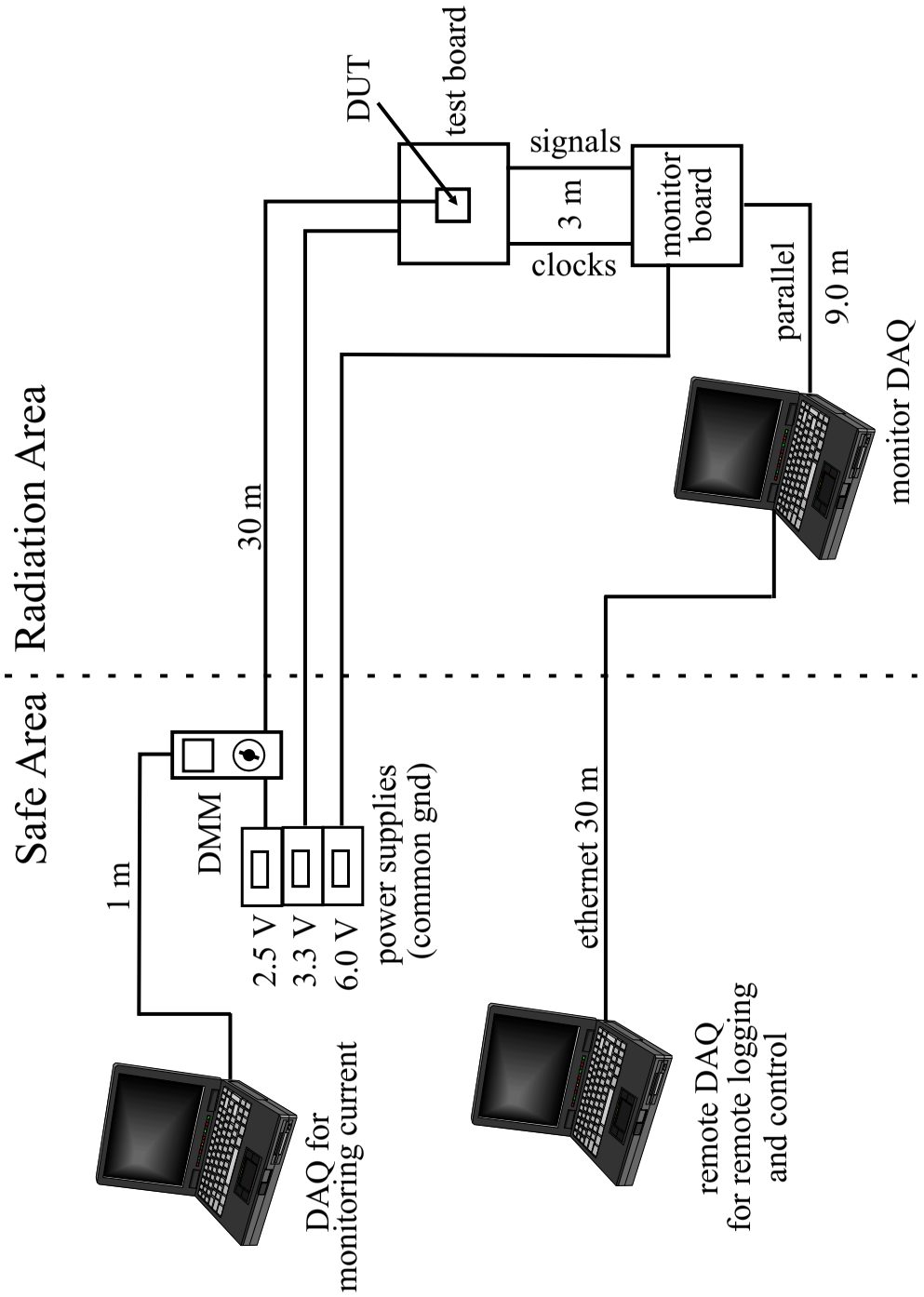


Figure 8.3: Test setup used for the proton irradiations of the DSM and DMILL prototypes.

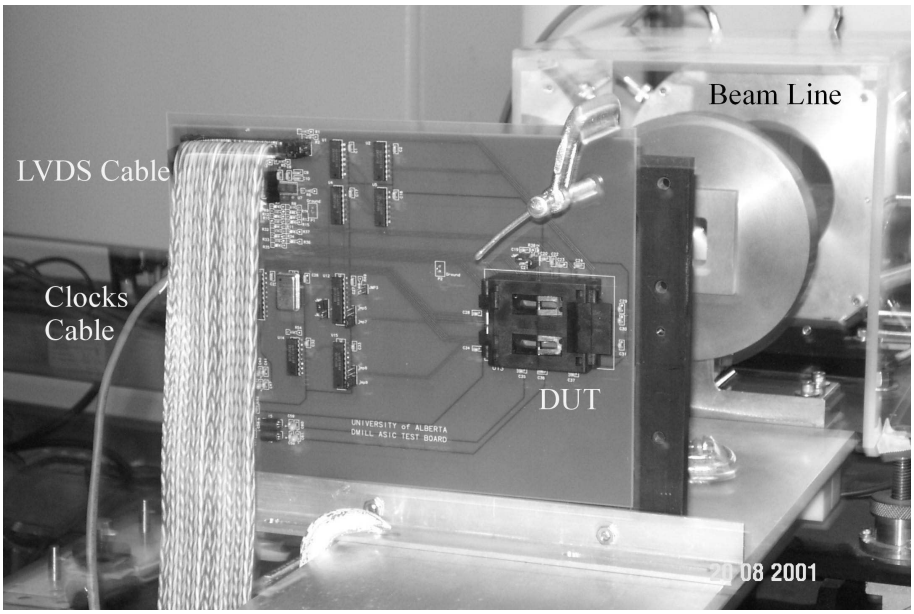


Figure 8.4: Photograph of the test board, *in situ*, used for the proton irradiations of the DMILL prototype SCAC showing the cables that carried the clock and LVDS signals. The proton beam entered the device from the back side of the board.

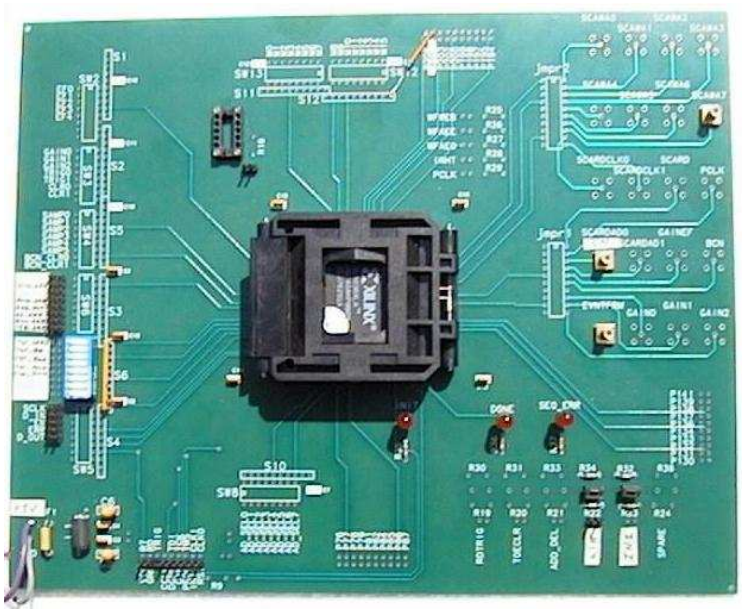


Figure 8.5: Photograph showing the test board and modified socket for the XC4036XLA test system.

totype SCACs were irradiated in order to obtain a proton-induced SEU cross-section at 10 proton energies between 18 MeV and 105 MeV. It should be noted that it was not expected that there would be much device-to-device variation as the fabrication processes were well controlled and thus it should be acceptable to use more than one device when collecting a data point for the SEU cross-section.

The proton beam contained a small degree of neutron contamination, but the neutron fluence, integrated over all energies, had been measured to be about 10^{-5} of the proton fluence at 70 MeV [90], and thus the radiation effects on the devices due to the neutrons were neglected.

The proton induced SEU cross-section is, by definition,

$$\sigma = \frac{N_o}{\Phi}, \tag{8.1}$$

where N_o is the number of proton-induced upsets and Φ is the proton fluence during the irradiation period. As described in the Section 7.1, when an upset could not be cleared after a reset was issued three times, the circuit was reconfigured by the monitoring program on the DAQ computer. This process introduced a deadtime of (8 ± 1) s. During this time the system was incapable of detecting any upsets. The deadtime causes the cross-section calculated from equation 8.1 to be underestimated. A correction was required to account for any missed upsets. Resetting the circuit took much less than a second and it was determined that the probability of an upset coming during a circuit reset was less than 10^{-6}.

8.2.1 Deadtime Correction

The method used for correcting the cross-section for missed upsets was to increase the observed number of upsets by an estimate of the number missed. The first step was to determine which upsets required the DUT to be reconfigured and were thus responsible for deadtime. Table 8.1 contains the number of upsets observed that required the DUT to be reconfigured, as well as those that simply required resets.

It was possible to measure the number of proton-induced SEUs for the circuit and configuration switches separately. This was because SEUs occurring in the switches could not be cleared by a reset. The SEU cross-section for each could then be calculated by

DUT #	Energy (MeV)	Fluence ($10^{10}\mathrm{cm}^{-2}$)	Upsets	
			Switch	Circuit
4	18.0 ± 2.1	$3.70 \pm 0.40 \pm 0.19$	$17^{+4.8}_{-4.2}$	$1^{+1.8}_{-0.6}$
3	20.0 ± 1.8	$5.94 \pm 0.59 \pm 0.30$	$46^{+7.3}_{-6.7}$	$1^{+1.8}_{-0.6}$
2	26.9 ± 1.5	$2.73 \pm 0.11 \pm 0.14$	$48^{+7.3}_{-6.7}$	$4^{+2.8}_{-1.7}$
2	35.4 ± 1.1	$4.66 \pm 0.07 \pm 0.23$	$100^{+10.8}_{-9.7}$	$8^{+3.3}_{-2.7}$
2	57.7 ± 0.6	$4.07 \pm 0.07 \pm 0.20$	$101^{+10.8}_{-10.2}$	$0^{+1.3}_{-0.0}$
6	75.6 ± 1.1	$3.77 \pm 0.26 \pm 0.19$	$88^{+9.8}_{-9.2}$	$3^{+2.3}_{-1.9}$
6	85.5 ± 1.0	$4.94 \pm 0.33 \pm 0.25$	$95^{+10.3}_{-9.7}$	$2^{+2.3}_{-1.3}$
1	94.7 ± 0.8	$4.28 \pm 0.32 \pm 0.21$	$91^{+10.3}_{-9.7}$	$7^{+3.3}_{-2.7}$
6	101.5 ± 0.8	$3.42 \pm 0.23 \pm 0.17$	$95^{+10.3}_{-9.7}$	$6^{+3.3}_{-2.2}$
6	105.0 ± 0.7	$3.97 \pm 0.26 \pm 0.20$	$91^{+10.3}_{-9.7}$	$4^{+2.8}_{-1.7}$

Table 8.1: Proton fluence and number of single-event upsets observed at each proton energy. The first uncertainty in the fluence is that due to dosimetry while the second is due to flux uniformity over the die.

making the appropriate substitution of the corresponding number of upsets N into equation 8.1. The uncertainties in the observed number of upsets were calculated by constructing 68.27% confidence interval belts for a Poisson probability distribution function following the method described in Ref. [103].

The observed number of upsets, N_o, would be smaller than the actual number N_a by the amount of upsets that would have occurred during the deadtime. Figure 8.6 shows the theoretical probability of one or more upsets occurring during the configuration time as a function of mean time between errors. For example, it can be seen that in order to keep the probability of an upset coming during configuration below 20% – the maximum uncertainty that could have been accepted, the mean time between upsets would have to be kept above about 35 s. This could be achieved by reducing the beam flux during irradiations. Consequently, Figure 8.6 was used to estimate the length of irradiation time that would be required for the test.

The correction to the observed number of upsets involved the deadtime, as well as the mean time between upsets. Therefore a different correction was required for the upsets occurring in the circuit than for those occurring in the switches. The corrected number of

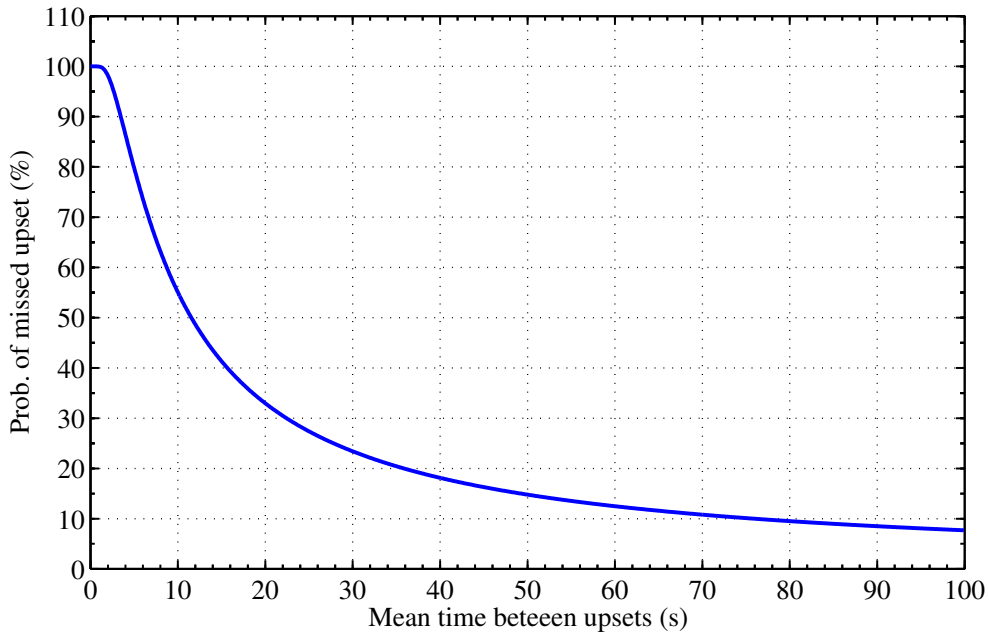


Figure 8.6: Probability of upset occurring during reconfiguration. The function is a Poisson distribution with the number of observed events greater than 0, and a deadtime of 8 seconds.

Energy (MeV)	Upsets		Cross-section (10^{-10}cm^2/device)	
	Switch	Circuit	Switch	Circuit
18.0 ± 2.1	$18.5^{+5.2}_{-4.6} \pm 0.4$	$1.1^{+1.8}_{-0.6} \pm 0.1$	$5.0^{+1.4}_{-1.2} \pm 0.6$	$0.30^{+0.47}_{-0.17} \pm 0.04$
20.0 ± 1.8	$50.9^{+8.1}_{-7.4} \pm 0.9$	$1.7^{+1.8}_{-0.6} \pm 0.7$	$8.6^{+1.4}_{-1.3} \pm 1.0$	$0.29^{+0.32}_{-0.16} \pm 0.03$
26.9 ± 1.5	$57.9^{+8.8}_{-8.1} \pm 1.9$	$6.8^{+2.8}_{-1.7} \pm 1.8$	$21.2^{+3.3}_{-3.0} \pm 1.4$	$2.50^{+1.22}_{-0.92} \pm 0.16$
35.4 ± 1.1	$112.5^{+12.2}_{-10.9} \pm 1.9$	$9.5^{+3.3}_{-2.7} \pm 1.0$	$24.1^{+2.6}_{-2.4} \pm 1.3$	$2.04^{+0.74}_{-0.62} \pm 0.11$
57.7 ± 0.6	$110.9^{+11.9}_{-11.2} \pm 1.6$		$27.2^{+2.9}_{-2.8} \pm 1.4$	
75.6 ± 1.1	$100.7^{+11.2}_{-10.5} \pm 2.1$	$5.2^{+2.3}_{-1.9} \pm 0.9$	$26.7^{+3.0}_{-2.8} \pm 2.2$	$1.38^{+0.66}_{-0.56} \pm 0.12$
85.5 ± 1.0	$106.9^{+11.6}_{-10.9} \pm 2.0$	$2.6^{+2.3}_{-1.3} \pm 0.4$	$21.6^{+2.4}_{-2.2} \pm 1.8$	$0.53^{+0.46}_{-0.27} \pm 0.04$
94.7 ± 0.8	$102.9^{+11.7}_{-11.0} \pm 2.0$	$8.4^{+3.3}_{-2.8} \pm 0.7$	$24.1^{+2.8}_{-2.6} \pm 2.1$	$1.96^{+0.79}_{-0.66} \pm 0.18$
101.5 ± 0.8	$109.0^{+11.8}_{-11.1} \pm 2.1$	$7.2^{+3.3}_{-2.2} \pm 0.7$	$31.8^{+3.5}_{-3.3} \pm 2.7$	$2.09^{+0.98}_{-0.67} \pm 0.17$
105.0 ± 0.7	$106.9^{+12.1}_{-11.4} \pm 2.5$	$6.6^{+2.8}_{-1.7} \pm 2.2$	$26.9^{+3.1}_{-2.9} \pm 2.2$	$1.67^{+0.90}_{-0.70} \pm 0.14$

Table 8.2: Dead-time corrected number of upsets and single-event upset cross-sections per device at each proton energy.

upsets are given in Table 8.2[†]. The expression for the actual number of upsets occurring in the configuration switches was given by

$$N_a^{sw} = N_o^{sw}(1 + C^{sw}), \tag{8.2}$$

where C^{sw} was the deadtime correction factor that accounted for the number of switch upsets not detected during reconfigurations of the FPGA. The expression for the actual number of upsets occurring in the circuit was given, to first order, by

$$N_a^{cir} = N_o^{cir} + C^{cir} N_o^{sw}, \tag{8.3}$$

where C^{cir} was the deadtime correction factor for the circuit upsets. The correction factor was the fractional deadtime $\tau/\Delta t$, where τ was the deadtime of 8 s and Δt was the mean time between upsets in the switches. The correction to the number of upsets in the circuit used the mean time between upsets observed in the circuit. The uncertainties for the actual numbers of switch and circuit upsets were obtained by propagation of errors. The distribution of times between switch upsets is shown in Figure 8.7. The data have been normalized and fit with an exponential probability distribution function, which naturally

[†]In this thesis, when two uncertainties are quoted, the first will be the statistical uncertainty and the second will be the systematic uncertainty, unless stated otherwise.

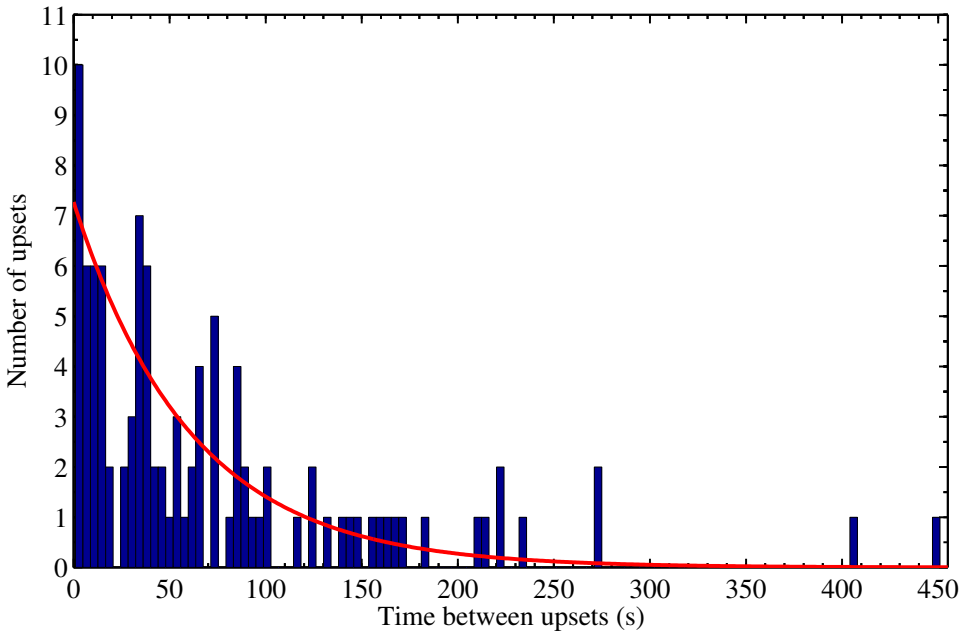


Figure 8.7: Exponential distribution fit to normalized histogram of time between errors for the data taken at 57.7 MeV for the XC4036XLA SCAC prototype. The deadtime of 8 s has been subtracted off the times.

describes the distribution of times between failures in composite systems [104]. The data were consistent with the exponential distribution. Due to the limited number of events the geometric mean and standard deviation were used to extract the mean time between upsets rather than the parameters from the fits to the exponential distribution. The results are tabulated in Table 8.3. The second order effect of the mean being skewed by the missing data below 8 s has been neglected. For the two energies where only one upset in the circuit was observed, 100% of the value was taken as the uncertainty. The correct cross-sections could then be calculated using the corrected number of upsets and the proton fluence (Table 8.2). The fluences, and related uncertainties, were calculated from the number of monitor counts measured during the tests. The conversion factor was provided at the test facility and is described in Section 5.4.

8.2.2 Alternative Method for a Deadtime Correction

Using an alternative method it should be possible to obtain the same deadtime correction to the cross-section described in the previous section. Rather than correcting for the

Energy (MeV)	Mean Time Between Switch Upsets (s)	Mean Time Between Circuit Upsets (s)
18.0	92.9 ± 23.5	1140.0 ± 1140.0
20.0	74.6 ± 8.9	525.0 ± 525.0
26.9	38.6 ± 5.8	135.3 ± 85.6
35.4	64.0 ± 5.9	526.4 ± 327.9
57.7	81.9 ± 8.2	N/A
75.6	55.6 ± 6.0	317.0 ± 121.9
85.5	64.1 ± 7.2	1236.5 ± 845.5
94.7	61.1 ± 6.5	517.3 ± 248.4
101.5	54.3 ± 4.7	654.8 ± 369.7
105.0	45.9 ± 4.5	277.3 ± 231.1

Table 8.3: Mean time between upsets for each type of upset and energy for the XC4036XLA SCAC prototype. No upset was observed in the circuit for the 57.7 MeV proton energy.

number of upsets missed during a deadtime period, the fluence could be corrected by omitting the protons incident on the device during deadtime in the calculation. The SEU cross-section can be written as

$$\sigma = \frac{N_o}{\phi t_{live}}, \tag{8.4}$$

where ϕ is the mean proton flux during the time the system was able to detect upsets (live-time t_{live}). This method required accurate measurements of t_{live}, which can be estimated using

$$t_{live} = t_{total} - N_o^{sw}\tau, \tag{8.5}$$

where t_{total} is the time elapsed during the proton irradiation of the device. Using this method, results were obtained that were consistent with those calculated in the previous section. It was not possible to use this method to obtain results with higher degree of precision than those in the previous section as the total time of each irradiation period was only known with an accuracy of 30 s and flux drifted during the irradiation periods at each energy. The latter can clearly be seen in Figure 8.8 where the upset number is plotted as a function of the irradiation time. As the proton induced SEU cross-section is defined to be a constant value at any particular energy (equation 8.1), changes in flux will appear as changes in the slope of the data in Figure 8.8[‡]. The slope will only be constant

[‡]The flux was not continuously measured at the PIF

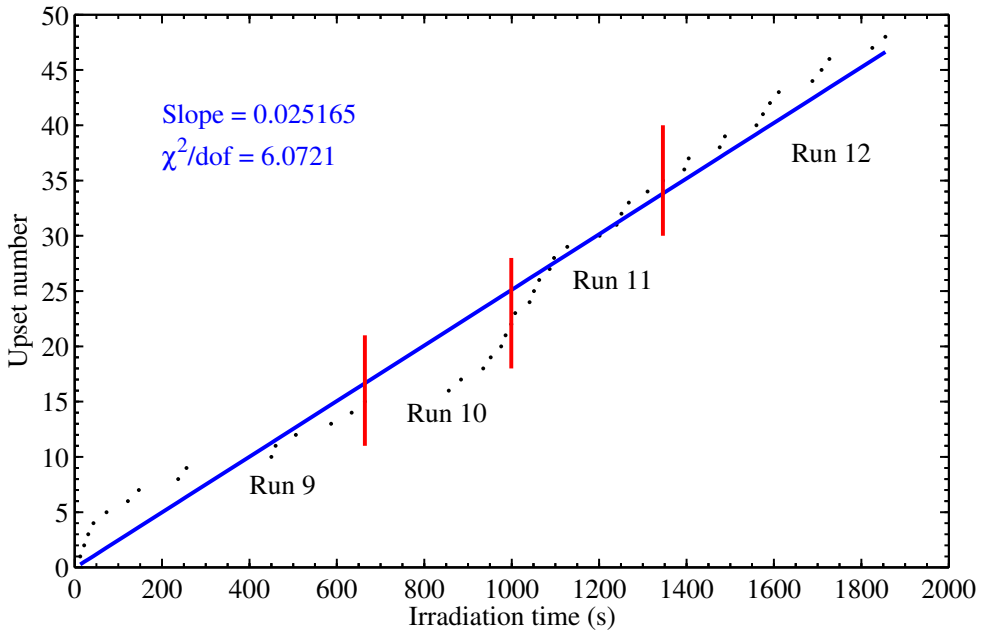


Figure 8.8: The upset number plotted against the time of upset (dots) for the XC4036XLA device irradiated with 26.9 MeV protons. A linear fit to the data, with the intercept forced to the origin, is superimposed on the plot.

within statistical fluctuations for irradiation periods where the flux was constant.

Table 8.2 shows the dead-time corrected switch and circuit upsets and the corresponding cross-sections. No circuit upsets were observed at 57.7 MeV. Since it was not possible to apply the dead-time correction procedure to this non-observation and estimate a corresponding error, this data point has been dropped from further analysis. As will be seen, the onset of saturation of the upset cross-section occurs well before 57.7 MeV and the non-observation of upsets at this energy is not likely to represent new physics, but rather a downward statistical fluctuation. The cross-sections for the switches, circuit, and total device, plotted against the proton energy, are shown in Figures 8.9, 8.10, and 8.11, respectively. The total proton-induced SEU cross-section was calculated using the sum of the switch and circuit upsets.

8.2.3 Fits of the XC4036XLA SEU Data to Empirical Reliability Functions

The proton-induced SEU measured cross-sections were measured for proton energies between 18 MeV and 105 MeV compared to the proton spectrum in ATLAS (Figure 2.11), which roughly covered the proton energy range between 1 MeV and 10 GeV. It was thus important to find a functional form that represented the data and could be extrapolated over the full ATLAS proton energy range such that estimates of SEU rates could be made for devices residing within the ATLAS detector. The data were fit with two empirical reliability functions. No analytic closed-form model based fully on physical principles exists, primarily due to the fact that proprietary device process rules play a major role in the models.

It has been shown [105, 106] that empirical reliability functions, specifically the Weibull and log-normal cumulative distribution functions (CDFs), can be used to model the lives of composite systems that fail due to fatigue or stress.

The Weibull CDF has been commonly used to model the proton-induced SEU cross-section, primarily due to its use in describing heavy-ion-induced SEU cross-sections. It has a functional form given by

$$\begin{array}{rcll} \sigma(E) & = & \sigma_{\mathrm{sat}} \left\{ 1 - \exp\left[- \left(\frac{E - E_0}{W} \right)^S \right] \right\} & \text{for} \quad E > E_0 \quad \text{and} \\ & = & 0 & \text{for} \quad E \leq E_0 \quad , \end{array} \tag{8.6}$$

where σ_{sat} is the asymptotic value of the cross-section for large energies, E_0 is the value of the energy at zero cross-section, W is a width parameter and S is a shape parameter. Table 8.4 shows the fit parameters for the Weibull CDF to the XC4036XLA data. The threshold energy, or energy value when the cross-section has fallen to half of its maximum value, for the Weibull CDF is given by

$$E_{th} = E_0 + W(\ln 2)^{\frac{1}{S}}. \tag{8.7}$$

The uncertainty in E_{th} was determined by propagating the elements of the full error matrix for the fit parameters E_0, W, and S, using the partial derivatives of equation 8.7.

An alternative empirical reliability model is the log-normal CDF, which is given in terms of the error function, erf, and complementary error function, erfc, as

$$\begin{array}{rcll} \sigma(E) & = & \frac{1}{2}\sigma_{\mathrm{sat}} \left[1 + \mathrm{erf}(z) \right] & \text{for} \quad z \geq 0 \quad \text{and} \\ & = & \frac{1}{2}\sigma_{\mathrm{sat}} \mathrm{erfc}(-z) & \text{for} \quad z < 0 \quad , \end{array} \tag{8.8}$$

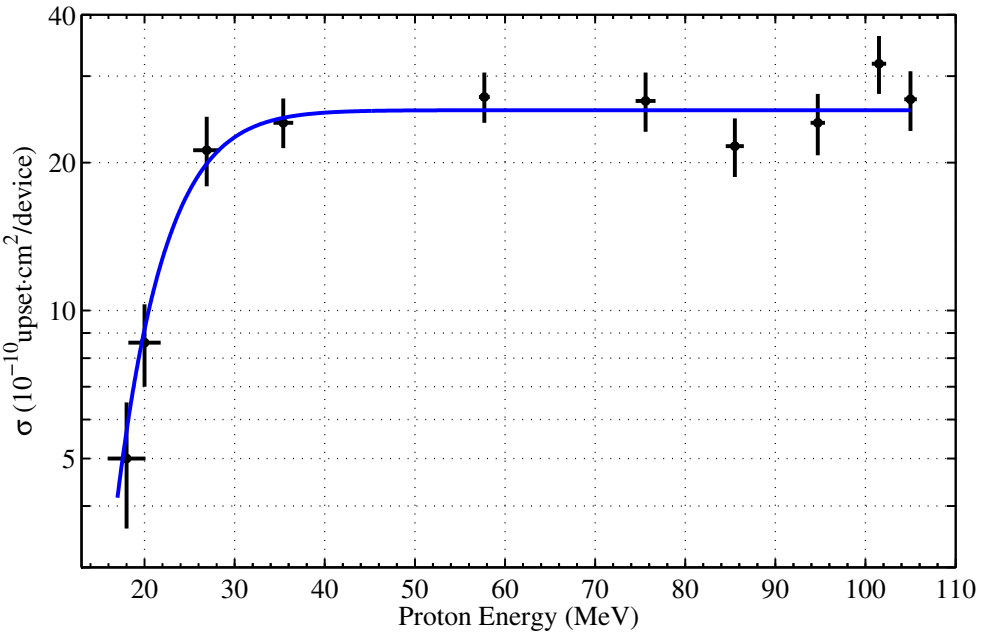


Figure 8.9: Proton induced single-event upset cross-section for the configuration switches of the XC4036XLA device.

where

$$z = \frac{\ln E - \ln E_0}{\sqrt{2}\ln W}, \tag{8.9}$$

and $\ln E_0$ is the mean of $\ln E$ and $\ln W$ is the standard deviation of $\ln E$. The threshold energy and saturation cross-section obtained from the fit parameters are listed in Table 8.5[§]. The log-normal CDF fits corresponding to Table 8.5 are shown on the plots in Figures 8.9, 8.10, and 8.11. Table 8.6 shows the threshold energy and saturation cross-section obtained using each of the reliability models. While there is agreement between parameters for the two models, there is a significantly larger uncertainty in the threshold energy determined from the Weibull CDF model. It can also be seen by comparing the correlation matrices for the Weibull CDF ($\mathbf{M_w}$) and log-normal CDF ($\mathbf{M_{ln}}$), Tables 8.10 and 8.11

[§]The fits made to the data were made using the MIGRAD minimization algorithm within the CERN minuit package [107]. Due to the relatively small amount of data used in the fits and large uncertainties in some of the data, convergence was quite sensitive to initial parameter values and there was concern that the parameter space might have a shape that could prevent a unique (global) minimum from being found. To examine this possibility a stochastic minimization routine, fast simulated annealing [108, 109, 110], was used. A goodness-of-fit criteria (reduced χ^2/dof) common to both methods was minimized and agreement was found between the two methods thus verifying that the global minimum had indeed been found. The simulated annealing method was abandoned in favour of the MIGRAD routine for convenience.

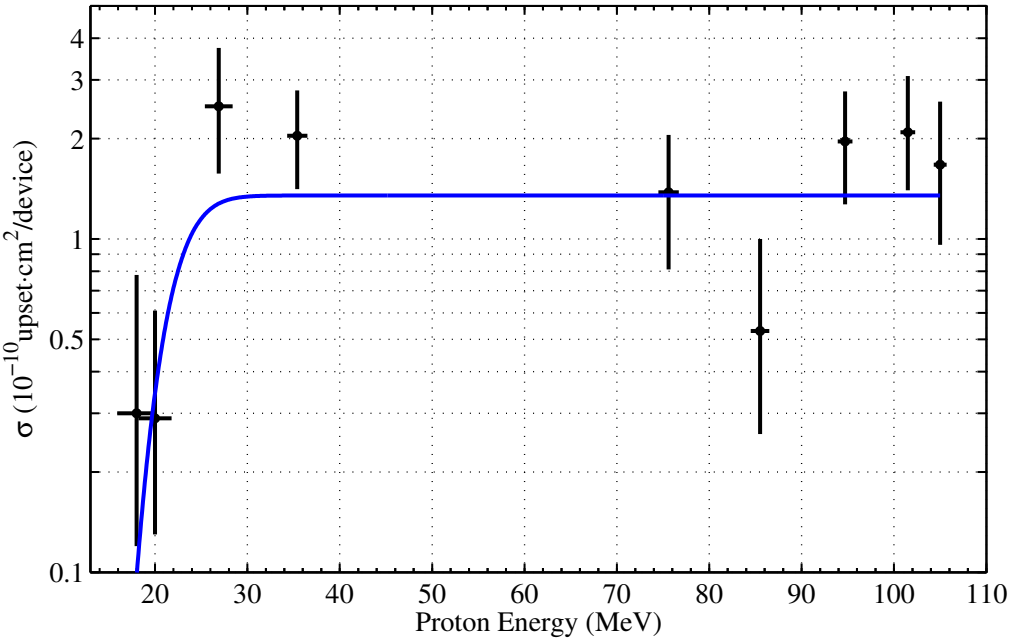


Figure 8.10: Proton induced single-event upset cross-section for the circuit of the XC4036XLA device.

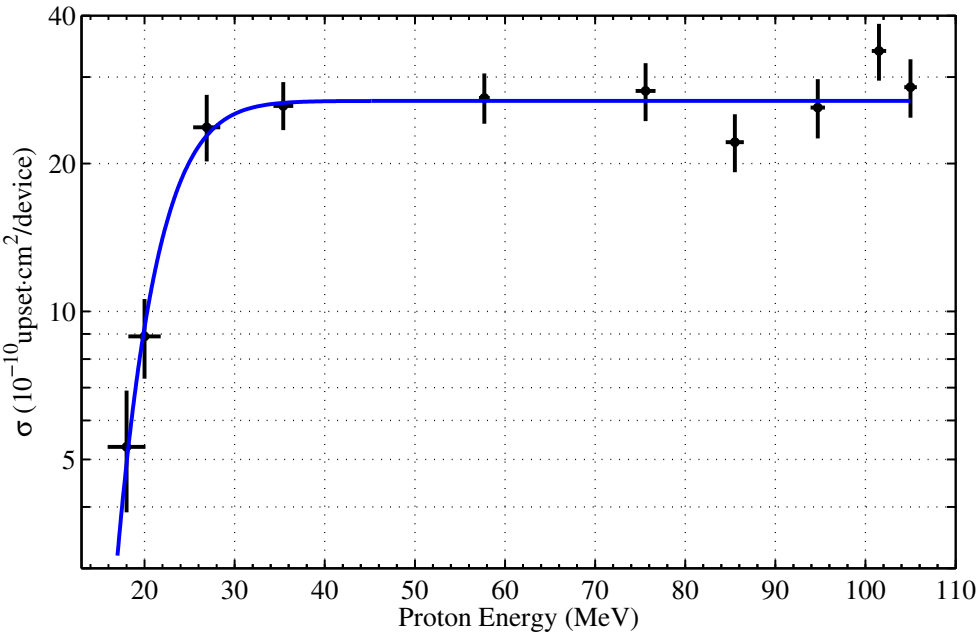


Figure 8.11: Total proton induced single-event upset cross-section for XC4036XLA device.

Data Description	Parameters	Fit Result
switch upsets	$\sigma_{sat}(10^{-10}\text{cm}^2/\text{device})$	26 ± 1
	E_0 (MeV)	13 ± 3
	W (MeV)	11 ± 3
	S (MeV)	2 ± 1
	χ^2/dof	0.81
circuit upsets	$\sigma_{sat}(10^{-10}\text{cm}^2/\text{device})$	1.3 ± 0.2
	E_0 (MeV)	1 ± 8
	W (MeV)	22 ± 8
	S (MeV)	9 ± 8
	χ^2/dof	1.8
total upsets	$\sigma_{sat}(10^{-10}\text{cm}^2/\text{device})$	27 ± 1
	E_0 (MeV)	1 ± 3
	W (MeV)	22 ± 3
	S (MeV)	5 ± 2
	χ^2/dof	0.90

Table 8.4: Parameters for a Weibull CDF fit to the XC4036XLA data.

Data Description	Parameters	Fit Result
switch upsets	$\sigma_{sat}(10^{-10}\text{cm}^2/\text{device})$	26 ± 1
	E_{th} (MeV)	22 ± 1
	W (MeV)	1.26 ± 0.09
	χ^2/dof	0.69
circuit upsets	$\sigma_{sat}(10^{-10}\text{cm}^2/\text{device})$	1.4 ± 0.2
	E_{th} (MeV)	22 ± 2
	W (MeV)	1.1 ± 0.1
	χ^2/dof	1.45
total upsets	$\sigma_{sat}(10^{-10}\text{cm}^2/\text{device})$	27 ± 1
	E_{th} (MeV)	22 ± 1
	W (MeV)	1.23 ± 0.08
	χ^2/dof	0.79
switch upsets (1999)	$\sigma_{sat}(10^{-10}\text{cm}^2/\text{device})$	26 ± 4
	E_{th} (MeV)	36 ± 4
	W (MeV)	1.1 ± 0.1
	χ^2/dof	0.76

Table 8.5: Parameters for a log-normal CDF fit to the XC4036XLA data.

Model	Data	Parameter	Fit Result
Weibull	switch	$\sigma_{sat}(10^{-10}\text{cm}^2/\text{device})$	26 ± 1
		E_{th} (MeV)	22 ± 6
	circuit	$\sigma_{sat}(10^{-10}\text{cm}^2/\text{device})$	1.3 ± 0.2
		E_{th} (MeV)	22 ± 7
	total	$\sigma_{sat}(10^{-10}\text{cm}^2/\text{device})$	27 ± 1
		E_{th} (MeV)	22 ± 6
log-normal	switch	$\sigma_{sat}(10^{-10}\text{cm}^2/\text{device})$	26 ± 1
		E_{th} (MeV)	22 ± 1
	circuit	$\sigma_{sat}(10^{-10}\text{cm}^2/\text{device})$	1.3 ± 0.2
		E_{th} (MeV)	22 ± 2
	total	$\sigma_{sat}(10^{-10}\text{cm}^2/\text{device})$	27 ± 1
		E_{th} (MeV)	22 ± 1

Table 8.6: Comparison of SEU model parameters obtained by the Weibull and log-normal CDFs.

respectively, that large negative correlations exist between both the width and shape parameters and the threshold energy for the Weibull CDF, while no such strong correlation exists between the parameters of the log-normal model. For the data described here it appears that the Weibull model contains a redundant parameter hinting that a model with fewer degrees of freedom might fit the data better.

$$\mathbf{M_w} = \left[\begin{array}{c|cccc} & E_{th} & W & S & \sigma_{sat} \\ \hline E_{th} & 1.000 & -0.958 & -0.953 & 0.312 \\ W & -0.958 & 1.000 & 0.842 & -0.167 \\ S & -0.953 & 0.842 & 1.000 & -0.390 \\ \sigma_{sat} & 0.312 & -0.167 & -0.390 & 1.000 \end{array}\right] \tag{8.10}$$

$$\mathbf{M_{ln}} = \left[\begin{array}{c|ccc} & \sigma_{sat} & E_{th} & W \\ \hline \sigma_{sat} & 1.000 & 0.477 & 0.330 \\ E_{th} & 0.477 & 1.000 & 0.748 \\ W & 0.330 & 0.784 & 1.000 \end{array}\right] \tag{8.11}$$

A choice was made to use the log-normal CDF to model the XC4036XLA data as the threshold energy and saturation cross-section could be obtained directly from the function and the errors in the parameters were well behaved, i.e. no parameter errors included part of the non-physical parameter space.

8.2.4 Comparison with Previously Collected Data

The analysis described above was performed on data obtained on the last of three proton tests of the XC4036XLA device. This test was executed in a manner that would provide good statistics for the cross-section calculation. Two earlier tests were carried out in part to obtain a cross-section measurement for the DUT, but they were primarily used to define a systematic method for the execution of all future tests. The data gathered at these initial tests were discussed in this section.

On June 14 1999, the first of the three tests of the XC4036XLA FPGA was executed at the TRIUMF PIF. Three proton energies were used to irradiate the XC4036XLA devices. Two devices were irradiated over a period of approximately 90 minutes and it was determined during this test that the devices were susceptible to upsets. Insufficient data were gathered to make a more quantitative assessment of the device's response to proton irradiation.

A more extensive test was performed with the XC4036XLA device at the PIF between October 31 and November 1st of 1999. The procedure for calculating the cross-sections and their associated uncertainties was the same as that discussed in the previous section, with the statistical uncertainty dominating the overall uncertainty in the cross-section values. One upset was observed in the internal circuit of the DUT at a proton energy of 83 MeV. All other observed upsets were associated with the configuration switches. The cross-sections determined from this data (Figure 8.12) were not inconsistent with those from the June, 2000 data. A log-normal CDF was fit to the data and there was agreement between the saturation cross-section and width parameter (see Table 8.5) although the uncertainties in the parameters were larger than those for the 2000 data. Agreement in the threshold energy parameter did not exist between the data sets, but this was not unexpected as the 1999 data did not examine proton energies lower than 31 MeV, where the severe drop in the cross-section was observed for the device during the June 2000 test.

8.2.5 Bit Normalization

The SEU cross-sections presented in Section 8.2 were dependent on the particular circuit configured in the FPGA. It is often desirable to remove some of the circuit dependence

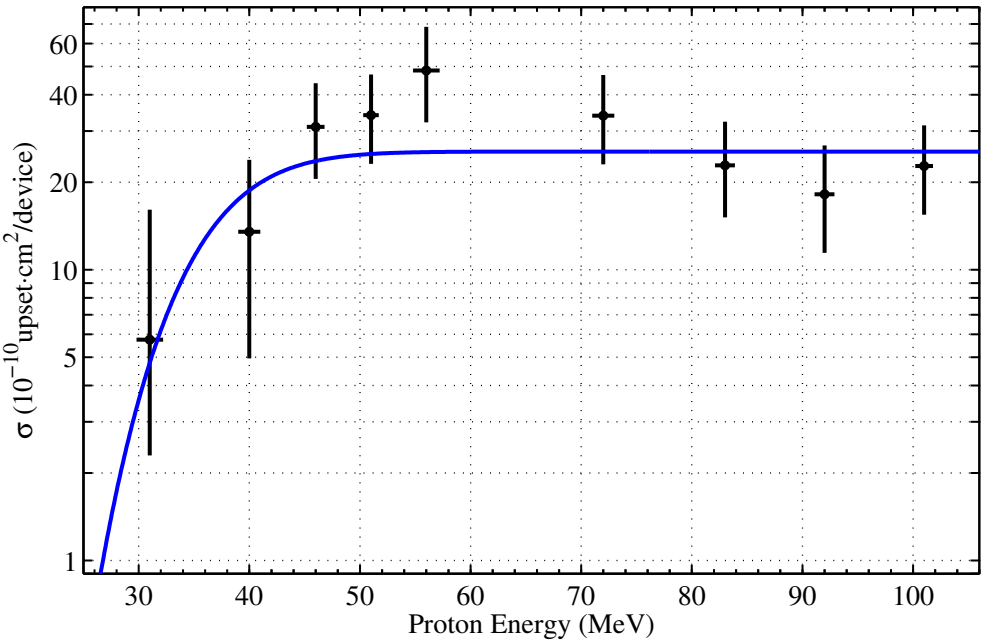


Figure 8.12: Proton induced SEU cross-section for the XC4036XLA taken at the PIF in the fall of 1999.

by scaling the cross-section by the number of primitive elements in the device, which are used by the circuit. This can be useful for designers who may want to consider the use of the device for a similar application or the same device with a different size. The natural primitive element for a RAM, which is the dominant logic in the FPGA, is a memory cell, or bit. Expressing the cross-section as a value per bit allows the prediction of the upset cross-section for other circuits in the same device. The cross-section per bit will actually be less than predicted since not every bit upset will have a consequence on a given circuit.

The XC4036XLA FPGA contains an equivalent of 832,528 bits [111]. The configurable switches contain about 129,600 bits and the configuration switch matrix about 632,600 bits. The remaining bits are in the I/O blocks and special circuit structures, like the read-back circuit, in the FPGA. Using the number of bits in the circuit used for the SCAC prototype circuit and the number in the underling switch matrix, the bit-normalized cross-sections were calculated and are plotted in Figure 8.13. Table 8.7 gives the saturation cross-sections for the bit-normalized data.

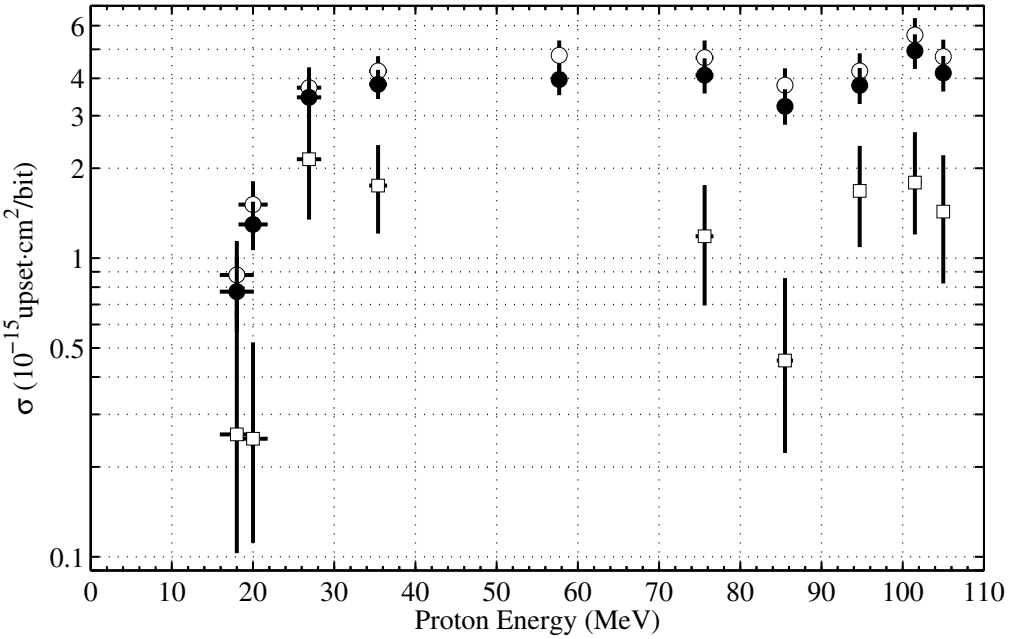


Figure 8.13: The single-event upset cross-section for the total device (solid circles), circuit (hollow squares), and configuration switches (hollow circles) normalized by the number of bits for the XC4036XLA device.

Data Description	Saturation Cross-Section (10^{-15}cm^2/device)
switch upsets	4.5 ± 0.2
circuit upsets	1.2 ± 0.2
total upsets	3.6 ± 0.2
switch upsets (1999)	4.5 ± 0.7

Table 8.7: Bit-normalized SEU saturation cross-section for the XC4036XLA prototype.

8.3 Proton-induced SEU Cross-Section of the DSM ASIC Prototype

Twelve DSM prototype devices were irradiated at the TRIUMF PIF facility on two occasions, June 8th to June 9th and September 4th to September 6th, of 2002 to measure the SEU cross-section and test for any other single-event effects. During the June test 8 devices were irradiated in the high intensity position of the low energy BL2C beam-line at energies between 20.0 MeV and 105.0 MeV. During the September test 4 devices were irradiated in the high energy BL1B beam-line at 491 MeV.

The monitoring for the DSM test was more sophisticated than that used for the SEE tests performed on the XC4036XLA devices. Mitigation techniques were included in the design of the DSM prototype and SEUs occurring in most parts of the device could be corrected or detected [17]. The SRAM portions of the circuit were protected by Hamming codes, while triple redundancy and majority logic were used for the registers. Single-bit upsets occurring in either part of the circuit could be corrected while multiple-bit upsets in the SRAM could be detected. The situation was complicated by the fact that data being transmitted off of the chip were not protected, which was the case for all of the devices. The bunch-crossing identifier and event counter, as well as the data being sent to the gain selector, were also unprotected. The upsets measured during the two irradiation periods at the PIF are listed in Table 8.8. Single-bit upsets that were corrected are referred to as “SRAM” upsets. Upsets occurring in the latency FIFOs were referred to as “LFIFO” upsets. Some of the LFIFO upsets were protected with double redundancy and were detectable, while others were protected by triple redundancy and were correctable. Both types of upsets occur in SRAM. They are protected with different EDAC circuits. Neither of these types of upsets will be of concern for operation in the ATLAS LAr readout system. A multiple-bit upset was referred to as an “MBIT” upset, while upsets occurring in the unprotected bunch-crossing identifier and event counter registers were referred to as “BCID” and “EVT” upsets respectively. Upsets occurring in the shift registers were referred to as “SHFT” upsets.

The cross-sections were determined in the same manner as for the XC4036XLA device with the exception that rather than differentiating between switch and circuit cross-section, the total and non-correctable upset cross-sections were determined separately.

DUT #	Energy (MeV)	Fluence ($10^{12}\mathrm{cm}^{-2}$)	Correctable		Non-correctable			
			SRAM	LFIFO	BCID	EVT	SHFT	MBIT
49	20.0 ± 1.8	3.25 ± 0.32	0	1	1	0	0	0
50	35.4 ± 1.1	3.21 ± 0.23	7	0	0	0	0	0
51	35.4 ± 1.1	3.21 ± 0.23	5	6	0	0	0	0
38	62.9 ± 0.5	3.12 ± 0.24	21	10	0	0	0	0
17	66.8 ± 1.2	2.84 ± 0.22	23	11	0	0	0	0
34	85.5 ± 1.0	3.00 ± 0.23	22	16	0	0	0	0
13	105.0 ± 0.7	3.02 ± 0.23	29	15	0	0	3	1
14	105.0 ± 0.7	2.97 ± 0.23	28	10	0	0	1	1
5	491.0 ± 1.0	15.24 ± 0.51	256	116	3	2	21	6
9	491.0 ± 1.0	7.97 ± 0.41	165	82	3	1	12	3
12	491.0 ± 1.0	7.97 ± 0.41	141	68	1	1	6	1
27	491.0 ± 1.0	10.60 ± 0.54	206	90	0	1	19	2

Table 8.8: Upsets measured during proton irradiations of DSM SCAC prototype.

The correctable and uncorrectable SEU cross-sections are shown in Table 8.9. No down-loading of bit-streams to the monitor FPGA was required and thus the only deadtime following upsets was the time required to load the registers and FIFOs, which was shorter than the time required to reset the XC4036XLA device. Thus no correction was performed. The contributions to the uncertainties were the statistical uncertainties inherent in the number of observed upsets and the dosimetry and uniformity systematics associated with the determination of the proton fluence. Figure 8.14 shows the SEU cross-section data plotted against proton energy and shows that the cross-section 491 MeV is more than twice the cross-section at 105 MeV. The 491 MeV data was taken using beam-line 1B at the PIF rather than beam-line 2C where all other data collected at the PIF was taken. It is likely that a calibration difference existed between the two data sets. The log-normal CDF was fit to the data and the fit parameters are given in Table 8.10 and plotted in Figure 8.15. The 491 MeV data was omitted from the fits.

Due to the lack of non-correctable upset data collected during the PIF tests, fitting of the data was difficult. To remedy the problem three data points recorded during a test of the an earlier protoype at the Harvard Cyclotron were used in addition to the

DUT #	Energy (MeV)	Cross-section (10^{-12}cm^2/device)	
		Total	Uncorrectable
49	20.0±1.8	$0.62^{+0.69}_{-0.39}$±0.06	$0.31^{+0.54}_{-0.19}$ ± 0.03
50	35.4±1.1	$2.18^{+1.03}_{-0.86}$±0.16	
51	35.4±1.1	$3.43^{+1.19}_{-0.99}$±0.25	
38	62.9±0.5	$9.93^{+2.02}_{-1.83}$±0.76	
17	66.8±1.2	$12.0^{+2.2}_{-2.0}$±0.9	
34	85.5±1.0	$12.7^{+2.3}_{-2.1}$±1.0	
13	105.0±0.7	$15.9^{+0.2}_{-0.2}$±1.2	$1.32^{+0.92}_{-0.55}$±0.09
14	105.0±0.7	$13.5^{+2.3}_{-2.1}$±1.0	$0.67^{+0.76}_{-0.42}$±0.05
5	491.0±1.0	$26.5^{+2.0}_{-2.0}$±2.0	$2.11^{+0.64}_{-0.57}$±0.16
9	491.0±1.0	$33.4^{+2.1}_{-2.1}$±1.7	$2.38^{+0.61}_{-0.52}$±0.12
12	491.0±1.0	$27.3^{+1.9}_{-1.9}$±1.4	$1.13^{+0.48}_{-0.34}$±0.06
27	491.0±1.0	$29.9^{+1.7}_{-1.7}$±1.5	$2.07^{+0.50}_{-0.44}$±0.11

Table 8.9: The proton induced total and uncorrectable SEU cross-section values measured for the DSM SCAC prototype. Measurements where no upsets were observed were omitted from the table.

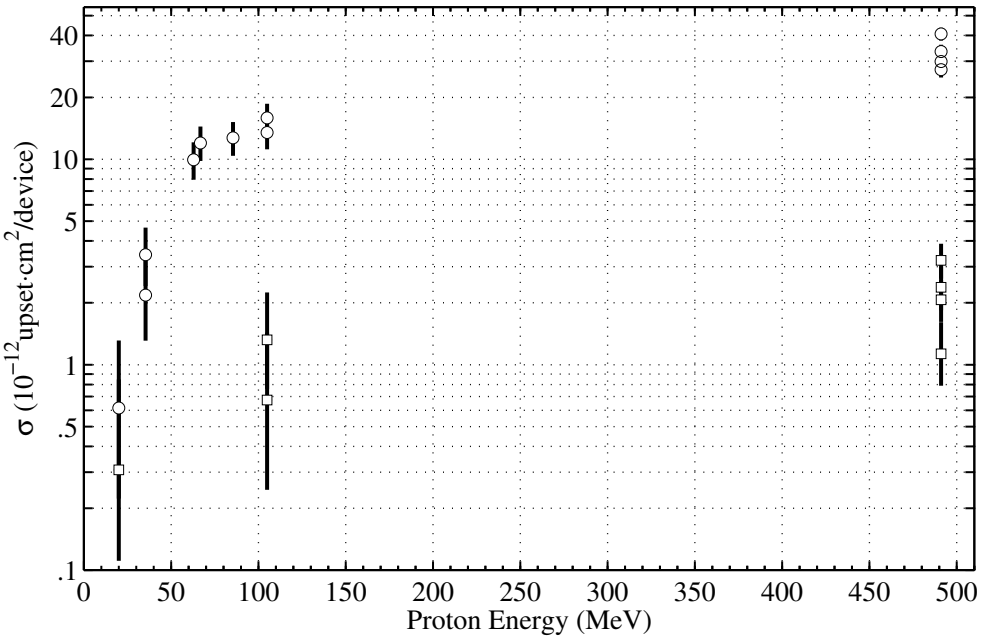


Figure 8.14: The total (circles) and uncorrectable (squares) proton induced SEU cross-section for the DSM device.

Data Description	Parameters	Value
total upsets	$\sigma_{\mathrm{sat}}(10^{-12}\mathrm{cm}^2/\mathrm{device})$	16±4
	$\mathrm{E_{th}}$ (MeV)	54±12
	W (MeV)	1.7±0.3
	χ^2/dof	0.49
uncorrectable upsets	$\sigma_{\mathrm{sat}}(10^{-12}\mathrm{cm}^2/\mathrm{device})$	0.5±0.1
	$\mathrm{E_{th}}$ (MeV)	44±24
	W (MeV)	2±1
	χ^2/dof	0.69
SRAM upsets	$\sigma_{\mathrm{sat}}(10^{-12}\mathrm{cm}^2/\mathrm{device})$	9±2
	$\mathrm{E_{th}}$ (MeV)	50±10
	W (MeV)	1.5±0.3
	χ^2/dof	0.26
LFIFO upsets	$\sigma_{\mathrm{sat}}(10^{-12}\mathrm{cm}^2/\mathrm{device})$	4.4±0.9
	$\mathrm{E_{th}}$ (MeV)	40±10
	W (MeV)	1.6±0.3
	χ^2/dof	0.42

Table 8.10: SEU cross-section parameters for the DSM prototype. The fit function is a log-normal CDF. The data used for the uncorrectable upset fit contained additional data from Ref. [100], while the total upsets data did not contain any data in addition to that described in this thesis.

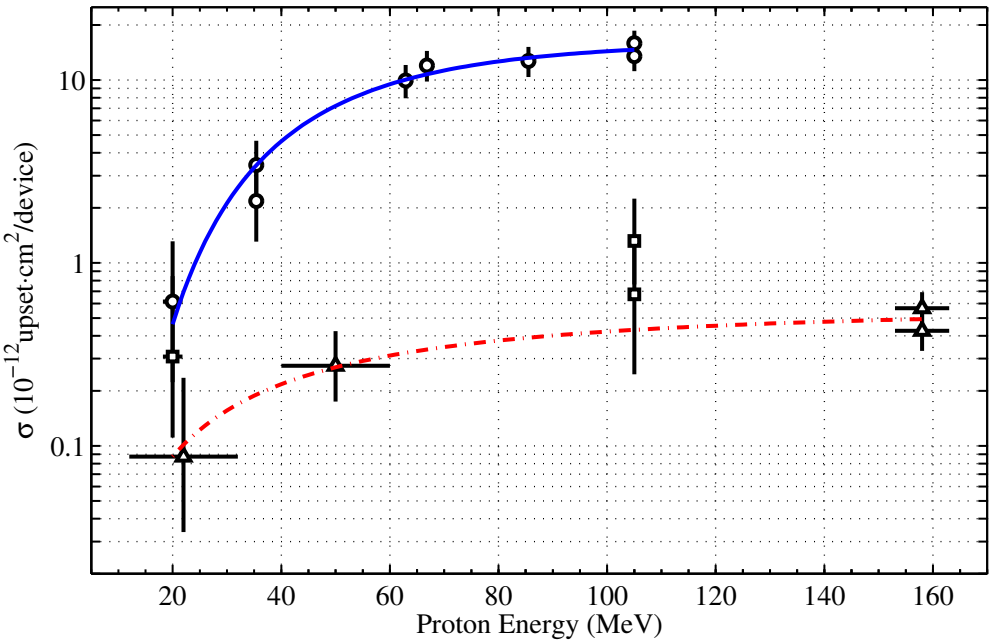


Figure 8.15: The total (circles) and uncorrectable (squares and triangles) proton-induced SEU cross-section for the DSM SCAC prototype that can be corrected. The triangles correspond to data taken from tests on an earlier prototype of the SCAC (Ref [100]). The data have been fit with a log-normal CDF. The Nevis data were not used in the fit for the total data and have not been included in the plot.

PIF data [100][¶]. Attempts were made to include the 491 MeV data in the fits to the uncorrectable data but the best fits were obtained when the 491 MeV was omitted and the Nevis data was used. The energy threshold of a fit to the total data and the uncorrectable upset data were consistent with one another while the saturation cross-section of the uncorrectable SEUs was an order of magnitude smaller.

The single-bit upsets detected in the SRAM are correctable but it was instructive to examine these upsets as they may provide valuable information pertaining to the behaviour of the device as a whole. If inadvertent changes were to occur during the future fabrication runs it is conceivable that device operation or behaviour could be affected. For example, slight changes in the process could alter the sensitivity of the SRAM cells to SEUs and this would become apparent as the measured threshold energy or other parameters could change. As a check of uniform SRAM sensitivity, Figure 8.16 shows the proton induced

[¶]The earlier prototype was tested by researchers from the Nevis Laboratories.

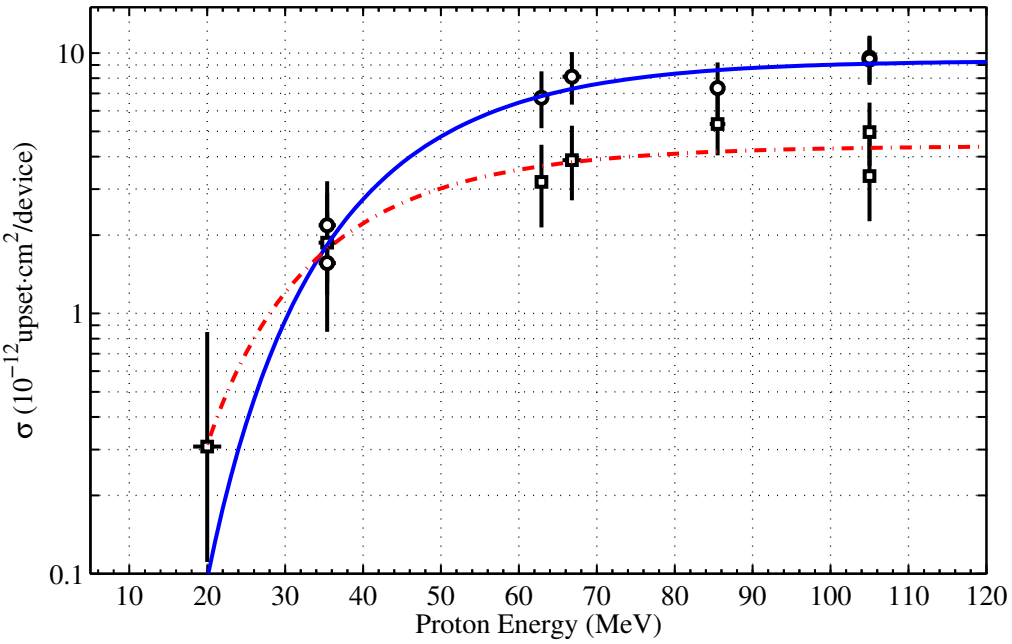


Figure 8.16: SRAM (circles) and LFIFO (squares) proton-induced SEU cross-sections for the DSM prototype SCAC. The curves are fits to the data using a log-normal CDF.

SEU cross-sections for the SRAM and LFIFO bits. The curves shown on the plot are fits to the data using the log-normal CDF and the fit parameters are summarized in Table 8.10. The threshold energies for the two cross-sections are consistent, but more data would be required to accurately determine the threshold energies for the SRAM and LFIFO cross-sections. A second fit was made to the SRAM and LFIFO upset data where the threshold energies for both were fixed to the value of that from the fit to the LFIFO fit. The ratio of saturation cross-sections agreed with that obtained from the fits made without fixing the threshold energy. In addition to estimating the SEU rate, the SEU cross-sections, both total and uncorrectable, will be used to perform quality control of the SCAC devices.

8.3.1 Angular Dependence of Cross-Section

The proton testing of the SCAC prototypes was performed with the beam incident on the front surface of the DUT (normal incidence), except the DMILL device which was irradiated from the back. The proton flux surrounding the electronics in ATLAS will clearly

vary to some degree with angle, and thus it is important to determine if there is an angular dependence to the SEU cross-section and rate. The DSM prototype was exposed to 491 MeV protons at the PIF with the beam penetrating a variety of angles between 0^o and 180^o in an attempt to determine the angular dependence, if any, of the SEU cross-section. The proton energy was chosen to be large enough that it would not significantly diminish during passage through the packaging and PC board. This was done using the SRIM simulation package.

A rotating apparatus for mounting the test board was built for use at the PIF (Figure 8.17). The board was mounted on the apparatus such that the proton beam was incident on the face of the DUT when the angle was set to 0^o. The board could then be rotated in 5^o increments through 360^o. The angular dependence of the total SEU cross-section for the DSM prototype is shown in Figure 8.18 and the data is listed in Table 8.11. The solid line is a constant value fit to the data while the dotted line is a cubic fit, which was chosen as it exactly parameterized the data. The statistics are relatively low and the data are consistent with some angular dependence of the SEU cross-section. When the cross-sections representing the uncorrectable upsets were plotted (Figure 8.19), no angular dependence was observed. The statistics for the data were too low to allow a statement about the angular dependence of the upsets. There were at most 23 upsets measured for any angle. As the uncorrectable upsets are of most interest with respect to the operation of the device in ATLAS, more data must be taken to determine if any angular dependence exists and will affect the determination of the upset rate in ATLAS.

Other researchers have found angular dependence on the proton induced SEU cross-sections with a deep-sub-micron CMOS SRAM device [112] and the behaviour observed for some devices was similar to that that graphed in Figure 8.18[‖]. One feature remains in Figure 8.18 that is not explained by the results cited above, the cross-section at 180^o is the largest of all measured. An increase in cross-section with proton incident angle might be expected as the track lengths within sensitive volumes could become larger and thus the likelihood of sufficient charge to cause an upset increases. This same reasoning would lead to the situation where the cross-section would increase until the incident angle reached 90^o and then it would decrease again for larger angles [113, 112]. It is possible that

[‖]The range of angles examined in Ref. [112] was only between 0^o and 80^o.

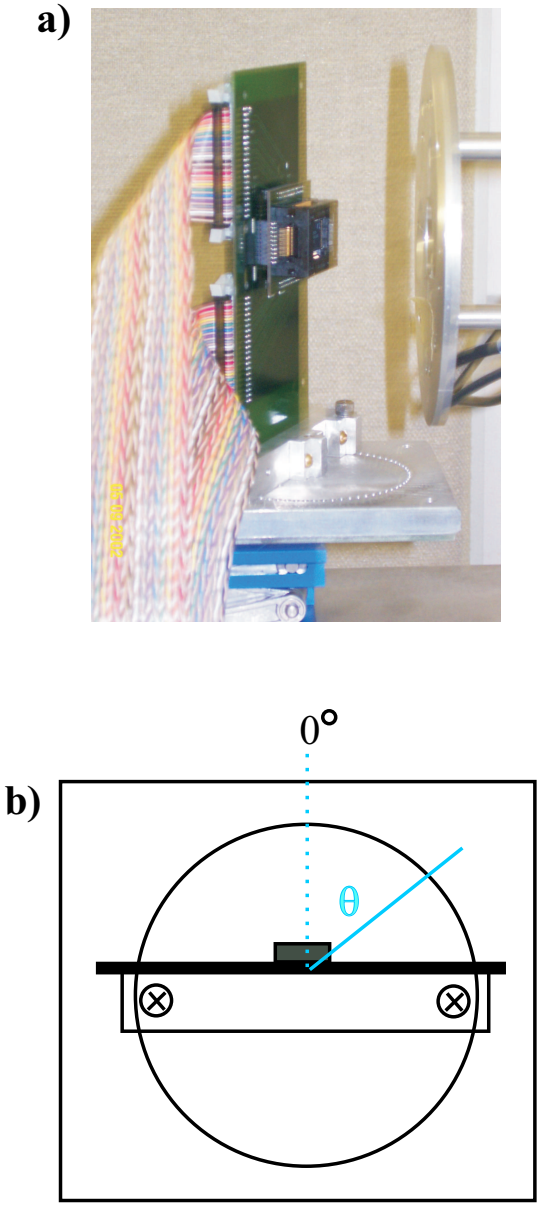


Figure 8.17: Apparatus used for testing the angular dependence of the proton induced SEU cross-section for the DSM prototype. The setup is shown as it was used at the PIF (a), and a top-down view (b) illustrates the definition of angle used in the text. The protons were incident along the normal to the chip face at 0^o

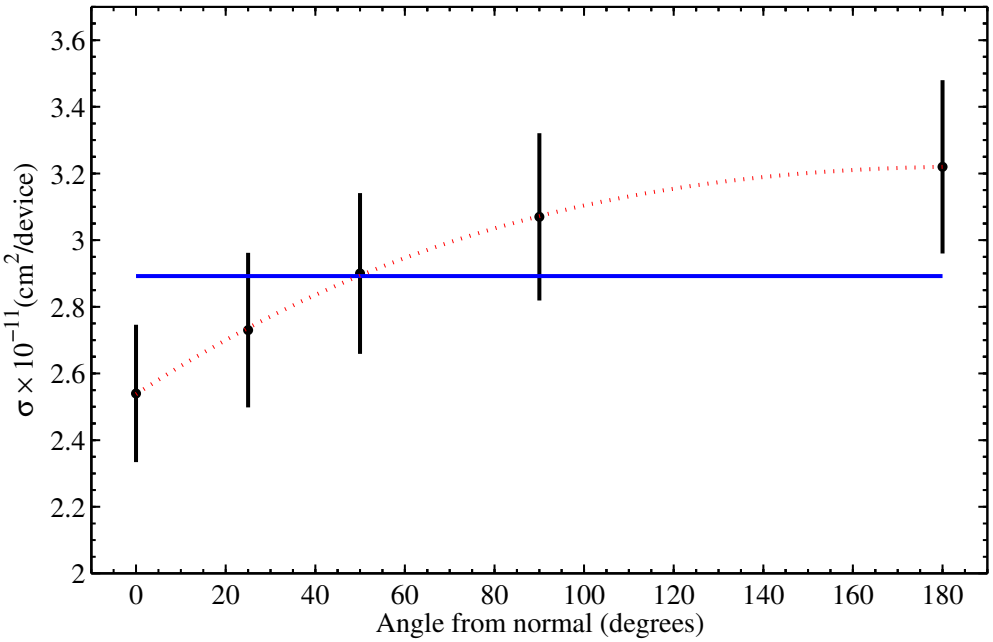


Figure 8.18: Angular dependence of the total SEU cross-section for DSM prototype exposed to 491 MeV protons. The solid line is a constant fit to the data while the dashed line is cubic fit, which exactly parameterized the data.

Angle (Degrees)	DUT #	Run #	Fluence ($10^{12}\mathrm{p/cm^2}$)	Upsets	
				Total	Uncorrectable
0	5	1	2.66 ± 0.14	$83^{+9.8}_{-9.2}$	$7^{+3.3}_{-2.8}$
	5	2	1.86 ± 0.09	$34^{+6.3}_{-5.7}$	$3^{+2.3}_{-1.7}$
	5	3	2.66 ± 0.14	$56^{+8.3}_{-7.2}$	$4^{+2.8}_{-1.7}$
	5	7	2.66 ± 0.14	$79^{+9.3}_{-8.7}$	$9^{+3.8}_{-2.7}$
25	12	11	2.66 ± 0.14	$81^{+9.8}_{-8.7}$	$7^{+3.3}_{-2.8}$
	12	12	2.66 ± 0.14	$65^{+8.8}_{-8.2}$	$1^{+1.8}_{-0.6}$
	12	13	2.66 ± 0.14	$72^{+9.3}_{-8.2}$	$1^{+1.8}_{-0.6}$
50	5	4	0.090 ± 0.009	$0^{+1.3}_{-0}$	$0^{+1.3}_{-0}$
	5	5	2.66 ± 0.14	$84^{+9.8}_{-9.2}$	$6^{+3.3}_{-2.2}$
	5	6	2.66 ± 0.14	$68^{+8.8}_{-8.2}$	$3^{+2.3}_{-1.9}$
	9	8	2.66 ± 0.14	$82^{+9.8}_{-9.2}$	$1^{+1.8}_{-0.6}$
90	9	9	2.66 ± 0.14	$90^{+10.3}_{-9.2}$	$10^{+3.8}_{-3.2}$
	27	14	2.66 ± 0.14	$78^{+9.3}_{-8.7}$	$9^{+3.8}_{-2.7}$
	27	15	2.66 ± 0.14	$77^{+9.3}_{-8.7}$	$3^{+2.3}_{-1.9}$
180	9	10	2.66 ± 0.14	$94^{+10.3}_{-9.7}$	$8^{+3.3}_{-2.7}$
	27	16	2.66 ± 0.14	$71^{+8.8}_{-8.2}$	$3^{+2.3}_{-1.9}$
	27	17	2.66 ± 0.14	$92^{+10.3}_{-9.7}$	$7^{+3.3}_{-2.8}$

Table 8.11: Data used for angular dependence studies.

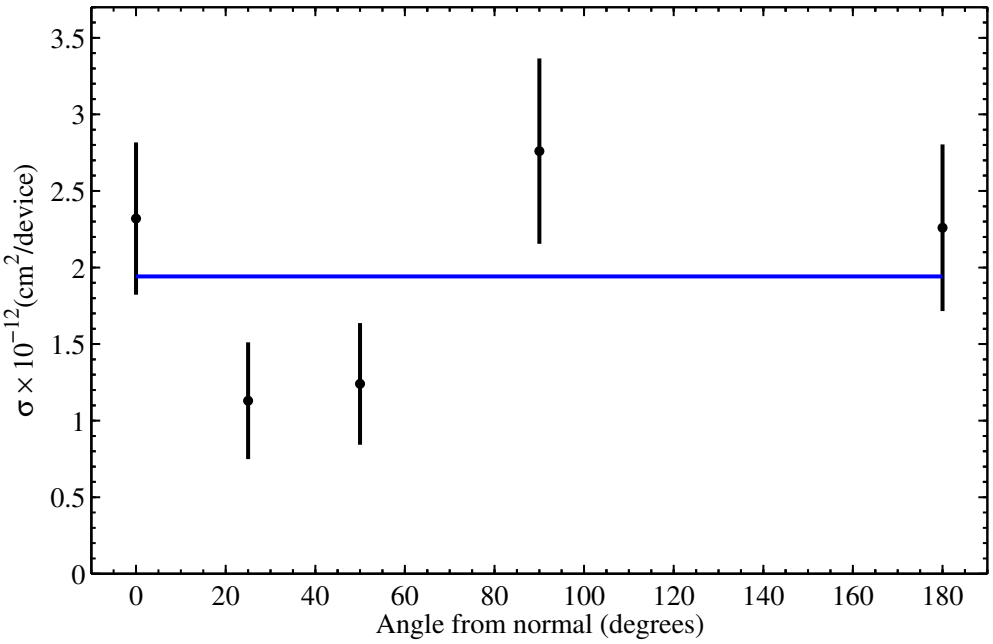


Figure 8.19: Angular dependence of the uncorrectable SEU cross-section for DSM prototype exposed to 491 MeV protons.

the continued increase in cross-section for the DSM SCAC prototype might be attributed to scattering of high Z nuclei into the die from materials within the chip. This would explain the increase in cross-section at 180^o . More testing would be required to ascertain the angular behaviour on the proton-induced cross-section over the full range of 0^o and 180^o .

8.4 Proton-Induced SEU Rate Estimates

Once the SEU cross-sections had been calculated, the spectra described in Section 2.6 (Figure 2.11) were used to estimate the rate of SEUs that would occur in the ATLAS detector for the SCAC prototypes. The upset rate R was given by

$$R = \int_0^\infty \sigma \frac{d\phi}{dE} dE \quad , \tag{8.12}$$

where σ was the SEU cross-section, ϕ was the proton flux, and E was the proton energy. Figure 8.20 is a plot of the integrand (using the XC4036XLA cross-section) and shows that

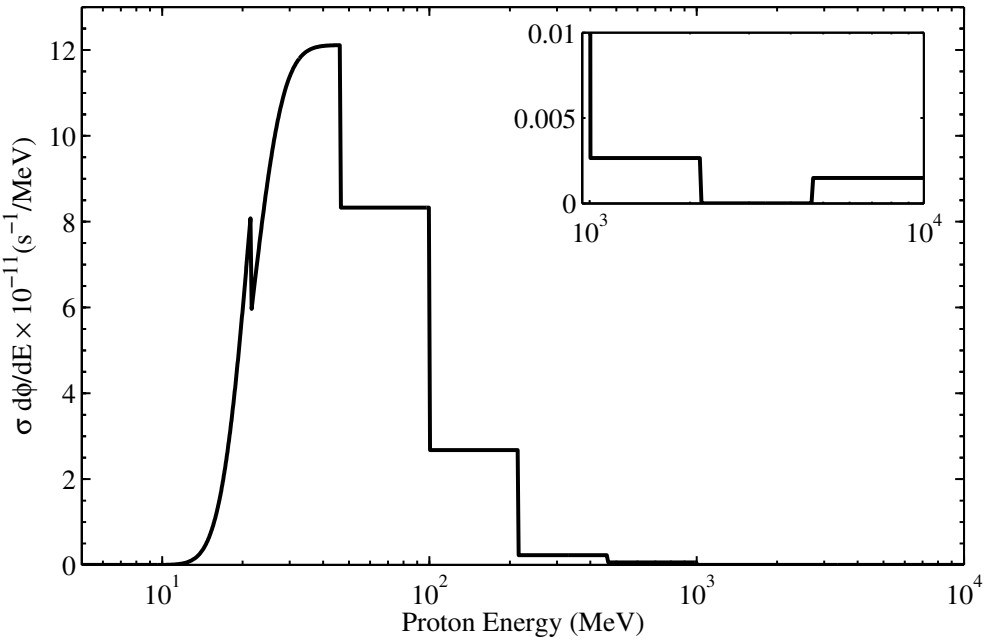


Figure 8.20: Product of the simulated proton energy spectrum $d\phi/dE$ and the SEU cross-section σ. The inset is a close-up view of the region between 1 GeV and 10 GeV. The discontinuous nature of the plot is because of the way that $d\phi/dE$ was binned.

protons with energies between 30 MeV and 200 MeV will give the largest contributions to the SEU rate in ATLAS.

8.4.1 SEU Rate for the XC4036XLA Prototype in ATLAS

While it was important to estimate the SEU rates in ATLAS for all of the candidate SCAC devices, this was especially true for the FPGAs. If upsets were to occur in the configuration switches, FPGAs would require downloads in order to regain functionality. The integral in equation 8.12 was evaluated to estimate the SEU rates in ATLAS. Rate estimates are listed in Table 8.12, along with the mean time between upsets (MTBUs) for the XC4036XLA prototype operating in the ATLAS environment. An additional step has been taken to scale the spectra to the 10 cm by 10 cm region where the SCAC will be situated. This was motivated by a more precise estimate of the spectra in the region. The latest version of the integrated spectra in the electronics region was used to normalize those used in the calculation [114].

There will be large contributions to the SEU rate in ATLAS due to pions and neutrons in addition to that from the protons. While the ideal situation would have been to irradiate the devices with both neutrons and pions, it was not done as facilities were not easily accessible. The TRIUMF facility is capable of providing both pions and neutrons that could be used for testing, however, the pion beam was out of commission until late in 2003, and sufficient neutron fluences to simulate the ATLAS environment could not be produced. Estimates for the pion-induced and neutron-induced SEU rates were made instead. As the neutron and proton non-elastic cross-sections have similar behaviour (Figure 8.21) [115, 116], with only about 10% of the upset rate due to neutrons below 20 MeV, the proton-induced SEU cross-section was used to estimate the neutron-induced SEU rate.

Some experimental SEU data for DRAMs irradiated with pions indicate that at about 200 MeV there is a significant increase of the SEU cross-section compared to protons of the same energy [117, 118]. However, there is some device-dependent spread in the experimental data and some devices seem to be rather consistent with an increase that is only slightly more than the difference in inelastic cross-sections. Recent results with SRAMs indicate that pions are no more likely than protons to create SEUs [119]. It is thus assumed that the same upset cross-section can be used for pions and protons in the energy region in which we have a sizable pion flux. The total device upset rates and mean time between upsets for protons, neutrons, pions and the total for these hadrons are listed in Table 8.12.

8.4.2 SEU Rate for the DSM Prototype in ATLAS

The total and uncorrectable SEU rates for the DSM SCAC prototype in ATLAS were estimated in the same manner as was done for the XC4036XLA prototype. The single-bit SEUs occurring in the RAM could be corrected in real time during operation. The uncorrectable SEUs, however, could not be corrected and would affect the data. If a difference in the addresses and controller bits coming from the two SCACs on a FEB is detected by the ROD in ATLAS, as discussed in Section 2.5, the board will be reset and the events stored in the SCA pipelines may be lost. Data sitting in the read FIFO will be lost, while data in the latency FIFO will only be lost if a trigger is issued. It was important to estimate the uncorrectable SEU rate in ATLAS to determine the amount of data affected by such

Hadron	Upset Type	Rate 10^{-8}(upset·s^{-1}/device)	MTBU
Proton	Switch	1.14	8.8 ATLAS·yr
	Circuit	0.06	171.6 ATLAS·yr
	Total	1.15	8.7 ATLAS·yr
Pion	Switch	1.13	8.8 ATLAS·yr
	Circuit	0.06	172.4 ATLAS·yr
	Total	1.15	8.7 ATLAS·yr
Neutron	Switch	73.4	15.8 days
	Circuit	3.77	2.7 ATLAS·yr
	Total	74.5	15.5 days
Total Hadron	Switch	75.7	15.3 days
	Circuit	3.89	2.6 ATLAS·yr
	Total	76.8	15.1 days

Table 8.12: Predicted SEU rates for XC4036XLA device if used in ATLAS LAr readout system. A year in this context refers to a year of LHC running which is taken to be 10^7 seconds, while a day is a calendar day (24 hours).

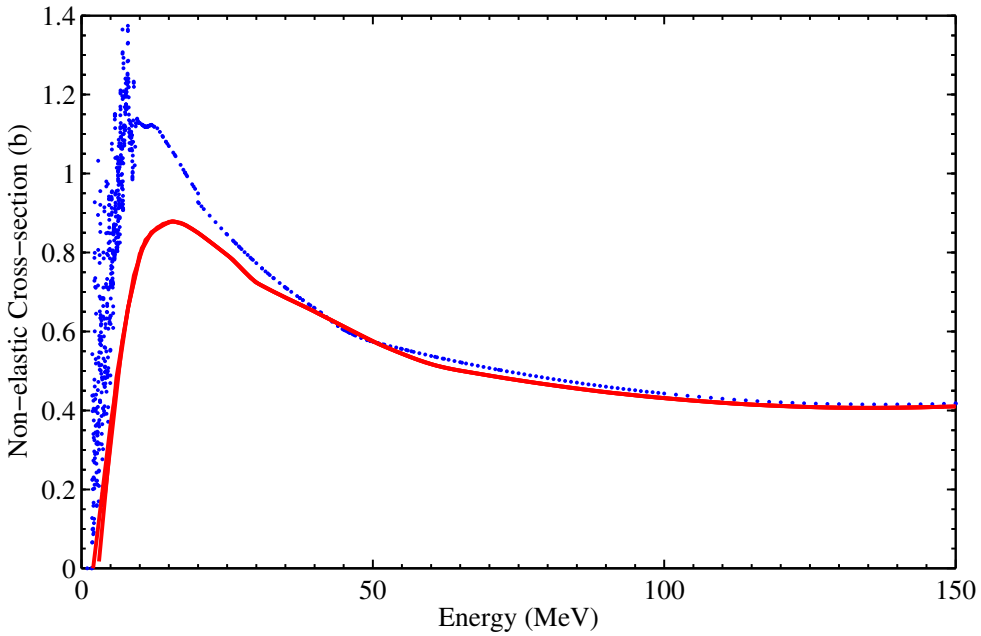


Figure 8.21: Inelastic cross-sections for neutrons (dots) and protons (solid line) on ^{28}Si. Data is from Ref [115]

Hadron	Upset Type	Rate 10^{-11}(upset·s^{-1}/device)	MTBU (1,792 devices)
Proton	Total	4.66	1.2 ATLAS·yr
	Uncorrectable	0.16	34.8 ATLAS·yr
Pion	Total	5.83	1.0 ATLAS·yr
	Uncorrectable	0.19	29.1 ATLAS·yr
Neutron	Total	282	55 hr
	Uncorrectable	9.83	65.8 days
Total Hadron	Total	292	53 hr
	Uncorrectable	10.18	63.4 days

Table 8.13: Predicted SEU rates for DSM SCAC prototype if used in ATLAS LAr readout chain. A year in this context refers to a year of LHC running which is taken to be 10^7 seconds, while hours and days are calendar hours and days.

upsets. The SEU rate estimates for protons, pions, and neutrons are listed in Table 8.13. There will be 1,792 SCACs used to instrument the electro-magnetic barrel calorimeter** and there will be one uncorrectable upset approximately every 2 months of contiguous operation. The MTBU of total SEUs in the ATLAS electro-magnetic barrel would be about 55 hours.

8.5 SEU Rate Estimate for the DMILL Prototype SCAC in ATLAS

The SEU rate estimate made for the DMILL prototype SCAC in ATLAS was made in a different manner than that described for the XC4036XLA and DSM prototypes. Due to problems encountered during the proton irradiation of the DMILL device, data were only taken using 68 MeV protons. The ATLAS radiation requirements stipulate that all proton irradiation tests, which are carried out to measure non-damaging SEE phenomena must use protons of energy greater than 60 MeV. The rate measured at that energy could then be used to estimate the upset rate due to the proton fluence integrated over energy.

The SEUs measured were not considered soft errors in that they could not be cleared. Once an SEU had occurred the monitor program could not reload the parameters into memories on the DUT until the power to the DUT had been cycled. After a power cycle

**Only the SCACs in the electro-magnetic barrel are considered here as they are closer to the radiation source than those used for the endcap calorimeters and the barrel is expected to have higher upset rates.

DUT #	Proton Fluence (10^{10}p/cm^2)
4	4.8 ± 0.3
5	4 ± 2
7	5.3 ± 0.3
9	4.5 ± 0.1
Average	4.6 ± 0.3

Table 8.14: The average proton fluence incident on each device prior to the device upsetting. Five runs are averaged for devices 4, 7, and 9, while six runs were averaged for device 5.

the DUT would again function normally. No other types of SEUs were observed.

The upset rate at ATLAS was determined by comparing the simulated hadron flux of 2.835×10^{10} h/cm^2/yr (at the position of the SCAC within ATLAS) to the fluence measured at the PIF during the test. Five runs were made for three of the four devices tested, and six runs were used for the fourth. The average proton fluence measured during the test was determined for each device and the results are listed in Table 8.14 along with the weighted average for all four of the tested devices. Comparing the average fluence between SEUs and the $\mathrm{SRL}_{\mathrm{SEE}}$ for the location of the DUT in ATLAS resulted in a value of 0.61 SEU/yr for a DMILL device. From this value the MTBU, to occur in the devices instrumenting the electro-magnetic barrel was determined to be 2.55 hr.

It was important to understand why all of the upsets observed required a power cycle so the nature of the observed upsets was further examined. A second indication that the upsets were not soft was that they occurred tightly grouped in time. The probability distribution for a SEU with time is an exponential distribution [104]. Section 8.2 illustrates this behaviour with a commercial FPGA. The data taken during the DMILL test did not appear to follow an exponential distribution. In order to determine the possibility that the data were not exponential, a data set that did follow an exponential distribution (that from Figure 8.7) was used for comparison. While the two data sets were taken with different devices a comparison can still be made. The resolution[††] of an exponential distribution is 100% by definition as the first and second moments are equal. Figure 8.22 shows

[††]The resolution here is defined as the ratio of second and first moments of the distribution, which should be 1, or 100% for an exponential distribution.

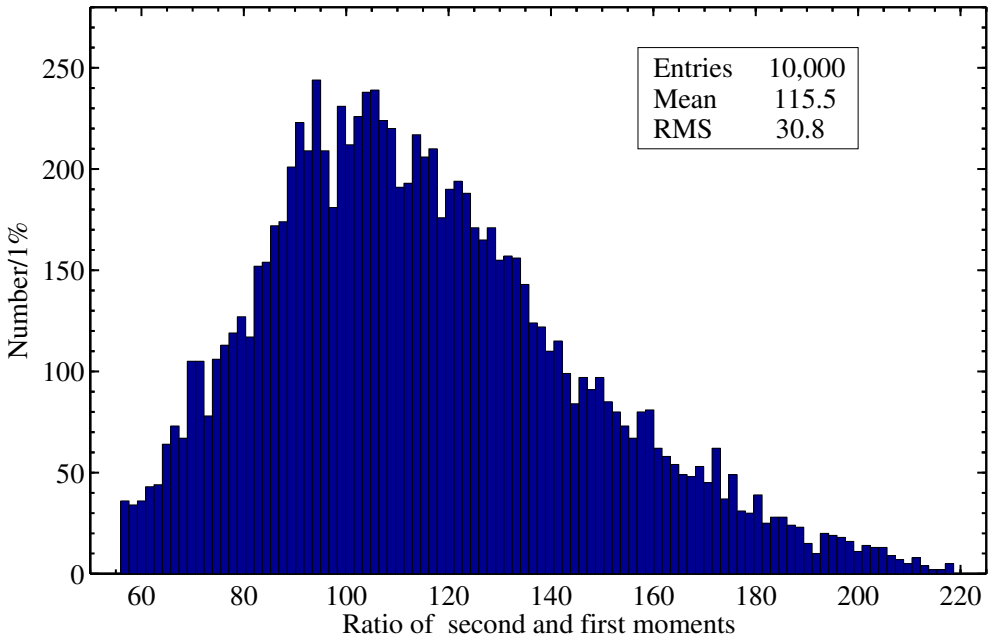


Figure 8.22: Distribution of resolutions for data taken with an XC4036XLA device from an earlier test.

a distribution of resolutions calculated by randomly selecting five data points from the exponential data taken with an earlier device and calculating their first and second moments. The most probable value (first moment) is consistent with 100%, which is what would be expected for data described by an exponential distribution. The groups of five data points were chosen to simulate the data taken during the test described in this section. To obtain good statistics in building the distribution in Figure 8.22, ten thousand samples of five points were used. This was an acceptable number as it was significantly less than the number of possible groupings of 5 numbers from a group of 101 (the number of data points in the baseline data), which is roughly equal to 10^{10} for groups of 5 taken from a population of 101 in size. Clearly, within a set of 10,000 samples chosen from the data there is small probability of duplicating the choice.

Once the baseline distribution of resolutions for an exponential data set had been built, one for each DUT, the resolutions for the data set of interest could be compared against it. The measured resolutions for the data taken are listed in Table 8.15. The differences in resolution between the mean of the distribution in Figure 8.22 and the DMILL data were

Device	Resolution (%)
4	7.3
5	37.0
7	5.6
9	3.9

Table 8.15: The resolutions (σ/μ) measured for each DMILL device tested.

then compared, as shown in Table 8.15. It is thus possible that the SEU data taken with the DMILL device is described by an distribution different from an exponential. The small resolutions of three of the devices, and the fact that all four devices upset after approximately the same irradiation time (or proton fluence) tends to indicate that a radiation induced systematic effect was observed. As will be seen in the following section, this effect was likely the build-up of charge on a capacitive element in an analog portion of the circuit.

8.5.1 Qualitative Studies of the DMILL Device and System

The work described in this section was motivated by Douglas Gingrich and carried out by Douglas Gingrich with assistance from Li Chen and Lars Holm. It is included for completeness. To probe the possibility of a systematic effect causing the results described in the previous section, the operation of two parts of the DMILL device were examined.

It was assumed that as there were no soft errors, the RAMs used in the device design were probably not failing under irradiation. Any sensitivity in the RAMs would have been detectable as the sequence of addresses stored in the RAMs would have become corrupted, or out of sequence.

The two remaining circuits which may have been causing the observed behaviour were the POR circuit and the input buffers, neither of which were part of the DMILL circuit library. To test the POR circuit, it was disconnected from the device circuit. This circuit was designed such that it could be disabled by removing a jumper. When the POR circuit was removed, the circuit upset behaviour was no longer observed. The behaviour appeared systematic and the effect appeared to be "cumulative". The purpose of the POR circuit was to allow reset signals to be detected by the controller. If the POR circuit was

continually executing this procedure the behaviour would be the same as that observed. Combining the cumulative behaviour with the observed performance of the controller circuit, it appeared as though a certain amount of irradiation would set the POR circuit into a state where it continuously reset the circuit rendering the controller circuit useless.

After the removal of the POR circuit, soft upsets were observed when the radiation was turned on or off. While this effect was clearly related to the radiation, it appeared not to be radiation damage related. The effect occurred regardless of the length of time the beam was on. Configuration of the test device after turning on the proton beam incident on the device did not result in any observed upsets. It was postulated that the effect was due to noise on two input pins which were left floating after the POR circuit was disconnected. Additional evidence that supports this hypothesis is that on the test-bench errors similar in appearance to soft SEUs were observed when the POR circuit was disconnected.

During the test it was observed that there was a link between occasional non-recoverable errors, occurring after the POR circuit was removed, and an increase in the current drawn by the input buffers on the test device. The lines connected to these buffers were examined to ensure that there were no spurious signals being generated by the monitor board. None were detected. Current must have been draining somewhere on the DMILL device. The effect was observed during test-bench operation and therefore a radiation effect was ruled out. A solution was obtained by disconnecting the POR circuit and ensuring that all of the pins on the device were connected to either ground or power through resistors. After this the problem was never observed again.

8.6 Destructive Single-Event Effects

The SEEs described thus far are non-destructive in that they can be cleared without permanently affecting the device. Damaging SEEs are a serious concern for devices to be used in ATLAS as device replacement will not easily be achieved. An SEL or other damaging SEE would appear as either a rapid increase in power supply current drawn by the device, in the case of SEL, or by permanent device malfunction for other SEEs, such as SEGR. The DMILL prototype was irradiated only with 68 MeV protons, the XC4036XLA prototype was irradiated with protons having energies up to 105 MeV, and the DSM prototype was irradiated with protons having energies up to 491 MeV.

To search for latch-up the XC4036XLA was exposed to the maximum proton energy of 105 MeV to a total fluence of $(5.9 \pm 0.3)\times10^{11}$ p/cm^2. One SEL was observed during this test and none were observed during the rest of the tests performed on the device. The SEL rate at ATLAS was estimated using Poisson statistics to build 95% confidence levels for the expected number of SEL cross-sections for each proton test energy. The results and values used in the calculations are given in Table 8.16. The spectra in Section 2.6 were used to calculate the rates as was done for the SEU rates. Linear interpolations were made between each of the cross-section values. The uncertainties in the proton fluence have not been included in the calculation. The proton-induced SEL rates, per device at ATLAS, were estimated to be between 1.3×10^{-13} SEL/s and 2.6×10^{-10} SEL/s to a 95% confidence level. These corresponded to a times between SELs of 7.87×10^5 device·yr and 388 device·yr. There will be an upper limit of 44, to a 95% CL, SCAC SELs in the FEBs instrumenting the electro-magnet barrel during the 10 years of ATLAS operation.

An alternate approach was used to estimate the SEL rate for protons in ATLAS. The one observed event along with the total hadron fluence as expected in the location of the SCAC were used calculate an SEL rate. The uncertainties are 68% confidence intervals about the mean for the measured SEL. The uncertainties in the spectra have been neglected. This rate range was then normalized to the total proton flux expected for ATLAS. Using this approach it was estimated that there will be 9^{+15}_{-5} SEL in the SCAC that instrument the electro-magnetic barrel calorimeter during the 10 years of ATLAS operation.

No latch-ups, or other permanent SEEs, were observed during any of the proton irradiations of the DMILL and DSM SCAC prototypes. The total proton fluence taken for the DSM device SEE tests was 6.64×10^{13} p/cm^2 and therefore the $\mathrm{RTC_{SEE}}$ has been satisfied for damaging, or permanent, SEEs for the DSM SCAC prototype. The DMILL device was irradiated to a proton fluence of 1.7×10^{12} p/cm^2.

8.7 Non-Ionizing Energy Loss Effects on the DSM Prototype

NIEL tests performed on the DSM prototype are included in this chapter for completeness, even though NIEL tests are not technically tests for SEEs. Neutron irradiations were performed on 10 DSM SCAC prototypes using the CERN PS/IRRAD2 facility. Ten de-

Energy (MeV)	Fluence (10^{10}p/cm^{-2})	N^{SEL} (95% CL)		Cross-sections (10^{-11}cm^2/device)	
		Lower	Upper	Lower	Upper
20.0	5.94	0	3.09	0	5.2
26.9	2.73	0	3.09	0	11.3
35.4	4.66	0	3.09	0	6.6
57.7	4.07	0	3.09	0	7.6
75.6	3.77	0	3.09	0	8.2
85.5	4.94	0	3.09	0	6.3
94.7	4.28	0	3.09	0	7.2
101.5	3.42	0	3.09	0	9.0
105.0	59.0	0.05	5.14	0.008	0.87

Table 8.16: Limits on the SEL cross-section in ATLAS at the 95% confidence level.

vices were irradiated to $(1.9 \pm 0.4)\times10^{13}$ n/cm^2 with two devices kept out of the radiation as controls. The devices absorbed approximately 70 Gy(Si) of TID and no effects due to the small dose were observed (the value of 70 Gy(Si) was provided by the staff of the PS/IRRAD2 and is lower than would be expected). The tests were performed in November, 2002 on behalf of the University of Alberta. In addition to these 10 devices, 4 earlier prototype DSM SCAC devices were irradiated to a higher 1 MeV equivalent in Si neutron fluence than the RTC_{NIEL} [100]. It was also possible to calculate the equivalent neutron fluence for the proton SEE tests. The relative NIEL values ($NIEL_p/NIEL_n$) at each energy were used to determine the equivalent fluence [98]. The corresponding values of NIEL are listed in Table 8.17. Only DUT #5 was irradiated to the required equivalent neutron fluence using protons.

8.8 Discussion of SEE Test Results

The ASIC prototype SCAC devices were affected to a lower degree than the COTS prototypes in terms of SEEs. The XC4036XLA FPGA demonstrated a saturation proton-induced SEU cross-section of $(1.3 \pm 0.2)\times10^{-10}$ cm^2/device in the logic circuit. This was significantly larger than the saturation SEU cross-section for the sum of correctable and uncor-

DUT #	Energy (MeV)	NIEL in Si (keV·cm^2)	NIEL$_p$/NIEL$_n$	p Fluence (10^{12}p/cm^2)	Equivalent n Fluence (10^{13}n/cm^2)
49	20.0	4.7	2.3	3.25	0.75
50	35.4	4.1	2.0	3.21	0.65
51	35.4	4.1	2.0	3.21	0.65
38	62.9	3.4	1.7	3.12	0.53
17	66.8	3.4	1.5	2.84	0.47
34	85.5	3.1	1.5	3.00	0.46
13	105.0	3.0	1.5	3.01	0.44
14	105.0	3.0	1.5	2.97	0.43
5	491.0	2.0	0.98	15.2	1.50
9	491.0	2.0	0.98	7.97	0.78
12	491.0	2.0	0.98	7.97	0.78
27	491.0	2.0	0.98	10.6	1.04

Table 8.17: 1 MeV equivalent in Si neutron fluences for proton data. The NIEL values have been normalized by the density of silicon.

rectable upsets for the DSM ASIC, which was measured to be $(1.6 \pm 0.4)\times10^{-13}$ cm^2/device[‡‡]. The greatest contribution to the SEU cross-section of the XC4036XLA device came from the underlying configuration switch matrix, which had a saturation cross-section of $(26 \pm 1)\times10^{-10}$ cm^2/device. Considering the 1,792 controllers used to instrument the electro-magnetic barrel calorimeter, and the spectra of all of the hadrons in the region of the FEBs, there would be approximately one SEU every 12 minutes of ATLAS operation for the configuration switches in the XC4036XLA device. Only SEUs that could not be corrected by the EDAC circuitry in the DSM SCAC would affect the data in ATLAS. There would be roughly one uncorrectable SEU every two months of contiguous operation. All of the upsets observed during the proton irradiations of the DMILL device appeared to be related to an analog circuit within the device. The circuit was disconnected after the test and no further proton testing was performed on the device. It was thus not possible to estimate an SEU rate for the DMILL device operating in ATLAS.

The XC4036XLA device experienced one SEL during the proton irradiation tests. This event occurred at 105 MeV. Using the one SEL event, and the lack of observation of such

[‡‡] A comparison between an FPGA circuit, not including the configuration switches, and an ASIC is appropriate as the FPGA logic circuit is a good approximation of an ASIC.

events at lower energies, an upper limit of 44 SELs occurring in the SCACs instrumenting the electro-magnetic barrel calorimeter was made (to a 95% CL). No destructive SEEs, including SELs, were observed during proton irradiations of either the DSM or DMILL SCACs.

Chapter 9

Summary

Five different prototype SCAC devices were tested following the procedure suggested by the ATLAS radiation tolerance group. Three commercially available re-programmable logic devices and two ASICs were exposed to various types of radiation to predict if they would operate in the ATLAS environment for 10 years. Figure 9.1 summarizes the results of these tests.

The TID tests performed on the EPF10K50E SCAC prototype in the x-ray facility showed a measurable increase in power supply current, drawn by the logic core of the device after a dose of between (682 $\pm$ 127) Gy(SiO_2) and (1040 $\pm$ 265) Gy(SiO_2) had been absorbed. The behaviour of the device during irradiation varied from piece to piece and showed evidence of failure that was observed as a leveling off in power supply current. The current drawn by the I/O circuitry of the device did not change during irradiation. Tests performed in the ^{60}Co facility showed no increase in power supply current drawn by either the logic core or I/O circuitry for doses up to (1.4 $\pm$ 0.4) kGy(SiO_2). It was likely that electrical problems related to the test board caused inconsistent results as the device would not operate without producing continuous errors following any of the irradiation periods. It would not be possible to suggest the EPF10K50 device for use in ATLAS without an understanding of how any electrical problems were affecting the device.

The TID test results for the XC2S150E SCAC prototype were more consistent from piece to piece than those of the EPF10K50E prototype. The current drawn by the core logic

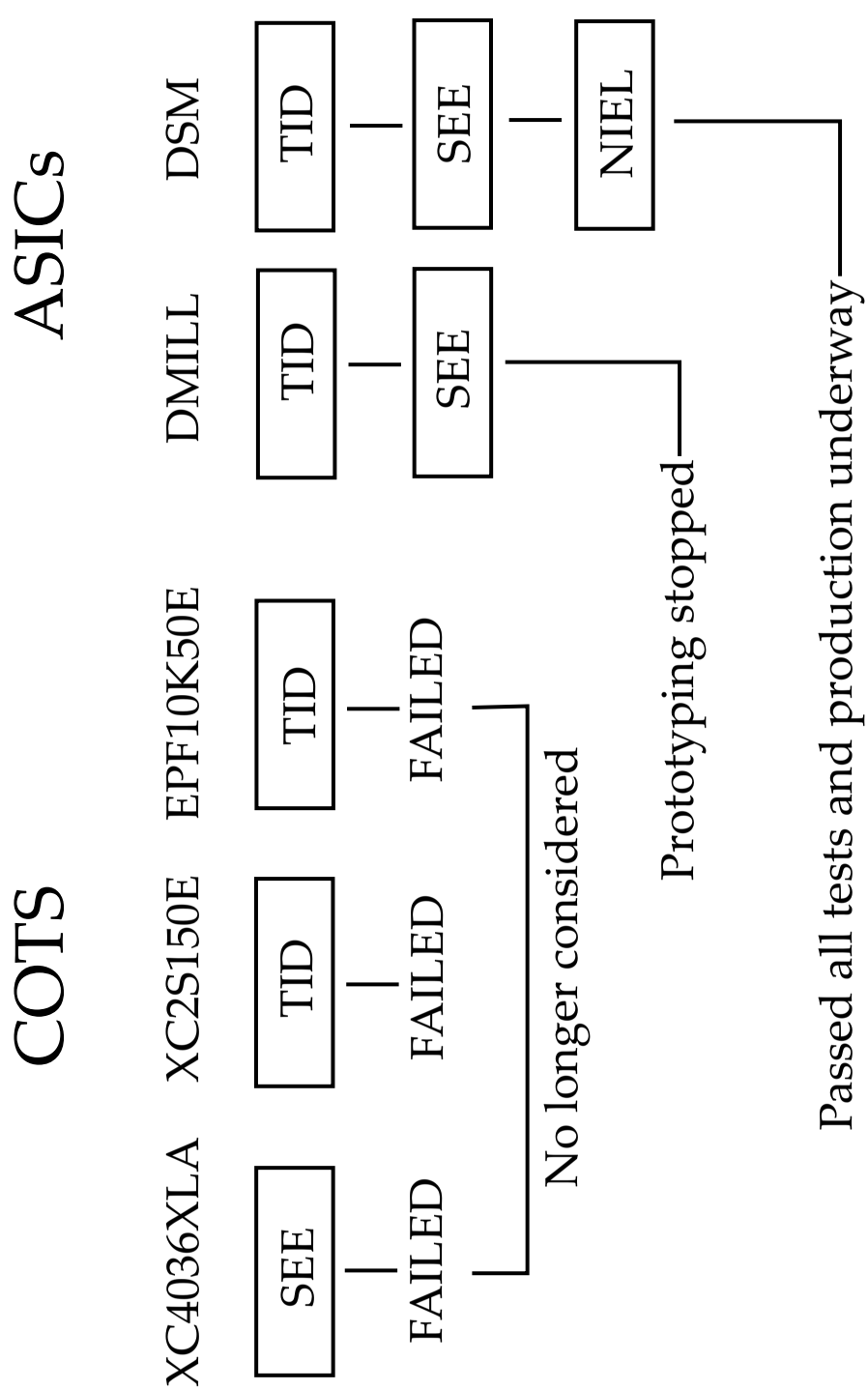


Figure 9.1: Diagram summarizing the test results and termination points of prototype testing.

began to measurably increase at doses between (317 $\pm$ 55) Gy(SiO_2) and (341 $\pm$ 59) Gy(SiO_2), and in the I/O logic between (375 $\pm$ 64) Gy(SiO_2) and (410 $\pm$ 68) Gy(SiO_2). The behaviour under x-ray irradiation varied little from piece to piece.

Neither of the two COTS prototypes tested for TID effects tolerance operated near the required dose of 2.76 kGy(SiO_2). Both devices showed no increases in power supply current for doses far greater than the 39.4 Gy(SiO_2) expected in their location within ATLAS during ten years of operation. If the safety factor for COTS devices was reduced it is conceivable that COTS devices would be sufficiently TID tolerant to permit their use in ATLAS. The EPF10K50E appeared to be more TID tolerant and could be chosen for use in ATLAS if a safety factor of 20 (a reduction of 3.5 times the current value) was acceptable.

An XC4036XLA FPGA prototype of the SCAC device was exposed to protons with energies between 20 MeV and 105 MeV in order that SEEs could be examined. The SEU cross-section was measured for the circuit, switches, and total device. The saturation cross-sections were found to be (1.3 $\pm$ 0.2) $\times 10^{-10}$cm^2/device, (26 $\pm$ 1) $\times 10^{-10}$cm^2/device, and (27 $\pm$ 1) $\times 10^{-10}$cm^2/device for the circuit, switches, and total device respectively. The threshold energies were measured to be (22 $\pm$ 3) MeV for the circuit, (22 $\pm$ 4) MeV for the switches, and (22 $\pm$ 2) MeV for the total device. Assuming 1,792 SCAC devices to instrument the electro-magnetic barrel calorimeter, and considering the fluxes of all of the hadrons, there would be an upset in the configuration switches of a SCAC every 12 minutes on average. The mean time between upsets for the circuit of the SCAC implemented in the XC4036XLA FPGA would be about 4 hours. One SEL was observed at 105 MeV during proton tests of the device. Using this event and the fact that no SELs were observed at lower energies, an estimate of the SEL rate for proton-induced SEL was made. For the 1,792 controllers in the electro-magnetic barrel calorimeter, the mean time between SEL was estimated between 25 days and 439 yr of operation at the 95% confidence level. As it would not be possible to access the detector and replace any devices that might become damaged due to latch-up, the use of the XC4036XLA could not be considered for use in ATLAS.

The radiation-hardened DMILL ASIC prototype device was subjected to x-ray and proton irradiations. The device absorbed a TID of (2.3 $\pm$ 0.4) kGy(SiO_2) with no measurable effect observed. This was a significantly higher dose than the 414 Gy(SiO_2) dose that

was required. Single event effect testing was performed on the DMILL prototype and the only SEUs observed appeared to be a result of an electrical problem with a part of the circuit. Due to high cost and a more attractive alternative – the DSM device – the DMILL implementation of the SCAC device was abandoned before further conclusive SEE testing was performed.

The device ultimately chosen on which to implement the SCAC for the ATLAS LAr FEB was the deep sub-micron ASIC. The DSM SCAC prototype was tested rigorously to ensure that it passed all of the ATLAS requirements. Several DSM devices were exposed to x-rays (12 devices) and protons (12 devices) to absorbed doses of (0.38 $\pm$ 0.05) kGy(SiO_2) to (20.00 $\pm$ 2.75) kGy(SiO_2) . The largest change in power supply current was about a 3.5% drop during the 20 kGy(SiO_2) x-ray irradiation. No degradation in device operation was observed during, or after, the TID tests. The SEU proton-induced cross-section was determined for the DSM SCAC and the saturation cross-section and threshold energy were determined to be (16 $\pm$ 4)$\times 10^{-12}$ cm^2/device and (54 $\pm$ 12) MeV respectively for the total upsets. The saturation cross-section and threshold energy were determined to be (0.5 $\pm$ 0.1)$\times 10^{-12}$ cm^2/device and (44 $\pm$ 24) MeV respectively for the uncorrectable upsets. An estimate of the MTBU for uncorrectable SEU upsets rate for all of the SCACs in the electro-magnetic barrel gave a value of 66 days. No permanent SEEs, such as SEL, were observed up to a fluence of 6.64$\times 10^{13}$ which was more than 20 times the required value of R_{SEE}. It is not expected that damaging SEEs will cause problems for operation of the SCAC in ATLAS. Ten of the DSM prototypes were irradiated with neutrons to a fluence of (1.9 $\pm$0.4) n/cm^2 and demonstrated no measurable damage. The proton-induced SEU cross-section at 491 MeV was examined to observe the extent, if any, of the angular dependence on the cross-section. The total (correctable and uncorrectable) SEU cross-section showed a gradual increase of about 27% in total from of the value at 0^o . Insufficient statistics prevented the conclusive determination of the angular dependence of the uncorrectable SEU cross-section.

While it is clear that the DSM SCAC prototype examined surpassed all of the requirements stipulated by the ATLAS radiation tolerance group, it was only the version of the prototype that was used for the qualification process. A pre-production version of the DSM SCAC has been submitted for fabrication and the production of the devices to be

installed in the ATLAS detector is expected in the end of 2003. Testing will need to be performed on these devices as well. It should be possible to ascertain if the process has changed by examining the SEU cross-section for both correctable and uncorrectable upsets, or during functional testing that will take place independent of the radiation tests. It is a fact, however, that only upsets that are uncorrectable will affect the performance of the SCAC within ATLAS. It is thus imperative that more data be taken to fully understand and further constrain the uncorrectable SEU behaviour of the device. This would mean that a better determination of the angular dependence of the uncorrectable SEU cross-section would need to be made. The energy of the proton beams at the PIF are sufficient to measure the saturation cross-section for any of the devices that were examined for this thesis, but it was difficult to make high-statistics measurements on devices that were more SEE tolerant, such as the DSM device. It is unlikely that it would be possible to use the PIF to obtain sufficient statistics to precisely determine either the shape of the uncorrectable SEU cross-section or the angular dependence of the uncorrectable SEU cross-section for the DSM device. This suggests the need to move to a higher flux proton facility for SEE testing of the DSM device, such as the cyclotron located at the Northeast Proton Therapy Center in Boston.

The two photon irradiated COTS devices both demonstrated TID tolerances to doses that greatly exceeded the projected total dose in the region. Due to the large safety factors used when determining the RTC for TID in COTS devices, neither of these COTS devices could be chosen for use in ATLAS. If the safety factor could be reduced (by purchasing devices from a single lot, for example) it may be possible for COTS devices to be used in ATLAS. If COTS devices are purchased from a single lot, and the effect of low dose rate on devices was understood, a reduced safety factor might be acceptable.

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Appendix A

Acronym Glossary

ASIC	Application Specific Integrated Circuit
ATLAS	A Toroidal LHC Apparatus
BCID	Bunch Crossing Identifier
BJT	Bipolar Junction Transistor
CCI	Cross Cancer Institute
CEA	Commissariat a l'Energie Atomique
CDF	Cumulative Distribution Function
CL	Confidence Level
CMOS	Complimentary Metal Oxide Semiconductor
COTS	Commercial Off The Shelf
CPLD	Complex Programmable Logic Device
CSR	Centre for Subatomic Research
DAM	Direction Des Millitaires
DAQ	Data Acquisition
DMILL	Durci Mixte Isolant Logico Lineaire (Hardened Mixed Isolating Linear Logic)
DMM	Digital Multi-meter
DOF	Degree of Freedom
DSM	Deep Sub-micron
DUT	Device Under Test
FEB	Front-end Board
FET	Field Effect Transistor
FIFO	First In First Out (pipeline)
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
HVL	Half Value Layer
kVp	Peak kilo-voltage
LAr	Liquid Argon (used to refer to the liquid argon calorimeter)
LHC	Large Hadron Collider
LVDS	Low Voltage Differential Signals
LVTTL	Low Voltage Transistor-Transistor Logic

MOSFET	Metal Oxide Silicon Field Effect Transistor
MTBU	Mean Time Between Upsets
NIEL	Non-Ionizing Energy Loss
NMOS	n-channel MOS
PC	Printed Circuit
PIF	Proton Irradiation Facility
PLD	Programmable Logic Device
PMOS	p-channel MOS
PN	Positive - Negative (as in PN-junction)
POR	Power On Reset
RAM	Random Access Memory
RMS	Root Mean Squared
ROD	Readout Driver
RTC	Radiation Tolerance Criteria
SCA	Switched Capacitor Array
SCAC	Switched Capacitor Array Controller
SEB	Single Event Burn-out
SEE	Single Event Effect
SEGR	Single Event Gate Rupture
SEL	Single Event Latch-up
SEU	Single Event Upset
SF	Safety Factor
SRAM	Static Random Access Memory
SRL	Simulated Radiation Level
TID	Total Ionizing Dose
TRIUMF	Tri University Meson Factory
TTCrx	Trigger and Timing Control Receiver Chip
TTL	Transistor-Transistor Logic

Appendix B

Raw Data

This appendix contains a record of all data collected during the period described in this thesis. The first section contains a list of all test periods and where data was recorded. The parameters used for each test performed at the PIF are tabulated in the second part of this appendix.

B.1 Data by Date

The devices tested are listed in Tables B.1–B.2. The numbers assigned to the devices were arbitrary and had nothing to do with manufacturer codes or date codes. The date ranges refer to the periods during which testing was performed on the device. They do not necessarily represent a single test. Where specific test periods are relevant they will be discussed within the text. Table B.1 is a list of the EPF10K50E CPLDs, XC4036XLA FPGAs, XC2S150E FPGAs and DMILL radiation-hardened ASICs tested. The DSM devices tested are listed in Table B.2.

Device	ID #	Test Type	Facility	Date(s) Tested
EPF10K50E	3	TID	^{60}Co	14/05/2001 - 12/06/2001
EPF10K50E	4	TID	^{60}Co	04/09/2001 - 27/09/2001
EPF10K50E	1	TID	x-ray	17/10/2001
EPF10K50E	5	TID	x-ray	01/11/2001
EPF10K50E	0	TID	x-ray	02/11/2001
EPF10K50E	2	TID	x-ray	04/11/2001
EPF10K50E	6	TID	^{60}Co	13/11/2001 - 09/12/2001
XC4036XLA	1	SEE	PIF	14/06/1999
XC4036XLA	2	SEE	PIF	14/06/1999
XC4036XLA	1	SEE	PIF	31/10/1999
XC4036XLA	1	SEE	PIF	12/06/2000
XC4036XLA	2	SEE	PIF	12/06/2000
XC4036XLA	3	SEE	PIF	12/06/2000
XC4036XLA	4	SEE	PIF	12/06/2000
XC4036XLA	5	SEE	PIF	12/06/2000
XC4036XLA	6	SEE	PIF	12/06/2000
XC2S150E	3	TID	x-ray	17/12/2001
XC2S150E	10	TID	x-ray	25/1/2002
XC2S150E	13	TID	x-ray	7/3/2002
XC2S150E	14	TID	x-ray	14/3/2002
DMILL	4	SEE	PIF	20/8/2001
DMILL	5	SEE	PIF	20/8/2001
DMILL	7	SEE	PIF	20/8/2001
DMILL	9	SEE	PIF	20/8/2001

Table B.1: EPF10K50E, XC4036XLA, XC2S150E and DMILL devices tested. The ID numbers where arbitrarily assigned to devices during testing for bookkeeping reasons.

Device	ID #	Test Type	Facility	Date(s) Tested
DSM	13	SEE	PIF	8/6/2002
DSM	14	SEE	PIF	8/6/2002
DSM	17	SEE	PIF	8/6/2002
DSM	34	SEE	PIF	8/6/2002
DSM	38	SEE	PIF	8/6/2002
DSM	49	SEE	PIF	9/6/2002
DSM	50	SEE	PIF	9/6/2002
DSM	51	SEE	PIF	9/6/2002
DSM	5	SEE	PIF	4/9/2002
DSM	9	SEE	PIF	4/9/2002
DSM	12	SEE	PIF	5/9/2002
DSM	27	SEE	PIF	5/9/2002
DSM	10	TID	x-ray	22/5/2002
DSM	32	TID	x-ray	27/5/2002
DSM	58	TID	x-ray	18/6/2002
DSM	56	TID	x-ray	26/6/2002
DSM	69	TID	x-ray	8/7/2002
DSM	155	TID	x-ray	17/7/2002
DSM	82	TID	x-ray	25/7/2002
DSM	81	TID	x-ray	1/8/2002
DSM	87	TID	x-ray	6/8/2002
DSM	93	TID	x-ray	20/8/2002
DSM	71	TID	x-ray	28/10/2002
DSM	104	NIEL	PS/IRRAD2	Nov. 2002
DSM	105	NIEL	PS/IRRAD2	Nov. 2002
DSM	109	NIEL	PS/IRRAD2	Nov. 2002
DSM	110	NIEL	PS/IRRAD2	Nov. 2002
DSM	112	NIEL	PS/IRRAD2	Nov. 2002
DSM	113	NIEL	PS/IRRAD2	Nov. 2002
DSM	114	NIEL	PS/IRRAD2	Nov. 2002
DSM	115	NIEL	PS/IRRAD2	Nov. 2002
DSM	116	NIEL	PS/IRRAD2	Nov. 2002
DSM	118	NIEL	PS/IRRAD2	Nov. 2002

Table B.2: DSM devices tested. The ID numbers where arbitrarily assigned to devices during testing for bookkeeping reasons.

Run #	DUT #	Proton Energy (MeV)	Range Setting	Scaler (Counts)	Upsets
1	1	59.0 ± 0.6	0	196000	1
2	1	59.0 ± 0.6	0	23000	1
3	1	59.0 ± 0.6	0	11400	0
4	1	59.0 ± 0.6	0	33360	1
5	2	59.0 ± 0.6	0	32990	1
6	2	26.0 ± 1.5	2050	33880	1
7	2	40.0 ± 1.0	1650	33100	1
8	2	40.0 ± 1.0	1650	8200	1

Table B.3: Data gathered during research trip to TRIUMF PIF in June, 1999. Beam-line 2C was used with the primary proton energy set at approximately 70 MeV. The upsets all occured in the configuration switches of the device.

B.2 SEE Data Run Parameters

A list of all of the data taken at the PIF is contained in Tables B.3–B.9. The data is organized sequentially by run number. Data was obtained on 6 different occasions for three different devices during the period between June 1999 and September 2002. Table B.3 contains the data taken in June 1999 with the XC4036XLA FPGA. Both of the available primary energies for beam-line 2C, 116 MeV and 70 MeV, were used to allow the proton induced single event upset rate to be measured over as wide an energy range as possible. The device was located in the standard position (refer to Section 5.4).

Table B.4 contains the data taken in October, 1999 with the XC4036XLA FPGA. The data was again taken using both primary beam energies of beam-line 2C and was located in the standard position.

A final test was performed at the PIF in order to make high-statistics measurements of the proton induced SEU cross-section of the XC4036XLA FPGA. Tables B.5 and B.6 contain the data taken during this test. The position and primary beam energies used were the same as in the two previous tests.

The DMILL ASIC was tested at the PIF for the purpose of detecting SEEs. The device was irradiated using 68.0 MeV protons in the standard position in beam-line 2C. Table B.7 contains the data taken for this test.

Run #	DUT #	Proton Energy (MeV)	Range Setting	Scaler (Counts)	Upsets	
					Switch	Circuit
1	1	56.0 ± 0.7	200	30000	8	0
2	1	46.0 ± 0.8	900	60000	8	0
3	1	31.0 ± 1.2	1800	60000	1	0
4	1	40.0 ± 1.0	1100	60000	3	0
5	1	51.0 ± 0.7	700	60000	10	0
6	1	101.0 ± 0.8	200	50000	10	0
7	1	72.0 ± 1.0	3300	50000	10	0
8	1	83.0 ± 0.9	2200	50000	8	1
9	1	92.0 ± 0.9	1200	50000	7	0

Table B.4: Data collected at the TRIUMF Proton Irradiation Facility in October, 1999. The runs with proton energy greater than 60 MeV were taken with the higher beam energy available for beam-line 2C.

Run #	DUT #	Proton Energy (MeV)	Range Setting	Scaler (Counts)	Upsets	
					Switch	Circuit
3	2	57.7 ± 0.6	200	178000	26	0
4	2	57.7 ± 0.6	200	443641	87	0
5	2	57.7 ± 0.6	200	105702	101	0
6	2	35.4 ± 1.1	1650	462668	29	0
7	2	35.4 ± 1.1	1650	798771	85	8
8	2	35.4 ± 1.1	1650	171838	100	8
9	2	26.9 ± 1.5	2050	353151	14	0
10	2	26.9 ± 1.5	2050	212872	21	0
11	2	26.9 ± 1.5	2050	204403	33	0
12	2	26.9 ± 1.5	2050	321753	48	4
14	3	20.0 ± 1.8	2300	1000312	13	0
15	3	20.0 ± 1.8	2300	1000224	29	0
16	3	20.0 ± 1.8	2300	967727	46	1
18	4	18.0 ± 2.1	2400	2000907	17	1

Table B.5: The raw data set from the June 2000 test of the Xilinx XC4036XLA FPGA at the TRIUMF proton irradiation facility. The data in this table was taken using a primary proton beam energy of 70 MeV.

Run #	DUT #	Proton Energy (MeV)	Range Setting	Scaler (Counts)	Upsets	
					Switch	Circuit
23	6	101.5 ± 0.8	200	216644	48	3
24	6	101.5 ± 0.8	200	115627	79	4
25	6	101.5 ± 0.8	200	82723	95	6
26	6	85.5 ± 1.0	2000	185181	20	0
27	6	85.5 ± 1.0	2000	72031	29	1
28	6	85.5 ± 1.0	2000	475243	95	2
30	6	75.6 ± 1.1	3000	191790	27	3
31	6	75.6 ± 1.1	3000	67050	33	3
32	6	75.6 ± 1.1	3000	178776	63	3
33	6	75.6 ± 1.1	3000	122546	77	3
34	6	75.6 ± 1.1	3000	79404	88	3
35	6	105.0 ± 0.7	0	66783	12	0
36	6	105.0 ± 0.7	0	165570	47	2
37	6	105.0 ± 0.7	0	160247	80	4
38	6	105.0 ± 0.7	0	71469	91	4
39	1	94.7 ± 0.8	1000	463725	71	7
40	1	94.7 ± 0.8	1000	110644	91	7

Table B.6: The raw data set from the June 2000 test of the Xilinx XC436XLA device at the TRIUMF proton irradiation facility. The data in this table was taken using a primary proton beam energy of 116 MeV.

Run #	DUT #	Energy (MeV)	Range Setting	Scaler (Counts)
1	4	68.0 ± 0.5	0	666080
7	4	68.0 ± 0.5	0	613124
10	4	68.0 ± 0.5	0	718425
11	4	68.0 ± 0.5	0	727451
12	4	68.0 ± 0.5	0	701525
13	5	68.0 ± 0.5	0	117374
14	5	68.0 ± 0.5	0	699194
15	5	68.0 ± 0.5	0	713706
16	5	68.0 ± 0.5	0	513834
17	5	68.0 ± 0.5	0	720968
18	5	68.0 ± 0.5	0	657235
19	5	68.0 ± 0.5	0	712235
22	7	68.0 ± 0.5	0	847770
23	7	68.0 ± 0.5	0	740224
24	7	68.0 ± 0.5	0	742150
25	7	68.0 ± 0.5	0	743695
26	7	68.0 ± 0.5	0	747324
27	9	68.0 ± 0.5	0	666058
28	9	68.0 ± 0.5	0	635965
29	9	68.0 ± 0.5	0	634535
30	9	68.0 ± 0.5	0	637830
31	9	68.0 ± 0.5	0	633080

Table B.7: Data taken with DMILL ASIC at the TRIUMF PIF for upset rate measurements. All data was taken with a proton energy of 68 MeV.

Run #	DUT #	Energy (MeV)	Range Setting	Scaler (Counts)	Upsets	
					Correctable	Uncorrectable
1	13	105.0 ± 0.7	0	70083	36	2
2	14	105.0 ± 0.7	0	90000	38	2
3	17	66.8 ± 1.2	3800	129000	34	0
4	34	85.5 ± 1.0	2000	110000	38	0
5	13	105.0 ± 0.7	0	21000	8	2
6	38	62.9 ± 0.5	0	115800	31	0
7	49	20.0 ± 1.8	2300	250000	1	1
8	50	35.4 ± 1.1	1650	188680	7	0
9	51	35.4 ± 1.1	1650	188680	11	0

Table B.8: Data taken with DSM ASIC at the TRIUMF PIF for upset rate measurements in June, 2002.

A final prototype, the DSM version, was tested at the PIF for the purpose of detecting SEEs. The device was irradiated using both the high and low primary energy settings of beam-line 2C. To obtain a sufficient proton fluence the irradiations were performed in the high intensity location. Table B.8 contains the data taken for this test. A second test of the DSM prototype was performed in September, 2002 for the purpose of exposing the device to high energy (491 MeV) protons. This data is contained in Table B.9. An additional column has been added that contains the angle of the incident beam relative the normal to the device face.

Run #	DUT #	Energy (MeV)	Range Setting	Scaler (Counts)	Angle (Degrees)	Upsets	
						Correct.	Uncorrect.
1	5	491 ± 5	0	999272	0	76	7
2	5	491 ± 5	0	701062	0	31	3
3	5	491 ± 5	0	999265	0	52	4
4	5	491 ± 5	0	999272	50	0	0
5	5	491 ± 5	0	999283	50	78	6
6	5	491 ± 5	0	999307	50	65	3
7	5	491 ± 5	0	999319	0	70	9
8	9	491 ± 5	0	999311	50	81	1
9	9	491 ± 5	0	999313	90	80	10
10	9	491 ± 5	0	999239	180	86	8
11	12	491 ± 5	0	999272	25	74	7
12	12	491 ± 5	0	999345	25	64	1
13	12	491 ± 5	0	999326	25	71	1
14	27	491 ± 5	0	999354	90	69	9
15	27	491 ± 5	0	999244	90	74	3
16	27	491 ± 5	0	999289	180	68	3
17	27	491 ± 5	0	999302	180	85	7

Table B.9: Data taken with DSM ASIC at the TRIUMF PIF for upset rate measurements in September, 2002.

Appendix C

Radioactivity and Dose Units

It is important to have an understanding of radioactivity and dose units when approaching a text on radiation studies of any type. Radiation units are arguably the most misused units in science. One complication that has led to this misuse is the use of SI (Systeme International) units within the last 20 years, which has essentially doubled the number of units. While SI units are primarily used in this thesis, both SI and traditional units will be covered for completeness. A second cause of the misuse of radiation units is the lack of understanding of the difference between radiation field and radiation effect.

Radiation units can be effectively divided into two categories, those pertaining to the source, regardless of effect, and those pertaining to the absorbing medium. Both activity and intensity relate to the source while absorbed dose refers to the effect on the medium. There are also units which specifically relate to the damage on humans. It makes the most sense to begin with the units describing the activity of the source. All of the discussion on units in this section was condensed from Ref. [120] unless otherwise stated.

The activity of a source is the number of nuclear decays per unit of time. The traditional unit of activity is the curie (Ci) which is measured as the activity due to 1 g of radium, or 3.7×10^{10} nuclear decays per second. Table C.1 summarizes all of the units described in this appendix. The SI unit for activity is the bequerel (Bq) and is equal to 1 nuclear decay per second.

When radiation is aligned into a beam, the corresponding measure of radiation field

strength is the flux. Flux is the number of particles passing through a unit area per unit of time and has units of $cm^{-2}s^{-1}$. The time integrated flux is called the fluence and has units of cm^{-2}.

One of the first properties of gamma radiation measured was the ionization of air by x-rays. The amount of ionization in air led to a measure of radiation field intensity, or more commonly, exposure. The traditional unit for the intensity is the roentgen (R). The roentgen is defined as the amount of radiation which will produce 1 electrostatic unit of charge (esu)* in 1 cm^3 of air at standard temperature and pressure (stp)†. The similar measure in SI units is the unnamed quantity of C/kg. One roentgen is exactly equal to 2.58×10^{-4} C/kg.

Unlike the units for activity and exposure, the units for dose depend on the material under irradiation. For example, under identical irradiation conditions, a block of lead and a block of Plexiglas (of the same size) would absorb different amounts of energy‡. The traditional unit of dose is the (rad). It is equivalent to the absorption of 100 ergs per g of material. The SI equivalent unit is the Gray (Gy), which is given as the absorption of 1 J per kg of the material. The unit of absorbed dose is given with the absorbing material following in parentheses, such as Gy(SiO_2) for silicon dioxide. The reason for this is that the amount of ionizing dose deposited in a material is dependent on that material.

A measure of non-ionizing energy loss (NIEL) damage inflicted on a material from a fluence of hadrons is the number of 1 MeV neutrons that would cause the same number of atomic displacements in the same material. A hadron fluence with a particular energy distribution will therefore be described by the 1 MeV equivalent neutron fluence. This measure is material dependent and the material must be included in the unit, i.e. 1 MeV equivalent in Si neutron fluence.

*The electrostatic unit of charge is equivalent to 3.336×10^{-10} coulombs.

†The conditions described by standard temperature and pressure for a gas are a temperature of 273.15 K and a pressure of 101.325 kPa.

‡It is here assumed that a block is large enough that variations, due to the stochastic nature of radiation, between blocks of the same size can be neglected.

Unit	Describes	Definition	Conversion
curie (Ci)	Activity	3.7×10^{10} decay/s	3.7×10^{10} Bq
bequerel (Bq)	Activity	1 decay/s	2.7×10^{-11} Ci
$cm^{-2}s^{-1}$	Flux	beam intensity	N/A
cm^{-2}	Fluence	time integrated beam intensity	N/A
roentgen (R)	Exposure	1 esu/cc air (stp)	2.58×10^{-4} C/kg
(C/kg)	Exposure	1 C/kg air (stp)	3.88×10^{4} R
Rad (rad)	Dose	100 erg/g (material)	0.01 Gy
Gray (Gy)	Dose	1 J/kg (material)	100 rad
Rem (rem)	Biological Dose	1 rad$\times$Q factor	0.01 Sv
Sievert (Sv)	Biological Dose	1 Gy$\times$Q factor	100 rem

Table C.1: Radiation units, with descriptions and conversions.

Appendix D

X-ray Dosimetry

This appendix describes the method used to measure the dose rate for devices irradiated in the x-ray facility. Dosimetry was performed by placing an ionization chamber under the DUT and measuring the counts* associated with the ion chamber. Figure D.1 shows a diagram, and Figure D.2 shows a photograph of the ion chamber placement relative to the DUT during dosimetry. In order to remove the effect of the top of chip socket, the lid was left open, with the device held in place with tape, during dosimetry measurements. This was not required for the DSM device as there was no top on the socket. Measurements were also made with the device removed from the socket. The reason for this approach was that the ion chamber would not fit above the DUT and thus all measurements had to be made with the chamber placed below the DUT and PC board. The dose absorbed at the die of the device was required and thus the effects of the packaging, socket, and PC board had to be accounted for and removed. More details on the method of calculating the dose are given in the next section.

Figure D.3 shows the readout electronics and the power source for the ion chamber. The ion chamber was powered by a -300 V DC battery. Current from the ion chamber was transferred to a current integrator using a coaxial cable. The cable attached to the ion chamber was a special tri-axial cable that carried the DC power to the chamber and the signals from it. A connector box was made to interface with the tri-axial cable and the

*Each count corresponded to a fixed amount of integrated charge.

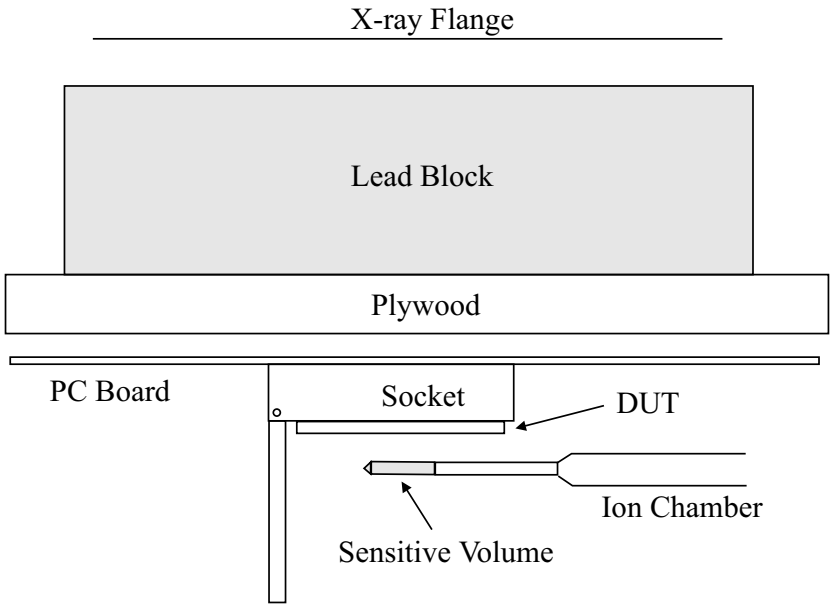

Figure D.1: Diagram of ion chamber placement during x-ray dosimetry.

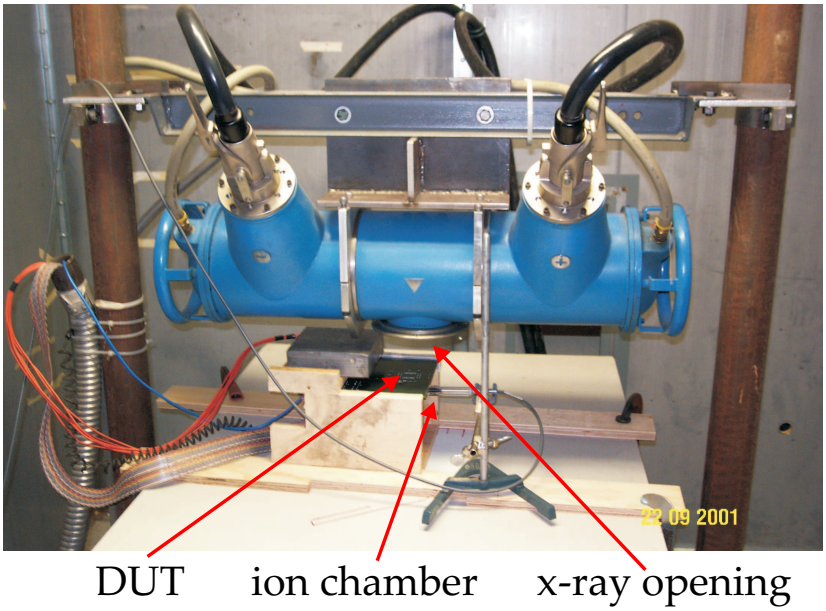

Figure D.2: Photograph of ion chamber placement during x-ray dosimetry.

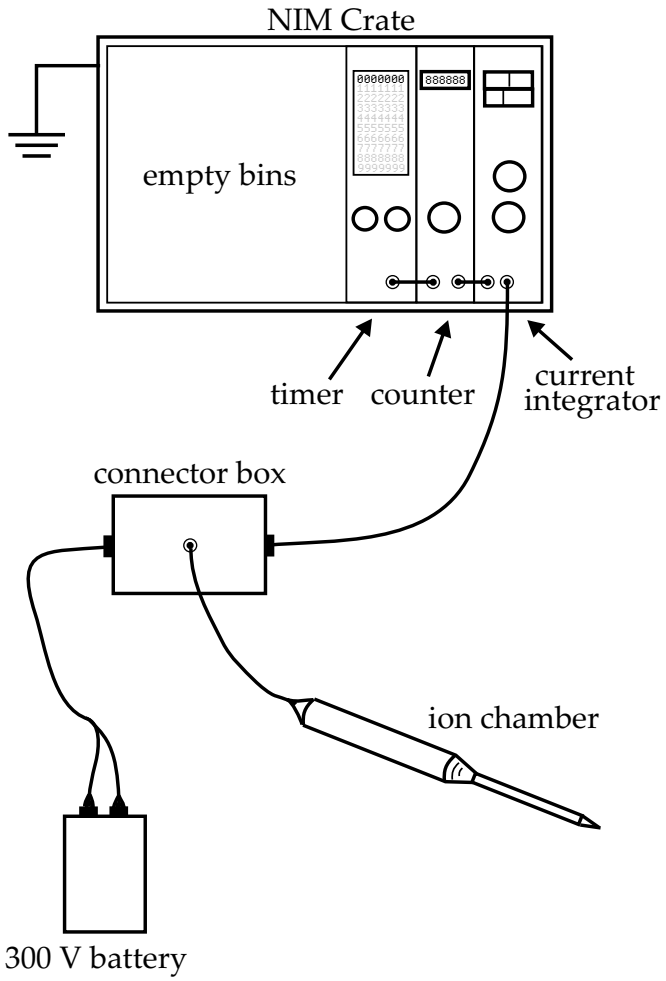

Figure D.3: Schematic of ion chamber readout and power source.

battery and readout electronics. Three NIM modules were used for the chamber readout: a current integrator, a pulse counter, and a timer. A discriminator setting on the integrator ensured that electronic noise did not contribute to the readout values. When the timer was turned on a pulse was sent to the counter which began counting the pulses coming from the integrator. When the timer was turned off, the counting was terminated.

D.1 Calculation of Total Ionizing Dose in Silicon Dioxide from an X-ray Source

This section describes the calculation of the dose absorbed by the oxides within the devices irradiated and includes a description of the procedure for calibrating the chamber readout system.

D.1.1 Calculation Details

The rate of dose absorption in the device under test was calculated by determining the dose rate above and below it. The dose rate is less than that above the DUT and greater than that below the DUT. Once the dose rate above and below the device were determined, the average of the two was taken to be the dose at the die of the device under test.

The first step in determining the dose rate was to measure the exposure rate above and below the DUT using a calibrated ion chamber. Due to the physical geometry of the test arrangement (Figure D.1), the exposure rate above the device had to be estimated from a measurement made in the position below the DUT. To reduce the uncertainty in this estimate the exposure rate was measured below the DUT socket with the DUT in place and again with it removed from the socket. A correction (described below) was then made to the exposure rate, with the DUT removed, to account for the offset from the desired position.

The counts coming from the current integrator had to be converted to units of exposure in air. The uncertainty in the counts measured per minute was estimated to be 1 count. The exposure rate was then converted to units of dose in SiO_2. The conversion between counts coming from the ion chamber and dose in SiO_2, including spatial corrections, was given by:

$$\dot{\mathrm{D}}(\mathrm{SiO_2}) = \frac{N \cdot C_{cal} \cdot C_{x2d} \cdot C_{mat} \cdot C_{dst} \cdot 60}{100}, \tag{D.1}$$

where $\dot{\mathrm{D}}(\mathrm{SiO_2})$ was the absorbed dose rate in Gy(SiO_2)/hr, N was the number of counts registered during the dosimetry time (1 minute), C_{cal} was the calibration constant relating measured counts to exposure rate, C_{x2d} was the constant to convert from exposure in air to dose in rad(air), C_{mat} was the constant to convert from dose in air to dose in SiO_2, and

Correction Factor	Measured Values
C_{cal}	0.672 ± 0.005
C_{x2d}	0.86
C_{mat}	1.51 ± 0.04
C_{dst} (bottom of DUT)	1.03 ± 0.02
C_{dst} (top of DUT)	1.06 ± 0.02

Table D.1: Constants used in the conversion from ion chamber counts/minute to krad/hr.

C_{dst} was the value of the spatial correction. The values of the constants in equation D.1 are described below and summarized in Table D.1. The remaining factors of 60 and 100 in equation D.1 convert from minutes to hours and rads to gray.

D.1.2 Calibration Constant

The x-ray facility at the Cross Cancer Institute (CCI) was utilized to calibrate the ionization chamber that was used for the dosimetry described in this thesis. The CCI x-ray facility is located on the south edge of the University of Alberta campus. Their chamber was calibrated by the National Research Council of Canada in Ottawa to a 1% accuracy.

Equipment Used in Calibration

Figure D.4 illustrates the layout of the ionization chamber and readout system with respect to the CCI facility. Due to the length of the cable connecting the ion chamber to the electrical box, which was approximately 2 meters in length [121], the electrical box was left in the radiation area with the ion chamber. The battery was left in the radiation area for the same reason. Three coaxial cables were connected together to transmit the signals coming from the chamber. There were 20 meters between the chamber in the radiation area and the readout system located outside the area.

Meteorological Measurements

The pressure and temperature were measured in order that a correction for the mass of air contained in the volume could be accounted for [122]. The reason for this correction was

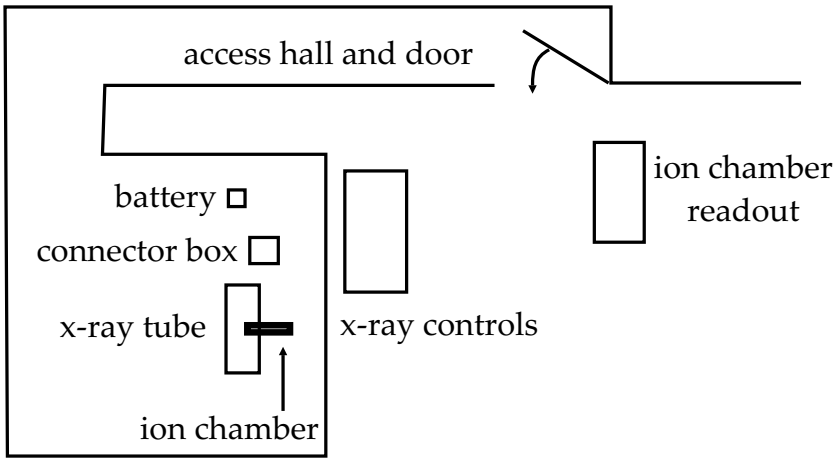

Figure D.4: Layout of the ion chamber and readout system at the CCI x-ray facility for the calibration procedure. Diagram is not to scale.

that the calibrations obtained for the CCI ion chamber, which were being compared with, were made at a temperature and pressure, of 23.2 ^{o} C and 1 atmosphere (760 mmHg), respectively. Using the ideal gas law, the corresponding correction was then given by

$$C_{PT} = \frac{P_{ref}}{P} \cdot \frac{(T[^oC] + 273.2)}{T_{ref}[^oC] + 273.2}. \tag{D.2}$$

The temperature and pressure measured during the calibration were (22.7 $\pm$ 0.2) ^{o}C and (705.00 $\pm$ 0.05) mmHg, which gave a correction value of 1.0762 $\pm$ 0.0007.

The temperature was measured at the CCI by a thermometer. This thermometer was located in the radiation area and checked against a more accurate thermometer on occasion. The pressure was measured by a barometer located just outside the radiation area. This barometer was last calibrated in December, 2001. Moisture was not measured at the CCI. The variation in humidity will only affect the chamber output by a maximum of 1%, and between relative humidity values of 15% and 80% the corresponding correction factor has a fixed value of 0.997 [123].

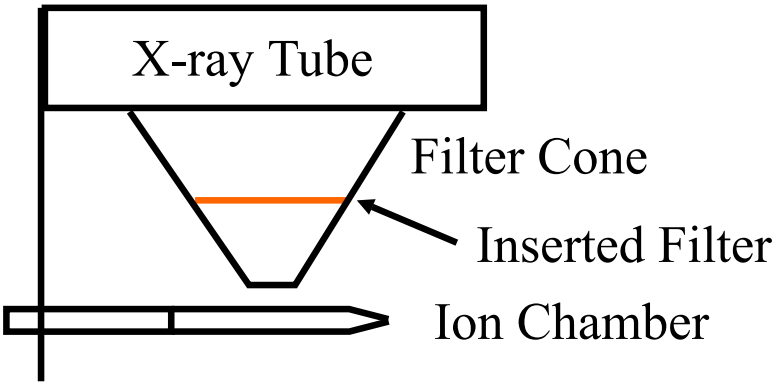

Figure D.5: The position of the ion chamber with respect to the x-ray tube and filter cone. The spatial offset between the tip of the filter cone and the center of the ion chamber was 5 mm. Not to scale.

Output Measurement for CSR Chamber and Readout

The first step of the calibration was to measure the output of the CSR system at fixed accelerating voltages (corresponding to particular half-value layers[†] (HVLs)) in the CCI x-ray facility. The chamber position relative to the x-ray tube is shown in Figure D.5.

The ionization chamber was mounted through a Plexiglas plate, which was attached to the x-ray tube housing. The displacement between the tip of the filter cone and the center of the CSR ionization chamber was 5 mm. A correction factor of 1.0336 was required to account for the spatial displacement between the chamber and the point at which the CCI calibrations were made (the tip of the filter cone). The cone used was a 10 cm by 10 cm unit.

Calibrations were made for five accelerating voltages. Each voltage had associated with it a particular HVL to give a corresponding beam quality, or hardness. Beam hardness refers to how mono-energetic the photons within it are. The x-ray control system at the CCI would not allow the x-ray generator to produce x-rays without the appropriate filter in place. The x-ray cone was keyed such that a particular filter, with a matching key, was required to be present in order for the operation to be permitted. It was not possible to "trick" the system into operation without filters. Table D.2 contains the filter mixtures used at each energy setting.

[†]A half-value layer is the amount of material required to attenuate a photon beam to half of its original intensity.

Accel. Potential (kV_p)	HVL (mm Cu)	Tube Current (mA)	Filter Mixture
300	2.83	10	0.3mm Sn + 0.5mm Cu + 1.5mm Al
200	0.9	15	0.35mm Cu + 0.5mm Al
175	0.47	16	0.1mm Cu + 2.5 mm Al
125	0.19	22.5	3.1 mm Al
75	0.066	29	2.5 mm Al

Table D.2: Accelerating potentials, corresponding HVLs, and tube currents for preset calibration settings used at the CCI x-ray facility. The filter mixtures are the filters that were required for operation of the x-ray generator at each energy setting.

Accelerating Voltage (kV_p)	CSR System Reading N (counts)	CCI System Reading N_C (counts)
300	162	88.50$\pm$0.05
200	161	88.60$\pm$0.05
172	162	89.50$\pm$0.05
125	163	90.20$\pm$0.05
75	159	87.90$\pm$0.05

Table D.3: Readings taken for CSR and CCI chambers and readout systems.

Three measurements were made with the entire CSR dosimetry system (ionization chamber and associated readout electronics) at each voltage setting. There was no fluctuation between the three readings at each setting. Each measurement was made for approximately 46 s, which corresponded to 100 monitor counts on the x-ray control readout. After the readings were made with the CSR dosimetry system, the CCI dosimetry system was used to take readings at the same voltages, for the same length of time. The CCI chamber was a PTW N30004-0010 farmer-type chamber and electro-meter, or calibrated current integrator, was a Capintec 48904779 unit. The readings taken with both systems are given in Table D.3.

Determination of Counts to Exposure Conversion Factor

To determine the factor to convert from counts from the CSR current integrator to exposure in R the exposure values for the CCI system were inferred from the electro-meter

Voltage (kV_p)	N_C (uncalib R)	I_S	N_X (R)	$S_C \pm \delta S_C$
300	88.50 $\pm$ 0.05	1.0336	1.1065 $\pm$ 0.0001	101.22$\pm$0.06
200	88.60 $\pm$ 0.05	1.0336	1.0853 $\pm$ 0.0001	99.39$\pm$0.06
175	89.50 $\pm$ 0.05	1.0336	1.0749 $\pm$ 0.0001	99.44$\pm$0.06
125	90.20 $\pm$ 0.05	1.0336	1.0686 $\pm$ 0.0001	99.63$\pm$0.06
75	87.90 $\pm$ 0.05	1.0336	1.0632 $\pm$ 0.0001	96.96$\pm$0.06

Table D.4: The correction and conversions used to obtain the exposure in R for the CCI ionization chamber. Electrometer readings and corresponding exposure values correspond to 46 seconds.

readings for the system. The exposure values for the CCI system electro-meter readings were given by

$$S_C = N_S \cdot N_X \cdot N_C, \tag{D.3}$$

where I_S, N_X, and N_C were the correction for chamber offset from calibration point, the factor to convert CCI electro-meter readings to exposure, and the average value of the electro-meter readings respectively. The conversion and correction values used in the above equation were obtained by the staff at the CCI from the NRC in Ottawa. All numerical values pertaining to the CCI system and used in this calibration are included in Table D.4.

The factor to convert the CSR dosimetry system from integrated current counts to exposure was then given by

$$C = \frac{S_c}{N} \cdot C_{PT}. \tag{D.4}$$

Table D.5 contains the values used in calculating the conversion factor C. The values for C are plotted against the accelerating voltage in Figure D.6.

Final Calibration Factor for 320 kV_p

The maximum operating voltage of the CSR x-ray generator is 320 kV_p. It was not possible to directly calibrate the CSR dosimetry system with the CCI dosimetry system as it was not possible to run the CCI x-ray generator at 320 kV_p. It was therefore necessary to extrapolate the value of the calibration factor at 320 kV_p from the data at lower voltages.

Accelerating Voltage (kV_p)	Tube Current (mA)	S_C (R)	N (counts)	$C \pm \delta C$ (R/count)
300	10	108.9±0.1	162	0.6722±0.0006
200	15	106.96±0.09	161	0.6644±0.0006
175	16	107.02±0.09	162	0.6606±0.0006
125	22.5	107.2±0.1	163	0.6578±0.0006
75	29	104.35±0.09	159	0.6563±0.0006

Table D.5: Values used to calculate the integrated current to exposure conversion factor for the CSR ion chamber system.

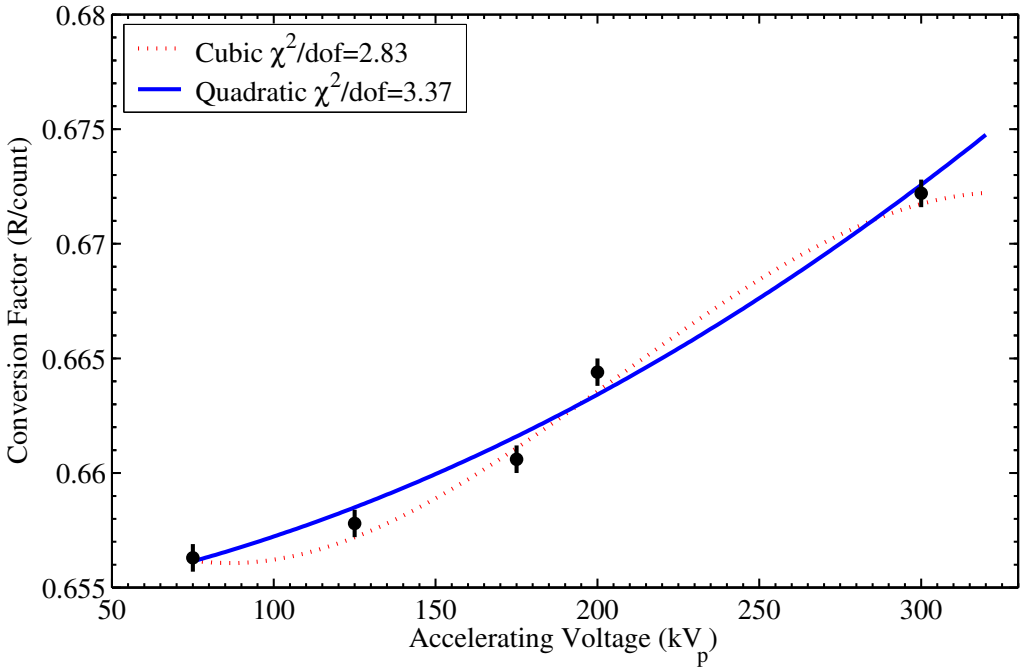

Figure D.6: The conversion factor for the CSR dosimetry system plotted against accelerating voltage. Quadratic and cubic fits were made to the data and are superimposed on the data.

Quadratic and cubic fits were made to the data (Figure D.6). The cubic fit had a smaller χ^2/degree of freedom, and was used for the extrapolated calibration factor. The value for the calibration constant at 320 kV_p was,

$$C(320) = (0.672 \pm 0.001)\ \mathrm{R/count}. \tag{D.5}$$

The error results from propagating the fit parameter uncertainties through equation D.4.

D.1.3 Conversion of Exposure to Dose in Air

The value for the constant to convert from exposure to the dose in air was taken from Ref[120] and had a value of 0.86.

D.1.4 Distance Correction

A correction was required to account for the decrease in radiation intensity with increasing distance from the x-ray tube. In order to make this correction, the plot in Figure D.7 was used. The plot was made with the setting of 320 kV_p and 10 mA. The curve on the plot is a fit made to the data and was given by

$$N = \frac{a}{(b+z)^2} \quad , \tag{D.6}$$

where N was the count rate in counts/min, z was the distance between the x-ray window and the ion chamber position. From the fit, a had a value of
(4.578 $\pm$ 0.004)$\times 10^7$ counts·mm^2/min, and b had a value of (118.50 $\pm$ 0.06) mm. The uncertainty in z dominated the overall uncertainty and had a value at the percent level. The value for the correction from the ion chamber to the top of the DUT was (1.08 $\pm$ 0.02), while the correction between the chamber and the bottom of the DUT had a value of (1.03 $\pm$ 0.02).

D.1.5 Material Correction

The last correction made to obtain a correct estimate of the dose absorbed by the DUT was for material. Once the dose in air had been determined, the dose in SiO_2 had to be calculated. The following relation equating the relative doses and their energy absorptions

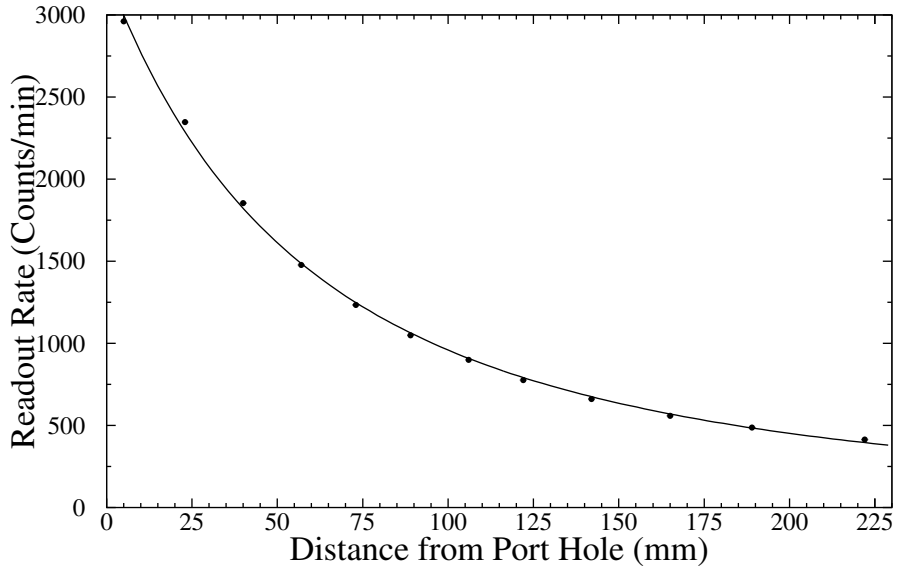

Figure D.7: Measurement of the counts coming from the ion chamber as a function of distance below the x-ray opening. This data is for the setting of 320 kV_p and 10 mA.

between the different materials was used:

$$\frac{\mathrm{D(SiO_2)}}{\mathrm{D(Air)}} = \frac{\mu_{SiO_2}}{\mu_{Air}}, \tag{D.7}$$

where the μs were the mass attenuation coefficients for two materials divided by their densities. The change in dose due to the material difference was thus given by μ_{SiO_2}/μ_{Air}. The correction factor was calculated using the National Institute of Standards and Technology database of mass attenuation coefficients. Figure D.8 shows the values of the correction as a function of photon energy. The corrections using both Si and SiO_2 are shown to illustrate that they were not interchangeable.

The correction was obtained by taking the ratio of the weighted attenuation coefficients for SiO_2 and air. The x-ray energy spectrum corresponding to the 320 kV_p setting would have to be used for the weighting function. If a form of the energy spectrum for the x-ray generator was known the correction would be calculated using

$$(C_{mat})_w = \frac{\int_0^\infty W(E)\mu_{SiO_2}(E)dE}{\int_0^\infty W(E)\mu_{Air}(E)dE}, \tag{D.8}$$

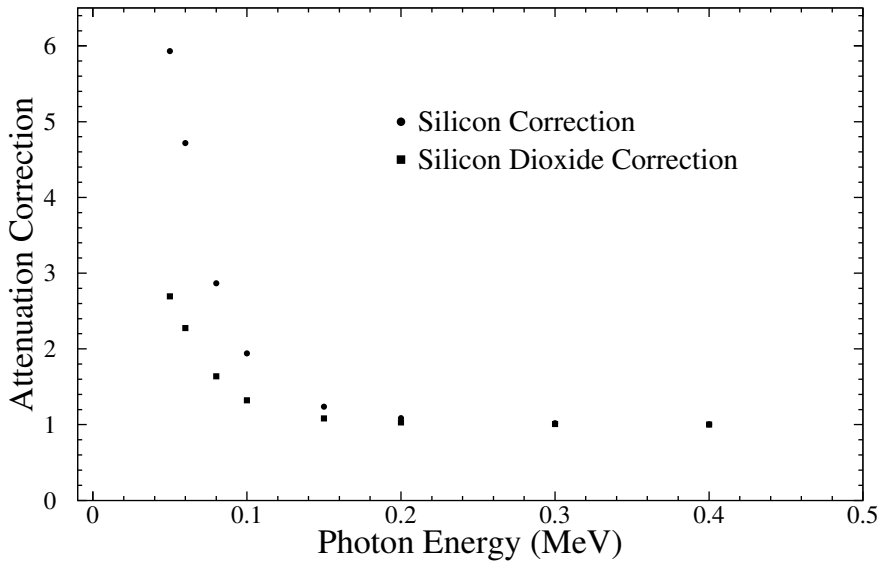

Figure D.8: Ratio of attenuation coefficients for silicon and silicon dioxide to air.

where $W(E)$ was the energy spectrum and the mass attenuation coefficients. Unfortunately the energy spectrum was not known and a method for estimating the spectrum was made by Dr. Douglas Gingrich, with assistance from Claudiu Cojocaru [99]. The method used attenuation measurements for well defined materials of well defined thickness to estimate the spectrum using a small number of discrete attenuation values. The photon spectrum was inferred by determining the spectrum that best characterized the set of attenuation values measured. Three different calculations were performed to obtain estimates of the photon energy spectrum from the measured attenuation values. A graphical method was used to obtain four discrete values that approximated the x-ray spectrum. Two other calculations were performed on the attenuation values that resulted in spectra with three discrete values. Table D.6 shows the three approximate spectra. Each of the three spectra was used in a weighted sum that replaced the integral in equation D.8 to obtain values of the material correction factor. The three values of the correction value were averaged to give a value that was used for the dosimetry calculation.

Combining the corrections gave values that could be used for dosimetry in any x-ray configuration.

Calculation Method	Energy (MeV)	Weighting
method 1	0.136 0.052 0.037 0.029	0.494 0.315 0.145 0.046
method 2	0.136 0.052 0.037	0.513 0.293 0.194
method 3	0.180 0.079 0.040	0.333 0.333 0.333

Table D.6: The weighting values for the three approximate spectra used in the dose calculation.

The last step in the dose rate calculation was to adjust for the uncertainty of the die position within the DUT, as well as the uncertainty in materials comprising the DUT. The dose at the die was taken as the weighted average of the top and bottom doses. The uncertainty was taken to be the larger difference between the weighted mean and the top or bottom dose. The conversion factors and their corresponding uncertainties, and hence the dose rates, depended on a number of parameters that could change from test to test. Code was written to automate the process of calculating the dose following each test.

Appendix E

Description of Monitoring Interface Used in XC2S150 and DMILL Tests

This appendix gives a brief description of the monitoring and DAQ systems used for the XC2S150 and DMILL test systems. More description of the software is given than the hardware as the author was only involved in the software. Monitoring hardware is described in sufficient detail to give a flavour of the overall system.

To ensure that the devices under test were examined in as close to realistic operating conditions as possible and that communication with the DUT could be performed quickly, an interface, or monitor, board was inserted between the test board and the data acquisition computer. The purpose of this monitor board was to behave in a similar fashion to the front-end board, described in Section 2.5.1. In addition, the monitor board received signals from the data acquisition computer and passed them on to the test device. Signals from the test device were sent to the data acquisition computer in the same fashion.

The primary requirements of the monitoring interface software was that it be able to configure the device under test (in the case of a programmable device) and the monitoring device with the circuits designed for them. It was also required to collect information sent from the monitoring device about the DUT and was responsible for loading registers in the SCAC. In addition, the monitor interface software logged data coming from the test device, via the monitor board. The system was designed to allow the testing of any controller prototype by simply substituting in the test board containing the device of interest. Each device under test required its own test board.

E.1 Monitor Interface for XC2S150E and DMILL Tests Systems

The hardware for this test system was designed by Dr. Douglas Gingrich and Li Chen and the hardware description is based on discussions and information provided by both of them. The monitor board, used for the DMILL and XC2S150 prototypes, (Figure E.1) contained a Xilinx Virtex 1000E FPGA, which was permanently attached to the board. The board also contained LEDs, switches, connectors and sockets for attaching programmable read only memories (PROMs). The FPGA on the monitor board contained roughly 1,000,000 gates and the circuit used for the test used approximately 5% of the device. There were two additional boards attached to the monitor board via long (4 cm) pins. A power board was connected below the monitor board. The power module was used to distribute power to the devices on the monitor board. A single voltage (6 V) was applied to the power module.

The purpose of the FPGA was to configure the SCA controller to run in its different operating modes, to monitor the output signals from the SCA controller, and to report errors to the computer. The architecture of the circuit in the FPGA consists of a kernel and a set of tasks. The kernel responses to commands from the computer and supervises the tasks. Each task communicates with the SCA controller and corresponds to one of the ASICs on the front-end board which is connected to the SCA controller. Figure E.2 shows the computer, kernel, tasks, SCA controller, and the communication between them.

E.1.1 Monitor Kernel

The monitor kernel communicates with the computer and supervises the four tasks. Commands are received from the computer over a serial port (`cpu_config_in`) and data is sent to the computer over a separate serial port (`cpu_config_out`). Strobe signals (`cpu_strobe`) from the computer cause the data to be transmitted over the two unidirectional serial ports. All state transitions are initiated by the computer polling the kernel.

The kernel can receive operation commands or monitor commands from the computer. An operation command is a request to set the SCA controller into a certain state. The kernel does not communicate with the SCA controller directly but makes operation requests to either the TTCrx task or the configuration controller task. These tasks can configure,

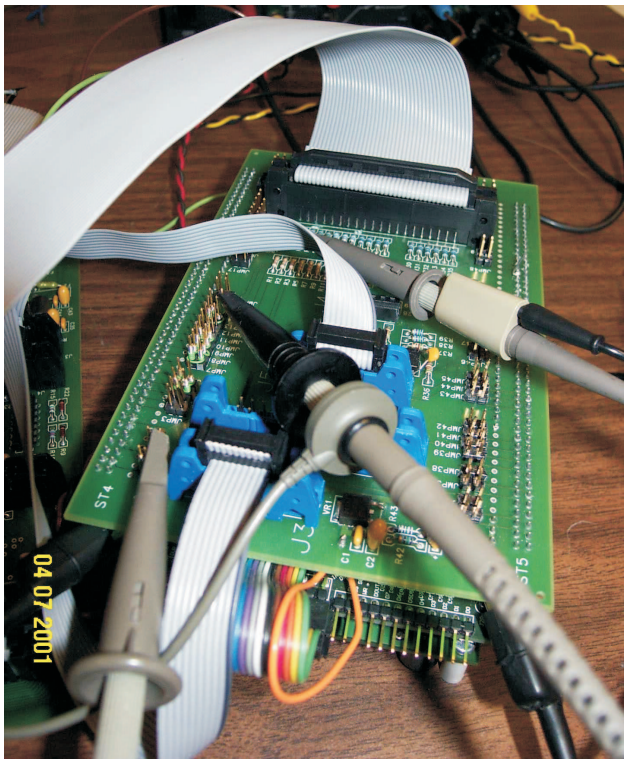

Figure E.1: Photograph of the monitor board used for the DMILL ASIC and XC2S150E tests. In the photograph probes are attached to the board for monitoring signals during one of the tests.

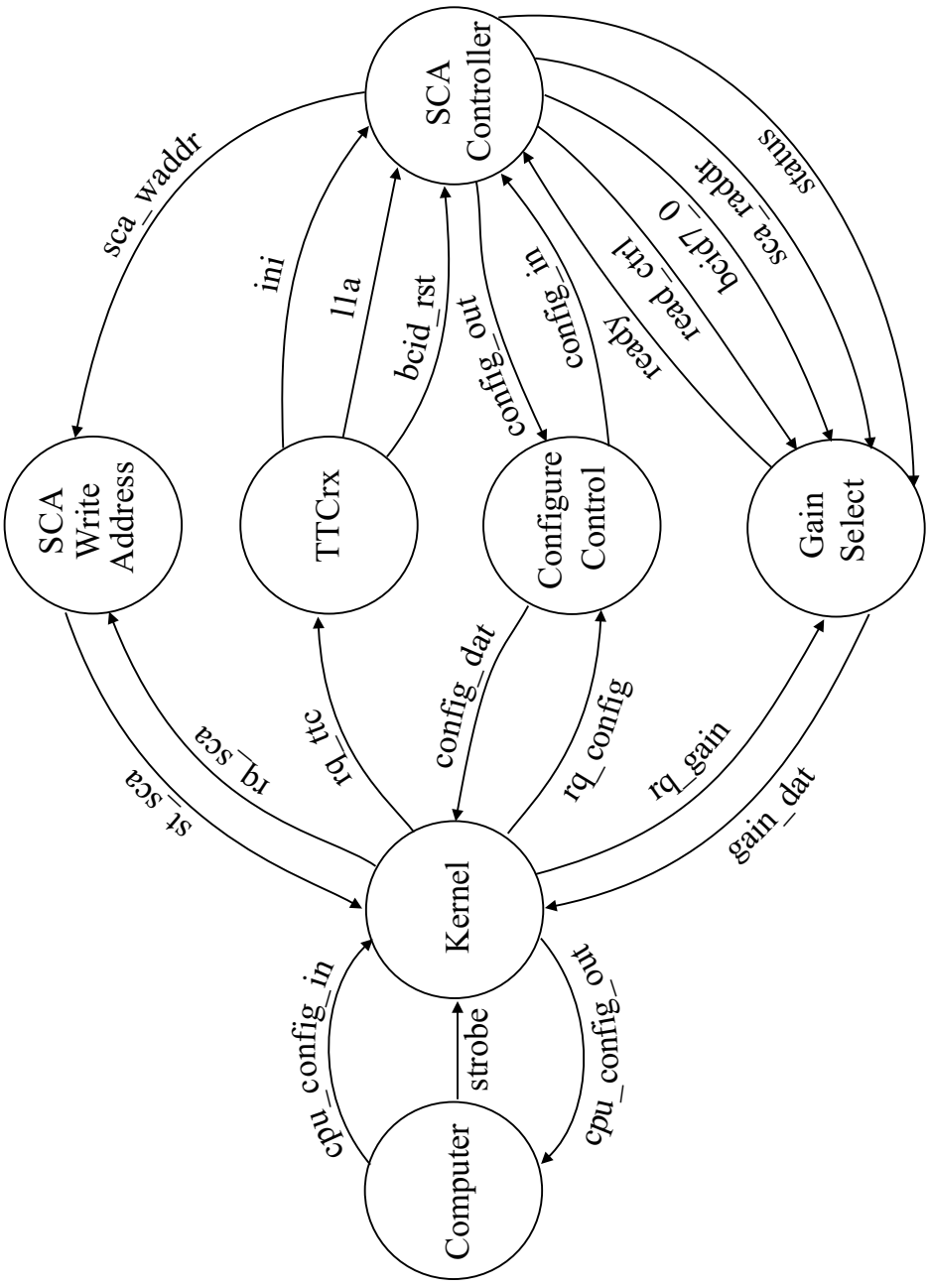

Figure E.2: Bubble diagram illustrating the flow of signals and data through the monitor device.

initialize, trigger, or reset the BCID counter of the SCA controller.

Monitor commands from the computer request information to be sent by the kernel to the computer for monitoring. When the kernel receives a monitor command it makes a request to either the SCA write address task, gain selector task, or configuration controller task for information which it then sends to the computer.

Ideally the kernel does not manipulate the data. Its function is to accept commands from the computer, supervise the tasks, and transmit monitor data from the tasks to the computer. All manipulation of the data from the SCA controller is performed by the monitor tasks which simulate the behaviour of the control devices on the FEB.

E.2 Software Interface

The monitoring software was designed to operate in two modes, interactive mode and batch mode. Interactive mode operation allowed the user to continuously enter instructions, which were then executed by the program. This mode of operation was used to debug problems with both the monitor software and the system. This code was modified into a full test-bench testing package*. Batch mode operation of the monitor program was used during radiation tests. In batch mode the user initially set a parameter that indicated the type of device to be tested. This was required as programmable devices had to be configured and ASICs did not. Once started the program required no additional input from the user. The following description of the monitor program pertains to the batch mode operation.

The operation of the monitor program is outlined in the flowchart in Figure E.3. The FPGA on the monitor board was initially configured and initialized by writing well defined values to its registers. Following these steps the program sent data for the DUT to the monitor device. If the test device was an ASIC the data values were to be loaded in registers on the DUT. If the test device was a re-programmable device, it required configuration before values were sent to its registers. After sending the data to the DUT the monitor device read the data back. If there was a discrepancy between the data sent and received by the monitor device a flag was set in an error register monitored by the DAQ

*These modifications were made by Li Chen of the University of Alberta.

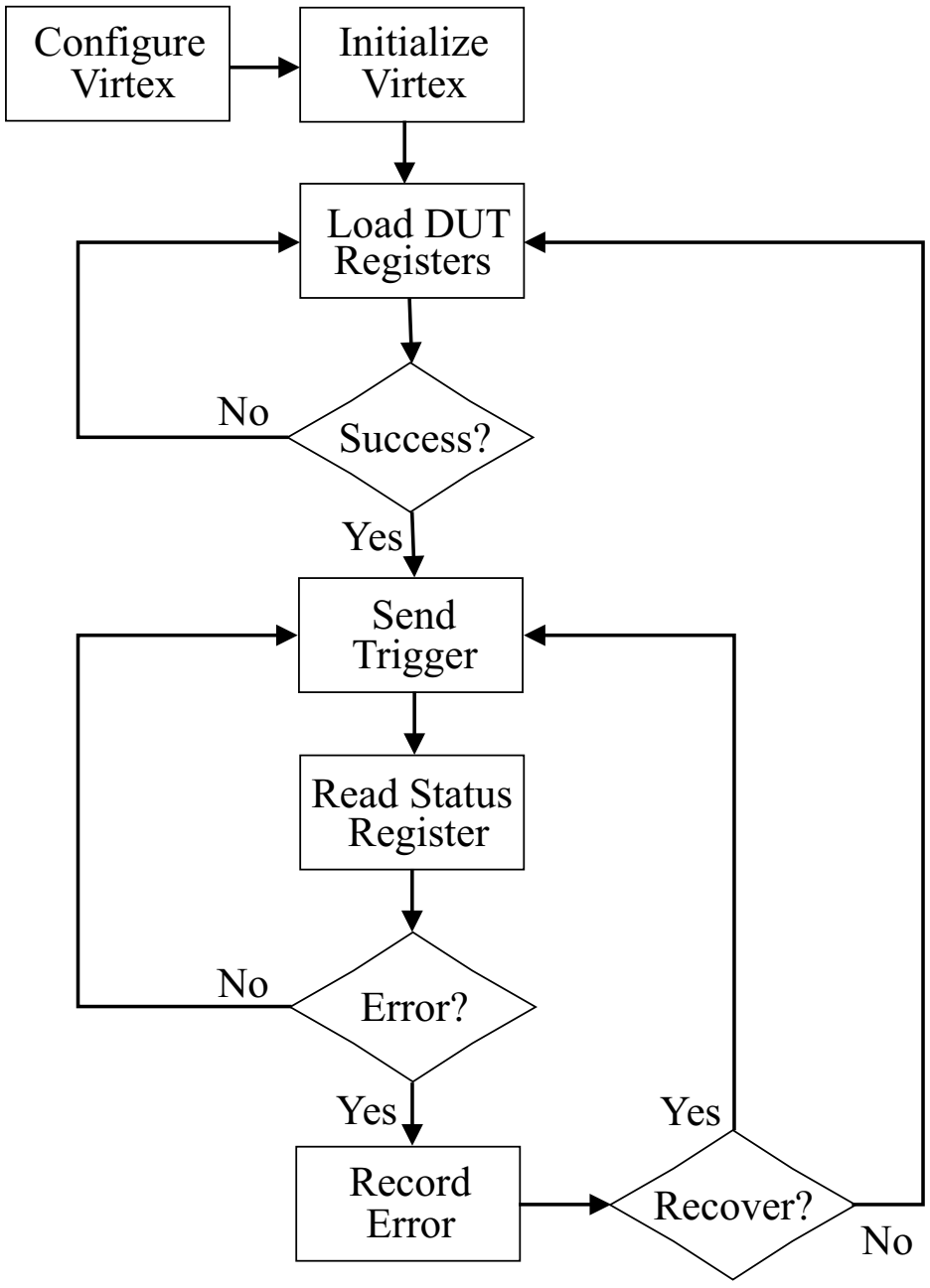

Figure E.3: Flow diagram illustrating program execution in batch mode. The cell referring to loading DUT register is specific to the case where an ASIC is being tested. In the case where a programmable device is under test this cell would also include the configuration of that device.

Error Bit	Associated Error
0	Addresses out of sequence
1	Error reading an address
2	Device not running properly
3	Free FIFO has gone empty
4	Overlapping samples have occurred
5	Done FIFO has gone full
6	Event FIFO has gone full
7	Controller has not yet been initialized

Table E.1: Test device errors associated with the 8 bits in the error register on the monitor device.

computer. The DAQ computer continued attempting to send the data to the DUT until the error register contained no set flags.

Once the DUT was operating, the monitor program continuously read an 8-bit status register on the monitor device. Each bit corresponded to a particular error occurring on the test device. Table E.1 lists the error associated with each bit of the error register. It is important to note that the test system was designed in such a manner that a trigger[†] needed to be sent by the monitor program in order that the error register on the monitor device could be read. As the trigger during tests was a software trigger, the trigger rate was entirely limited by the software and hardware of the DAQ computer. The maximum trigger rate attainable was measured at approximately 540 Hz.

Once an error was detected by the monitor program, the error was recorded and a reset command was sent to the DUT. The reset command returned the test device to an initial run state and restarted it. If it was not possible to reset the DUT, the registers and RAMs on the DUT were again reloaded and a reset was attempted. In the case of a programmable device, a reconfiguration would also be initiated upon failure to reset the DUT. We defined that the DUT was not resettable if after a predetermined number of reset attempts, usually three, the DUT would not reset.

[†]In the case of these tests, a trigger is a command sent by the monitor program to the monitor device. The monitor device then simulates the trigger command, which would be sent to the controller in ATLAS during operation.