University of Alberta

Library Release Form

Name of Author: Kaston Leung

Title of Thesis: Effects of Ionizing Radiation on I_{DDQ} Testing

Degree: Master of Science

Year this Degree Granted: 2005

Kaston Leung
Electrical and Computer Engineering
ECERF, 2nd Floor
University of Alberta
Edmonton, Alberta
T6G 2V4, Canada

Date: _____

The most exciting phrase to hear in science,
the one that heralds new discoveries,
is not "Eureka!" but "That's funny..."
-Isaac Asimov

University of Alberta

EFFECTS OF IONIZING RADIATION ON I_{DDQ} TESTING

by

Kaston Leung

A thesis submitted to the Faculty of Graduate Studies and Research in partial fulfillment of the requirements for the degree of **Master of Science**.

Department of Electrical and Computer Engineering

Edmonton, Alberta
Fall 2005

University of Alberta

Faculty of Graduate Studies and Research

The undersigned certify that they have read, and recommend to the Faculty of Graduate Studies and Research for acceptance, a thesis entitled **Effects of Ionizing Radiation on I_{DDQ} Testing** submitted by Kaston Leung in partial fulfillment of the requirements for the degree of **Master of Science**.

Dr. Ying Tsui
Supervisor

Dr. Douglas M. Gingrich
Co-Supervisor

Dr. Vincent Gaudet
Examiner

Dr. Roger Moore
External Examiner

Date: _____

Abstract

The increase in subthreshold leakage current, due to the decrease in minimum device feature sizes, causes a decrease in the difference between the mean levels of *quiescent power supply current* (I_{DDQ}) in defective and defect-free static *complementary metal oxide semiconductor* (CMOS) digital *integrated circuits* (ICs). This decrease poses a problem for the testing technique called *I_{DDQ} testing*, whose effectiveness is dependent on the magnitude of this difference.

This thesis investigates the effects of ionizing radiation on CMOS circuits and defects in CMOS circuits in order to determine if this difference, and hence the effectiveness of I_{DDQ} testing, can be increased with the application of ionizing radiation. Several CMOS test structures have been fabricated and irradiated with varying doses of ionizing radiation. Experimental data shows an increase of up to an order of magnitude in this difference for a type of defect known as a *gate oxide short*.

Acknowledgements

This work was partly supported by research grants from the Natural Sciences and Engineering Research Council of Canada, and equipment loans from the Canadian Microelectronics Corporation and the University of Alberta. I would like to thank my supervisors Dr. Xiaoling Sun and Dr. Doug Gingrich for their guidance, direction, and patience. I would like to thank Dr. Li Chen, Tyler Brandon, Dan Leder, and Dr. Igor Filanovsky for their assistance and suggestions during the design of the test chip. I would like to thank Mike Hume, Drew Price, John Schaapman, Lars Holm, Len Wampler, and Dr. Shengli Liu for their contributions to the design of test hardware and their assistance in the operation of the x-ray accelerator. I would like to thank Christian Giasson, John Koob, and Kris Breen for their assistance with the data analysis and for taking the time to discuss my ideas with me. Without the efforts of these people, the completion of this project would have been immensely more difficult. Finally, I must thank Michelle Zuliani for her understanding and encouragement.

Table of Contents

List of Figures

List of Tables

Nomenclature

List of Acronyms

CAD	computer aided design
CMC	Canadian Microelectronics Corporation
CMOS	complementary metal oxide semiconductor
CUT	circuit under test
EOS	electrical overstress
ESD	electrostatic discharge
IC	integrated circuit
MOSFET	metal oxide semiconductor field effect transistor
NMOS	n-channel metal oxide semiconductor
PCB	printed circuit board
PDN	pull-down network
PMOS	p-channel metal oxide semiconductor
PUN	pull-up network
RBB	reverse body bias
RILC	radiation induced leakage current
s-a-0	stuck-at 0 fault
s-a-1	stuck-at 1 fault
SOI	silicon-on-insulator
SSF	single stuck-at fault
TSMC	Taiwan Semiconductor Manufacturing Company

List of Symbols

η	process technology dependent parameter
λ	wavelength of an electromagnetic wave (m)
μ	carrier mobility ($cm^2\ V^{-1}\ s^{-1}$)
C_d	capacitance per unit area of the depletion region ($F\ \mu m^{-2}$)
C_{it}	capacitance associated with charges created by interface traps (F)
C_{ox}	capacitance per unit area of the gate oxide ($F\ \mu m^{-2}$)
E	energy of a photon (eV)
I_{DD}	power supply current (A)
I_{DDQ}	quiescent power supply current (A)
I_B	MOSFET substrate current (A)
I_D	MOSFET drain current (A)
I_F	current measured on the MOSFET terminal (source or drain) through which the most gate current is observed (A)
I_G	MOSFET gate current (A)
I_{NF}	current measured on the MOSFET terminal (source or drain) through which the least gate current is observed (A)
I_S	MOSFET source current (A)
I_{sub}	subthreshold leakage current of a MOSFET (A)
K	body effect coefficient ($V^{\frac{1}{2}}$)
L	MOSFET gate length (μm)
M_D	mean I_{DDQ} of defective ICs (A)
M_G	mean I_{DDQ} of defect-free ICs (A)
S	inverse of the slope of the logarithmic I_D versus V_G curve in the subthreshold region ($\frac{\Delta V_G}{\Delta I_D}$)
T	temperature (K)
V_B	MOSFET substrate voltage (V)
V_D	MOSFET drain voltage (V)
V_G	MOSFET gate voltage (V)
V_S	MOSFET source voltage (V)
V_{in}	input voltage of a logic gate (V)
V_{out}	output voltage of a logic gate (V)

V_t	thermal voltage (V)
V_{th}	threshold voltage of a NMOS or PMOS transistor (V)
V_{tn}	threshold voltage of a NMOS transistor (V)
V_{tp}	threshold voltage of a PMOS transistor (V)
W	MOSFET gate width (μm)

Chapter 1

Introduction

Testing is an important step in the manufacturing of *integrated circuits* (ICs). Its purpose is to detect defects in ICs, which may either cause the IC to function incorrectly or adversely affect its performance. Currently, the most widely used implementation of digital ICs is known as *static complementary metal oxide semiconductor* (CMOS). The primary advantage of using static CMOS digital logic circuits is their low power consumption. A significant amount of power is only consumed during switching on the circuit inputs. When the circuit is in steady state, comparatively little power is theoretically consumed. This property has given rise to a testing technique known as I_{DDQ} *testing*. This technique detects physical defects in ICs by observing the increased *quiescent power supply current* (I_{DDQ}) caused by their presence. This is a powerful testing technique because it requires relatively little effort to detect many kinds of defects.

However, as IC manufacturing technology advances and minimum feature sizes are scaled down to the deep-submicron region, the intrinsic leakage current of the MOSFET devices used in CMOS circuits increases. This causes the level of the I_{DDQ} of defect-free circuits to approach that of defective circuits, making it more difficult to distinguish between the two using I_{DDQ} testing. This problem threatens to render this powerful testing technique obsolete as minimum feature sizes continue to scale down.

This thesis investigates the possibility of applying ionizing radiation to increase the difference between the I_{DDQ} of defect-free and defective static CMOS circuits. It is known that exposure to ionizing radiation can increase MOSFET currents. However, research has not yet been done to determine the effect of ionizing radiation on the behaviour of physical defects commonly found in CMOS circuits. It is possible that exposure to ionizing radiation increases the current caused by IC defects more than it increases the current in defect-free ICs. If this is the case, ionizing radiation can be used to improve the defect-detecting capabilities of I_{DDQ} testing, and thus help to alleviate the aforementioned problem caused by scaling. The goal of this work is therefore to discover the effects of ionizing radiation on the behaviour of common IC defects, and to determine if these effects are beneficial to

I_{DDQ} testing.

To this end, an experiment has been constructed to facilitate the observation of these effects. Test chips containing multiple CMOS test structures have been fabricated and exposed to various doses of ionizing radiation. The changes in electrical characteristics due to this exposure have been analyzed. Evidence suggesting that ionizing radiation could aid in the detection of a certain type of defect will be shown.

1.1 Thesis Organization

In Chapter 2, an overview of I_{DDQ} testing is given. I_{DDQ} testing is compared with more traditional voltage testing techniques, and the unique benefits of I_{DDQ} testing are presented in order to demonstrate its value to the IC industry. The characteristics of the defects in CMOS circuits commonly detected by I_{DDQ} testing are described. The problems which confront I_{DDQ} testing due to technology scaling are explained and some suggested solutions are presented in order to place the work of this thesis in context with other research.

In Chapter 3, a qualitative overview of the effects of ionizing radiation on CMOS devices is given. The changes in the electrical characteristics of MOSFETs, due to ionizing radiation, are described and the mechanisms which cause these changes are explained.

In Chapter 4, the details of the experiment central to the work of this thesis are given. The design of the test chip is explained and design decisions are justified. A description of the equipment used and the experimental procedure followed is given.

In Chapter 5, the data obtained from the experiment is analyzed. The method of analysis is first explained. The changes in electrical characteristics of the test structures due to ionizing radiation are then analyzed in order to determine any effects beneficial for I_{DDQ} testing.

In Chapter 6, a summary of the thesis is given and conclusions are drawn. As well, the limitations of the experiment are discussed and future work that could strengthen the findings of this work is suggested.

Chapter 2

I_{DDQ} Testing

In this chapter, an overview of I_{DDQ} testing is given. Static CMOS digital logic circuitry is first reviewed, and the process by which I_{DDQ} testing detects defects in these circuits is then explained. I_{DDQ} testing is then compared to traditional voltage testing techniques and the unique properties and benefits of I_{DDQ} testing are presented in order to demonstrate its value to the integrated circuit industry. The characteristics of the defects that are commonly detected by I_{DDQ} testing are then given, and their effects on static CMOS circuits are explained. Finally, the problems associated with applying I_{DDQ} testing to deep-submicron technology are explored and a survey of some suggested solutions is presented.

2.1 Static CMOS Digital Logic

The most widely used style for designing digital logic *integrated circuits* (ICs) is known as *static CMOS* [1]. A static CMOS digital logic gate consists of two networks: a *pull-up network* (PUN) and a *pull-down network* (PDN). Figure 2.1 shows the general structure of such a digital logic gate. The PUN is composed of PMOS transistors and provides a low resistance path between the output of the logic gate and V_{DD} when the output is meant to be a logic 1. Conversely, the PDN is composed of NMOS transistors and provides a low resistance path between the output and V_{SS} when the output is meant to be a logic 0. These two networks are *complementary*, meaning that they are designed in such a way that any possible combination of inputs to the logic gate will result in either a low resistance path through which current can either flow from V_{DD} to the output or from the output to V_{SS}, but never both simultaneously. Current flowing from V_{DD} to V_{SS} is referred to as I_{DD}.

Whenever the inputs to the logic gate are in a steady state, no path exists from V_{DD} to V_{SS} and I_{DD} is only equal to the leakage currrent of transistors that are not switched on. This relatively low I_{DD} results in little power consumption while inputs are stable. This is known as low *static power* consumption. A significant amount of power is only consumed by the circuit when switching occurs on one or

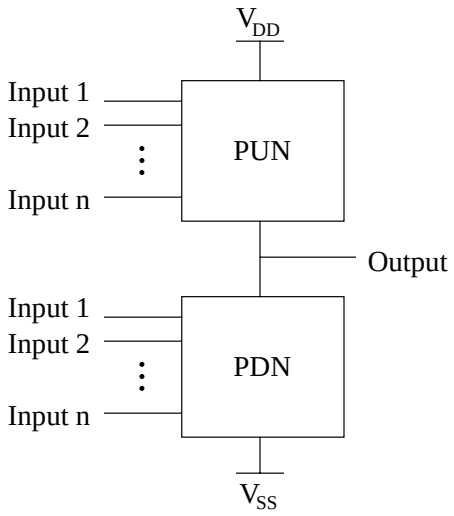


Figure 2.1: Static CMOS digital logic gate.

more of the inputs. For a short time during switching, the voltage on these inputs reaches a value less than or equal to V_{DD} - V_{tp} (where V_{tp} is the threshold voltage for a PMOS transistor) but greater than or equal to V_{SS} + V_{tn} (where V_{tn} is the threshold voltage for an NMOS transistor). This causes some PMOS transistors in the PUN and some NMOS transistors in the PDN to simultaneously conduct, which can result in a low resistance path from V_{DD} directly to V_{SS} through which current can flow. This results in a high value of I_{DD}, which in turn causes high power consumption. This relatively high level of power consumption that occurs during switching on the inputs is known as high *dynamic power* consumption. However, since inputs are stable during most of the operation of logic gates, static CMOS gates are considered to have low overall power consumption. This is a key advantage of implementing digital logic using a static CMOS design style.

2.2 I_{DDQ} testing

A *defect* is defined as any physical difference between a circuit and its intended design. Since low static power consumption is a characteristic inherent in static CMOS digital logic circuits, abnormally high static power consumption can indicate the presence of a defect. This concept is exploited in the testing technique known as *I_{DDQ} testing*.

2.2.1 How I_{DDQ} Testing Works

Quiescent power supply current (I_{DDQ}) is the I_{DD} of a static CMOS circuit measured when all inputs are in a steady state. Many defects can cause a significant elevation in I_{DDQ} over that of a non-defective circuit. Figure 2.2 illustrates the basic concept

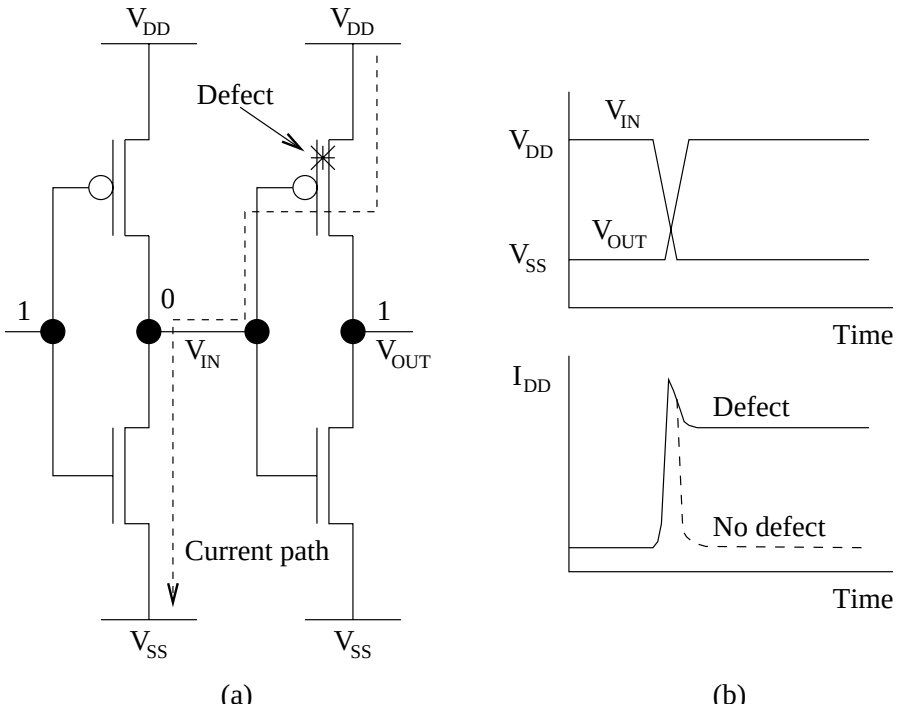


Figure 2.2: An example of a defect causing high I_{DDQ}. The current path caused by a defect is shown in the schematic in (a). The I_{DD} of the defective circuit before, during, and after switching on the input is shown in (b).

involved in I_{DDQ} testing. Figure 2.2(a) shows two static CMOS inverters linked in a chain. The PMOS transistor of the second inverter contains a defect which causes a resistive connection to be formed between its source and gate terminals. Figure 2.2(b) shows I_{DD} in relation to the input and output voltages of the defective inverter. When V_{in} is equal to V_{DD}, the defect does not cause an increase in I_{DD} since the source to gate voltage (V_{SG}) of the PMOS transistor is zero. When V_{in} transitions from V_{DD} to V_{SS}, I_{DD} increases as explained in section 2.1. However, when V_{in} settles to a stable value, a voltage drop equal to V_{DD} occurs across the defect, allowing current to flow from V_{DD} to V_{SS} through the path indicated by the dashed line. This leads to the elevated I_{DDQ} indicated by the solid line in the graph. The dashed line indicates the negligible I_{DDQ} that would be present in a non-defective circuit. The presence of the defect is therefore revealed by the elevated I_{DDQ}.

In this example, to detect the defect, it is necessary to drive V_{in} to a logic 0 in order to create a voltage drop across the defect. It can be said that a requirement for detecting resistive defects using I_{DDQ} testing is that the two circuit nodes across the defect must be at opposite logic values [2]. This ensures that current flows from V_{DD} to V_{SS} through the low resistance path provided by the defect causing an increase in the I_{DDQ} of the circuit. This process is known as *sensitizing* the defect.

2.2.2 Importance of I_{DDQ} Testing

Many semiconductor manufacturers presently consider I_{DDQ} testing as an essential part of their overall IC testing strategy. This section describes the effectiveness of I_{DDQ} testing relative to conventional and more established test techniques and discusses some reasons why it has garnered significant interest and support from the IC testing community.

2.2.2.1 Overview of Structural Voltage Testing

The current measurement based testing technique now known as I_{DDQ} testing was first formally proposed in 1981 [3]. Until then, the only standardized testing techniques for digital logic ICs fell into the realm of *voltage testing*. As the name suggests, voltage testing involves the observation of circuit input and output voltages in order to determine whether or not a circuit is operating properly. The *Circuit Under Test* (CUT) is stimulated with a set of input voltages, known as *test vectors*, and the output voltages are then compared to those that a properly functioning CUT is expected to generate.

Voltage testing can be classified into two main categories: *Functional testing* and *structural testing* [4]. Functional testing tests the CUT by comparing the test vectors and resulting outputs with some or all of the entries in the truth table of the CUT. That is, the CUT is tested according to its logical function. Structural testing tests the CUT according to the circuit architecture defined by its gate-level schematic. This involves the use of test vectors which are designed to detect behavioural models of defects known as *fault models*. Fault models are representations of the behaviour of defects at a desired level of abstraction. In structural voltage testing, defects are abstracted as erroneous digital behaviour in the gate-level schematic of a CUT. While functional test vectors must vary from CUT to CUT because they are based upon circuit functionality, structural test vectors can be generated using algorithms which can be applied to all CUTs. This is possible because the fault models, which the structural test vectors are designed to target, are applicable to all CUTs. These algorithms allow for the generation of a much smaller number of structural test vectors, capable of detecting a large portion of structural faults, compared to the large number of test vectors required to perform a complete functional test. For these reasons, structural testing has received much more attention in the literature than functional testing. As well, structural testing has become a standard test method supported by a variety of *Automatic Test Pattern Generation* (ATPG) tools, which use various algorithms to generate structural test vector sets.

Numerous fault models exist in the world of IC testing, but the most popular and established one used in industrial structural testing is the *single stuck-at fault* (SSF). SSFs are assumed to affect only the interconnections between logic gates. The SSF is based on the assumption that all defects in a given CUT result in a

node being fixed or "stuck at" either logic 0 or 1. There are therefore two kinds of SSFs: *stuck-at 1* (s-a-1) and *stuck-at 0* (s-a-0). To illustrate how SSFs are used, consider the case where a test engineer is trying to detect a s-a-1 fault on a given circuit node. It is first necessary to attempt to drive the node to a logic 0 value by manipulating the available inputs to the CUT, known as the *primary inputs*. The ease with which any given node in a CUT can be driven to a desired logic value is known as *controllability*. Secondly, it is necessary to propagate the value of the node in question to the available outputs of the CUT, known as the *primary outputs*. The ease with which the logic value at any given node in a CUT can be propagated to a primary output is known as *observability*. Structural test vectors are derived in order to accomplish both of these tasks. If, after the test vector has been applied, the propagated value of the node in question does not match that which is expected from a fault-free circuit, it is concluded that a s-a-1 fault has been detected on the node in question. Test vectors are generated in order to detect s-a-0 and s-a-1 faults on as many nodes in the CUT as possible. The *SSF coverage* of a set of test vectors for a given CUT states the percentage of all possible SSFs in the CUT that are detectable. It has become the standard metric used by suppliers and customers to describe the quality of all structural test methods.

2.2.2.2 I_{DDQ} Testing vs. Structural Voltage Testing

A primary reason for the widespread dominance of the SSF in digital IC testing is the ease it allows in the development of test vectors. With the use of SSFs, test vector generation requires only a gate-level description of the CUT since it is assumed that defects result only in incorrect digital behaviour. This is much easier than dealing with the largely analog characteristics of real physical defects. However, voltage testing using SSFs has been criticized for targeting faults that are behavioural abstractions of physical defects, instead of targeting the root cause of circuit failures, which are the defects themselves. The goal of IC testing, after all, is not to detect faults, but to detect defects. Various publications have shown that the SSF does not accurately model physical defects. Using a system called *inductive fault analysis*, which extracts circuit-level behaviour from physical defects, it was shown that SSFs do not accurately model an alarmingly large percentage of physical defects [5], [6]. Empirical evidence obtained using experimental test chips has also supported this claim [7], [8], [9].

Unlike structural voltage testing, I_{DDQ} testing is a *defect-oriented* test method, meaning that it targets physical defects and not fault models. Because of this, it is able to detect defects that the SSF-based structural test can not. Efforts have been made in order to investigate the value of I_{DDQ} testing relative to other testing methods. To this end, industrial semiconductor manufacturers have applied a variety of testing methods to ASICs made using commercial processes and analyzed their abilities to detect the presence of defects. To date, the largest of the experi-

ments of this nature is the SEMATECH study [10], [11]. In this study, a sample of 20,000 IBM graphics controller devices fabricated using a 0.45 μm, three metal layer process was subjected to four different test methods. It was found that out of the 20,000 devices tested, 1,463 failed the I_{DDQ} test but passed the three other tests, one of which was a structural voltage test with 99.7% SSF coverage [12]. Consequently, one of the important conclusions drawn from the results of the SEMATECH experiment was that I_{DDQ} testing is a test technique capable of detecting defects that are undetectable using other test techniques, and is therefore indispensible. Defects that are uniquely detected by I_{DDQ} testing are referred to as *I_{DDQ}-only defects*. Because increased I_{DD} can significantly lower battery lifetimes, defects that cause high I_{DDQ} are a particularly serious concern for systems with power consumption constraints, such as battery-operated systems, and for systems with high reliability requirements, as is the case in medical or space applications.

The conclusion drawn from the SEMATECH experiment has also been drawn from the results of other similar experiments. In [13] it was shown that even taking I_{DDQ} measurements after applying test vectors developed for voltage testing, and not I_{DDQ} testing, resulted in the detection of defects that are undetectable by voltage testing with 100% SSF coverage. In [14] it was shown that the introduction of I_{DDQ} testing into an industrial production test strategy lowered product failure rates to a level below what was attainable using only voltage testing with high SSF coverage. The detrimental effect of I_{DDQ}-only defects on circuit functionality has also been investigated. In [15], through analysis of the SEMATECH experiment data, it was concluded that information-carrying signals in the CUT are affected by 90% of I_{DDQ}-only defects. In addition, it was shown that at least 19% of these defects could dangerously degrade logic signals. Clearly, it can be said that I_{DDQ}-only defects pose a threat to circuit functionality and that it is well worthwhile to detect these defects.

While the detection of I_{DDQ}-only defects is an obvious advantage of applying I_{DDQ} testing, another advantage is the inherent observability which it provides. Since the presence of a defect is indicated by increased I_{DDQ}, it is only necessary to have access to the V_{DD} and V_{SS} power rails in order to observe the presence of a defect once it has been sensitized. As in structural voltage testing, test vectors are used to sensitize defects, but unlike structural voltage testing, it is not necessary to expend effort to propagate any logic values in order to make them observable. It can be said that I_{DDQ} testing has much higher observability than structural voltage testing, and therefore requires much less effort in the test generation process. This makes I_{DDQ} testing an especially powerful tool for detecting defects that affect deeply embedded nodes which are not easily accessible via primary inputs and outputs, and thus require a great deal of effort to control and observe using structural voltage testing.

Since SSF coverage remains an important test metric for the CMOS IC industry, it has also been shown that I_{DDQ} testing can be used to detect SSFs. In [16], it was

shown that significant benefits could be obtained when conventional algorithms, used to generate test vectors designed to detect SSFs, were modified to generate test vectors suitable for I_{DDQ} testing. Specifically, SSF coverage was improved, test vector set sizes were reduced, and less computational effort (measured in terms of CPU cost) was expended for test vector generation. A primary reason for these improvements is that there was no need to take observability into account during the test vector generation process. In addition to this, it was found that faults such as *logically redundant faults* and *multiple stuck-at faults*, which were considered previously intractable, were detectable with the introduction of I_{DDQ} testing. Logically redundant faults are SSFs which can not be propagated to a primary output, and are therefore undetectable using conventional structural voltage testing. However, since I_{DDQ} testing does not require any fault propagation, these faults are made detectable. Multiple stuck-at faults are faults which include the possibility of having more than one SSF present in a given CUT. Detection of these faults are virtually intractable using conventional structural voltage testing because it is possible for one SSF to mask the presence of another SSF present in the same CUT. I_{DDQ} testing is able to detect multiple stuck-at faults because there is no way that one SSF can mask the increased I_{DDQ} caused by another SSF.

In general, augmenting the fault coverage of a voltage test for a given CUT requires an incrementally increasing amount of effort as fault coverage approaches 100%. As fault coverage approaches 100%, an increasingly large number of test vectors must be added to the vector set in order to obtain any further benefit. However, adding a small set of I_{DDQ} test vectors can dramatically increase fault coverage with much less additional effort than is required by adding conventional voltage test vectors. In [17], it was shown that a SSF coverage of more than 95% could be achieved by adding an I_{DDQ} test vector set of approximately 20 vectors to a voltage test vector set with a SSF coverage of 80-85%. Achieving such an increase in SSF coverage by using only a conventional voltage test approach would require a much larger additional number of voltage test vectors. Clearly then, I_{DDQ} testing is valuable not only because of its ability to detect I_{DDQ}-only defects, but also because it is able to increase the effectiveness of test methods aimed at detecting SSFs.

For all of the aforementioned reasons, the value of I_{DDQ} testing has been acknowledged by both industry and academia. By the mid 1990s, many companies had developed and commercialized CAD tools designed to generate I_{DDQ} test vectors and to facilitate the modification of digital IC designs to make them more suitable for I_{DDQ} testing [18]. In the late 1980s, numerous publications in conferences and journals, addressing various issues surrounding I_{DDQ} testing, began to emerge. In response to this, the IEEE Technical Committee on Test Technology approved a new workshop on I_{DDQ} testing that was held in conjunction with the International Test Conference in 1995. The value of using not only voltage testing, but a variety of testing techniques, including I_{DDQ} testing, has been asserted in several publications [12], [16], [19], [20]. I_{DDQ} testing is now generally accepted as an

indispensible tool which is necessary as part of a suite of testing techniques needed to ensure low defect levels in static CMOS digital ICs.

2.3 Defects Detected by I_{DDQ} Testing

Since I_{DDQ} testing is a defect-oriented technique, an overview of the kinds of defects that are typically detected by I_{DDQ} testing is presented here. IC defects are caused by either unintended alterations to the manufacturing process, such as particulate contaminants, or activity which stresses the circuit after fabrication. Both of these can result in unintended and undesirable regions of extra conduction or insulation. Since their causes can vary so widely, the characteristics of defects can also differ greatly from device to device. However, it has been shown that most defects can be broadly classified as either short or open circuits [21]. Short circuit defects are any unintended connections between two or more circuit nodes. They can not be assumed to have a resistance of zero and they may have linear or non-linear I-V characteristics. Open circuit defects refer to electrical discontinuities in the circuit and typically have very high resistance. Open circuit defects which cause a significant decrease in I_{DDQ} are not detected by I_{DDQ} testing. However, these defects typically result in incorrect logical behaviour and are therefore detected by voltage testing.

All of the defects described below cause elevated I_{DD} in some way. As previously mentioned, this symptom leads to increased power consumption, which is particularly undesirable in battery-powered systems, or any such systems where low power consumption is a priority. As explained below, these defects can also cause other undesirable effects that may not be detected by SSF-based voltage testing. This emphasizes the need to detect such defects using other less conventional testing techniques such as I_{DDQ} testing.

2.3.1 Bridging Defects

A *bridging defect* is any undesired resistive connection between two or more nodes of a circuit. This can result from either additional conducting material or missing insulating material. These defects are typically caused by either particulate contaminants in the fabrication process or errors in the fabrication process such as misalignment of masks in the lithography stage. Bridging may occur between two nodes on the same metal or polysilicon layer of an IC, or between nodes on two different layers. As manufacturing technology advances and metal and polysilicon pitches decrease, bridging defects caused by particulate contaminants become more of a concern. For example, a particle with a diameter of 0.5 μm has a relatively low chance of causing a bridging defect in a process with 2 μm metal pitch, but the same particle has a much higher chance of causing bridging in a process with only 0.25 μm metal pitch.

The behaviour of bridging defects has been analyzed and reported in the literature and in general it has been found that the effect of the defect is dependent on the resistance of the bridging defect relative to the resistances of the MOSFETs in the affected logic gates [22], [23], [24]. The effect of bridging defects can be explained with the aid of the diagrams shown in Figure 2.3. Of course, bridging defects can theoretically occur between any two nodes of a circuit, but it is impractical to analyze all such defects. One such case is presented here in order to illustrate the general effect of bridging defects and their resistance. Figure 2.3(a) shows two CMOS digital logic gates whose outputs are connected through a bridging defect with resistance R_D. If the inputs to the two gates are such that PUN_1 and PDN_2 are off and PUN_2 and PDN_1 are on, then the two gates can be modeled as the circuit in Figure 2.3(b) where R_{P1} and R_{P2} are the pullup resistances of PUN_1 and PUN_2 and R_{N1} and R_{N2} are the pulldown resistances of PDN_1 and PDN_2 respectively. The voltages at V_1 and V_2 can therefore be expressed with Equations 2.1 and 2.2 using voltage division:

$$V_1 = V_{DD}\left(\frac{R_{N1}}{R_{N1}+R_D+R_{P2}}\right), \tag{2.1}$$

$$V_2 = V_{DD}\left(\frac{R_{N1}+R_D}{R_{N1}+R_D+R_{P2}}\right). \tag{2.2}$$

As $R_D \to \infty$, $V_1 \to V_{SS}$ and $V_2 \to V_{DD}$ as is expected in a properly functioning circuit. However, as $R_D \to 0$, $V_1 \to \frac{V_{DD}}{2}$ and $V_2 \to \frac{V_{DD}}{2}$ (assuming $R_{P1} = R_{P2} = R_{N1} = R_{N2}$). This means that V_1 and V_2 can have indeterminate logic values depending on a the resistance of the defect. Bridging defects can also cause an increase in propagation delay. For example, a node being charged from V_{SS} to V_{DD}

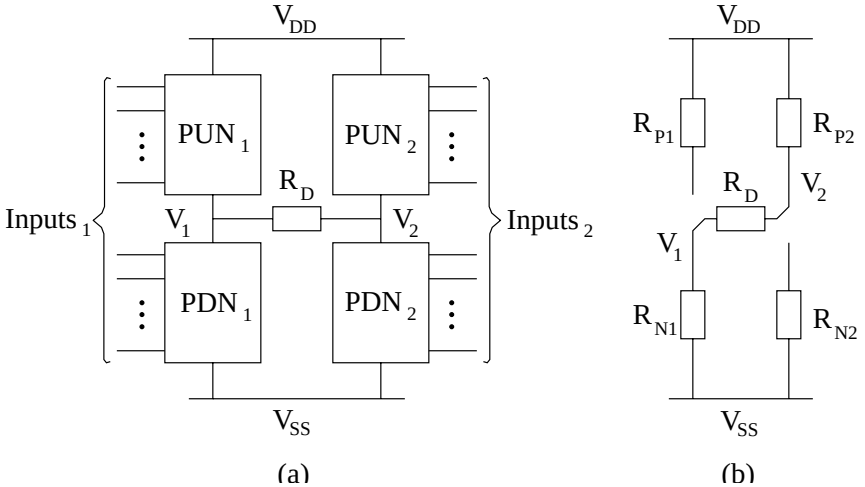


Figure 2.3: Modeling of bridging defects. The CMOS circuit in (a) can be modeled by the resistive network in (b) when PDN_1 and PUN_2 are on.

may be slowed if that node is bridged to a node with a voltage of V_{SS} through a defect. Degraded logic voltage levels can be caused in a similar manner if a node is not permitted to be fully charged to V_{DD} or fully discharged to V_{SS} because of a bridge to another node at a voltage of V_{SS} or V_{DD} respectively. Degraded logic voltage levels result in lower noise margins, which make the affected circuit more susceptable to malfunction in the presence of environmental noise. So, while bridging defects may not result in erroneous node voltages, they can pose a serious threat to circuit reliability.

Because circuit node voltages may not be erroneous, these defects may not be detected using voltage testing. However, they always result in a path of lowered resistance from V_{DD} to V_{SS}. In Figure 2.3(b), the defect provides a path for increased I_{DDQ} through R_{P2}, R_D, and R_{N1}, which is therefore detectable using an I_{DDQ} test. In [24], it was shown that monitoring I_{DDQ} during voltage testing provided greatly increased defect coverage over SSF testing alone. As well, it was shown that I_{DDQ} test generation was quicker and provided more complete defect coverage than an SSF test.

Inductive fault analysis has suggested that the greatest number of defects results in bridging behaviour [5]. In [25], a structure was constructed for the measurement of the resistance of bridging defects in metal layers, and was fabricated on a number of wafers from different production lines and different batches. It was found that the majority of the bridging defects had a relatively low resistance of less than 500 Ω. Since the effect of a bridging defect on a given circuit is higher when its resistance is lower, this is not welcome news for IC manufacturers.

2.3.2 Gate Oxide Shorts

A *gate oxide short* is an electrical connection through the thin layer of oxide separating the gate polysilicon from the silicon surface of a MOSFET. A gate oxide short can be thought of as a specific kind of bridging defect. However, because of its particular causes and characteristics, it is presented separately here. As shown in Figure 2.4(a) and (b) respectively, these shorts can occur between the gate and source or drain regions, or between the gate and substrate. In both cases, gate oxide shorts create an undesired current path through the gate oxide, thus violating the requirement that the gate be electrically isolated from the other terminals of the transistor for proper operation.

Gate oxide shorts are a result of a variety of physical mechanisms. They can either be created at the time of fabrication by errors in the manufacturing process, or they can occur later when imperfections in the structure of the transistor break down due to electrical field or thermal stress. The latter is known as *time-dependent dielectric breakdown*. With modern IC manufacturing technology using gate oxides with thicknesses of 50 $\AA$ or less, the smallest variation in thickness greatly increases the possibility of defects [18]. In addition, as technology advances, allowing device

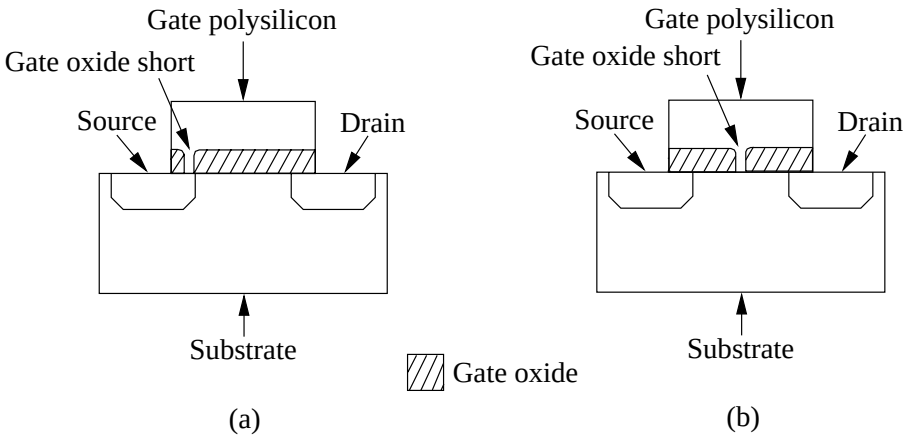


Figure 2.4: Gate oxide shorts in a MOSFET.

sizes to shrink and reducing gate oxide thicknesses accordingly, gate oxide shorts will become increasingly prevalent.

Gate oxide shorts that occur between the gate and source/drain are typically caused by *electrostatic discharge* (ESD) or *electrical overstress* (EOS) [26]. This is due to the fact that ESD/EOS usually causes defects at locations in the gate oxide where higher electrical fields occur due to structural irregularities. In a MOSFET, these are found at the edges of the gate where the field oxide, which insulates a transistor from other nearby conducting materials, interfaces with the gate polysilicon. Since these edges are located above the source and drain regions, most gate oxide shorts caused by ESD/EOS are gate-to-source/drain shorts. A detailed description of how ESD/EOS causes these defects can be found in [27].

Gate oxide shorts that occur between the gate and substrate are usually caused by time-dependent dielectric breakdown [26]. These shorts are primarily a result of structural imperfections in the gate oxide or in the silicon substrate beneath the gate oxide, which occur in the manufacturing process. Since these defects appear randomly along the length of the gate, they are more likely to be found in the longer area above the substrate than in the comparatively shorter areas above the source/drain regions. Metal ions, particulate contaminants, and crystalline defects are known to reduce the dielectric strength of gate oxide, while silicon substrate defects are typically induced by oxidation. A detailed description of how time-dependent dielectric breakdown occurs can be found in [28].

Experiments have been conducted to assess the electrical characteristics that gate oxide shorts impose upon individual MOSFETs, and how they alter the behaviour of logic gates. In [29], gate-to-source/drain and gate-to-substrate oxide shorts were induced in 3 μm technology MOSFETs using an ESD method, which creates shorts at random locations along the length of the gate, and a laser cutting instrument, which allows for control of the location of the short. For reasons explained above, the ESD method primarily resulted in shorts between the gate and

source/drain regions. The laser cutting method was used to obtain shorts between the gate and substrate.

Gate current (I_G) versus gate voltage (V_G) curves were measured for NMOS transistors with both of these types of gate oxide shorts. These curves showed that shorts between the n doped gate and the n+ doped source/drain regions exhibited linear or ohmic behaviour, while shorts between the n doped gate and the p doped substrate exhibited non-linear behaviour characteristic of p-n junctions. Non-linear behaviour was also observed for the gate-to-substrate shorts created in PMOS transistors using the laser cutting method. These electrical characteristics were confirmed in [30] using "real" and "simulated" gate oxide shorts in 1.5 μm technology MOSFETs. The "real" shorts were obtained by subjecting transistors to voltage stress until gate oxide rupture occurred, while the "simulated" shorts were obtained by shorting the gate to the substrate with designed contacts as described in [31].

In order to induce a conducting channel between the drain and source of a MOSFET, the gate-to-source voltage (V_{GS}) must be greater than or equal to the threshold voltage (V_{th}). However, if its resistance is sufficiently low, a gate-to-source short can prevent this. This stops the MOSFET from being turned on and permanently restricts its operation to the cutoff region.

As shown in [29] and [32], a key characteristic of logic gates containing transistors with gate oxide defects is elevated I_{DDQ}. Increased I_{DDQ} occurs whenever opposite logic voltage levels are placed on either side of a gate oxide short, providing a current path from V_{DD} to V_{SS}. Figure 2.5 shows two such possible paths in a CMOS inverter chain which can result in elevated I_{DDQ}.

In [29], inverters were constructed using either a NMOS or PMOS transistor with a gate oxide short. It was observed that the logic voltage levels for the input and output voltages of the defective inverters were slightly degraded, but were not logically incorrect. When the defective inverters were placed in a larger combinational logic circuit, the output of this circuit produced a logically correct output in almost all cases. Degraded logic 0 voltage levels can occur when a gate oxide short in a pull-up PMOS transistor prevents pull-down NMOS transistor from fully pulling down circuit node voltage levels to V_{SS}. Figure 2.6 illustrates how this can happen in an inverter chain. The converse case, where a gate oxide short in a pull-down NMOS causes a degraded logic 1, can also occur. As previously mentioned, degraded logic voltage levels are a concern because they can negatively affect noise margins.

It was also observed that gate oxide shorts can cause increased propagation delay. This can be attributed to the adverse affect that gate oxide shorts have on transistor drain currents. Simplified models of drain current (I_D) of MOSFETs are shown in Equations 2.3 and 2.4 for saturation and triode regions of operation respectively, where k is a constant determined by carrier mobility, gate oxide capacitance, and gate width-to-length ratio, V_{GS} is the gate-to-source voltage, and V_{DS} is the drain-to-source voltage:

$$I_D = k(|V_{GS}| - V_{th})^2. \tag{2.3}$$

$$I_D = k\left[(|V_{GS}| - V_{th})|V_{DS}| - \frac{|V_{DS}|^2}{2}\right]. \tag{2.4}$$

As can be seen in these equations, drain current has a quadratic dependence on

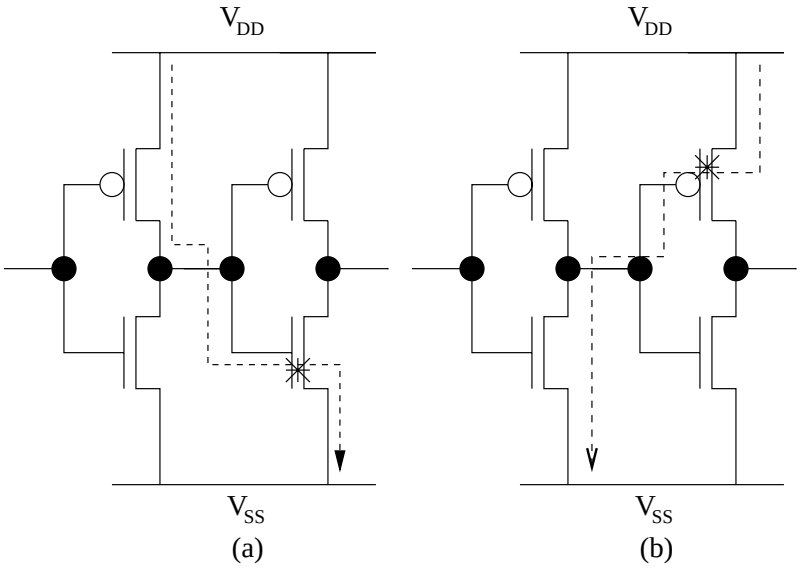


Figure 2.5: Current paths in a CMOS inverter chain caused by gate oxide shorts in (a) an NMOS transistor and (b) PMOS transistor.

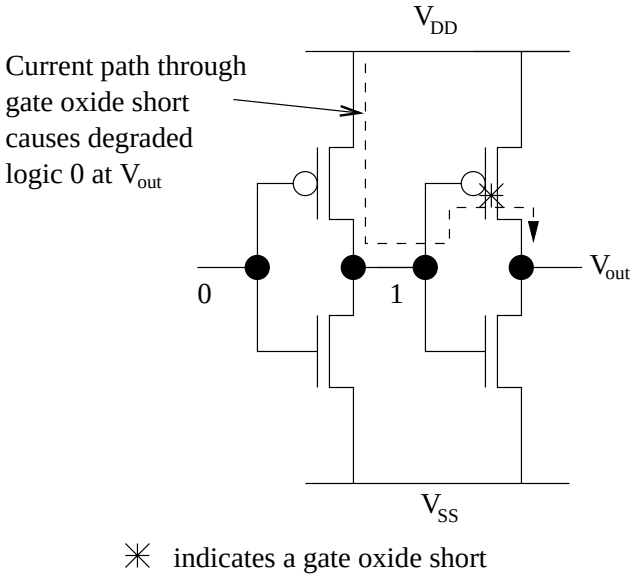


Figure 2.6: Degraded logic value caused by a gate oxide short.

V_{GS} in the saturation region and a linear dependence on V_{GS} in the triode region. Depending on its resistance, a gate-to-source short may not reduce V_{GS} enough to prevent the transistor from being turned on, as previously mentioned, but may simply serve to reduce V_{GS}. This causes decreased drain current according to equations 2.3 and 2.4. This weakened current can cause an increased delay in the charging or discharging of a circuit node, hence increasing propagation delay.

A property of gate oxide shorts that is of particular concern is that their electrical characteristics can vary with time and environmental parameters. This is due to the fact that an electric field must occur across the gate oxide for a sufficient amount of time in order for time dependent dielectric breakdown to result in a gate oxide short. It was shown in [32] that ICs with gate oxide shorts may not initially cause functional failure but can subsequently change after periods of high temperature and voltage stress to affect functionality. In [33], it was shown that, depending on the resistance value of a gate oxide short, disturbances in power supply voltage or temperature can cause functional errors that would not occur under normal operating conditions. These observations are a serious concern because they indicate that ICs with gate oxide shorts can initially escape detection during manufacturing testing, but can then later experience functional errors depending on operating conditions.

Gate oxide shorts do not necessarily produce incorrect logical behaviour [29], [32], meaning that SSF-based voltage testing is not a reliable means of detection. Elevated I_{DDQ}, however, has been shown to be a consistent characteristic of ICs containing gate oxide shorts, provided that node voltages are biased such that a voltage drop equal to V_{DD} occurs across the short.

2.3.3 Transistor Stuck-On Defects

A *transistor stuck-on defect* or simply *stuck-on defect* is any imperfection in the circuit which causes a transistor to conduct when it is not supposed to. This can result from such defects as unwanted conducting material between the drain and source terminals of a transistor, or a break in a signal line which causes a transistor gate terminal to have a floating voltage.

In [34], a defect causing a source-to-drain short is described where the active region of the transistor extends past the gate polysilicon. This is illustrated in Figure 2.7. In this case, the source and drain terminals are shorted together, allowing current to flow from drain to source (or vice versa) regardless of the voltage applied to the gate. This causes the transistor to be stuck-on. This kind of defect can be caused by particulate contaminants or errors such as mask misalignment in the fabrication process.

Another defect which can cause a transistor to be stuck-on is the *floating gate* defect. This occurs when the polysilicon gate of a transistor has a break in it, disconnecting it from its signal line and leaving it "floating". The layout of a transistor with such a defect is shown in Figure 2.8. Traditionally, transistors with floating

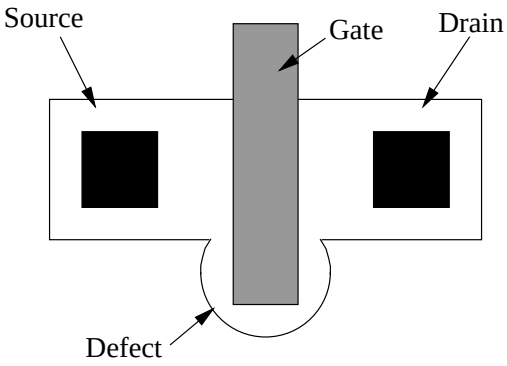


Figure 2.7: Transistor stuck-on caused by source-to-drain short.

gates have been modeled as transistors that are permanently in the cutoff region or *stuck-off*. However, it was shown in [35] that even if a transistor gate is externally disconnected, it is still capacitively coupled to the other transistor terminals, and that the transistor can be made to conduct current if enough voltage is applied to the other terminals. In [36] and [37], it was shown that if a metal line in another IC layer overlaps a floating NMOS transistor gate (as shown in Figure 2.8) and there is sufficient voltage on the metal line, the transistor can be made to conduct. This occurs if the coupling effect between the metal and poly is able to raise the gate voltage of the transistor above V_{th}. It has been shown that this is possible in a wide range of realistic situations. The degree of conduction is largely determined by the metal-poly overlap area.

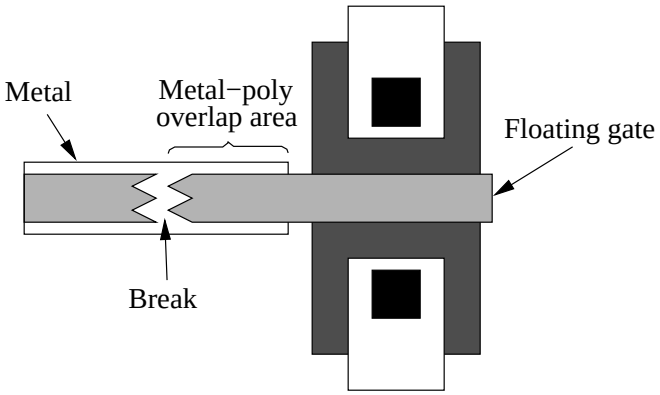


Figure 2.8: Layout of a transistor with a floating gate defect.

Figure 2.9 shows how a floating gate defect can affect the I_{DDQ} of a CMOS inverter. In this diagram, V_{metal} represents the voltage on a nearby metal line which is capacitively coupled to the gate poly of the NMOS transistor of the inverter. Though V_{in} is low, the NMOS transistor still conducts because V_{metal} is high enough to influence its gate voltage. This results in the indicated current path, which increases I_{DDQ}. V_{out}, however, may still be logically correct and may therefore escape detec-

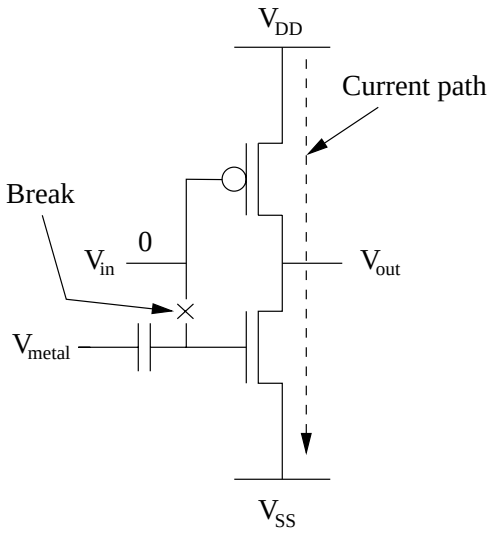


Figure 2.9: Current path caused by a floating gate defect.

tion using a voltage test as described in [38]. Much like a bridging defect or a gate oxide short, a stuck-on transistor may also result in degraded logic voltage levels and higher propagation delay by preventing a node from being completely charged or discharged, or by slowing this process.

2.4 I_{DDQ} Testing of Deep-Submicron Technology

I_{DDQ} testing is based upon the assumption that the mean I_{DDQ} value of the defect-free CMOS digital ICs in a given lot is much lower than the mean I_{DDQ} value of the defective ICs in that lot. In general, the distribution of I_{DDQ} values for a given lot of ICs is shown in Figure 2.10 where M_G is the mean I_{DDQ} value of the defect-free ICs and M_D is the mean I_{DDQ} value of the defective ICs. In practice, I_{DDQ} testing is performed by setting a current value known as an *I_{DDQ} threshold*, indicated in Figure 2.10, which separates the defect-free portion of the distribution from the defective portion. The I_{DDQ} test is a pass/fail test: ICs that have an I_{DDQ} value below the I_{DDQ} threshold are considered free of defects and ICs whose I_{DDQ} value exceeds this threshold are considered defective. The setting of this threshold is therefore extremely important in the I_{DDQ} testing process. If the threshold is set too low, then a significant number of defect-free ICs may erroneously be considered defective, and if the threshold is set too high, then many defective ICs may pass the I_{DDQ} test. Therefore, in order to set an I_{DDQ} threshold which allows for an effective test, it is highly desirable for the distributions of the defective and defect-free ICs to be separated by as large an amount as possible.

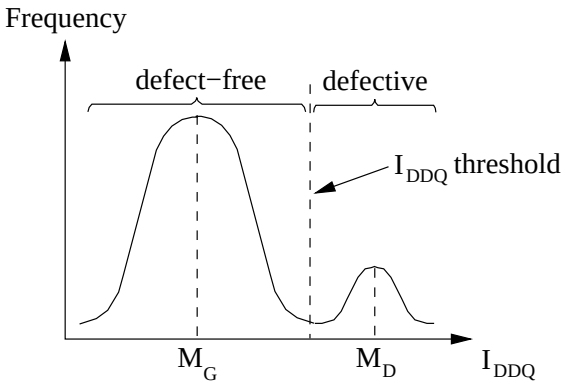


Figure 2.10: General distribution of I_{DDQ} values for a given lot of CMOS digital ICs.

2.4.1 The Problem of Scaling

Unfortunately, as manufacturing technology advances and transistor sizes continue to decrease, supply voltage and threshold voltage must also decrease in order to maintain the same internal MOSFET electric field strengths and avoid electrical breakdown. One by-product of these decreases is a resulting increase in transistor *sub-threshold leakage current*. This is the drain-source current that flows through the transistor when the gate to source voltage is less than the threshold voltage of the transistor, which is modeled by Equation 2.5 where μ is the carrier mobility, C_{ox} is the gate capacitance per unit area, $\frac{W}{L}$ is the channel width to length ratio, V_t is the thermal voltage, and η is a technology dependent parameter:

$$I_{sub} = \mu C_{ox} \frac{W}{L} V_t^2 e^{\frac{V_{GS}-V_{th}}{\eta V_t}} \left(1 - e^{-\frac{V_{DS}}{V_t}}\right). \tag{2.5}$$

Threshold voltage and V_{DS} (which scales down with V_{DD}) scale down by the same factor that is used to scale gate length, gate capacitance (which is inversely proportional to gate oxide thickness) scales up by this factor, while carrier mobility, width-to-length ratio, thermal voltage, and the technology dependent parameter all remain relatively constant [1]. For V_{GS} = 0 V, it can be shown that the reduction in threshold voltage and increase in gate capacitance will outweigh the reduction in V_{DS} and thus cause an increase in subthreshold leakage current. This serves to increase the current through transistors in static CMOS circuits when they are turned off.

Table 2.1 shows the projected characteristics of MOSFETs for high-performance digital ICs (for such applications as microprocessor units) from 2001 to 2016 [39]. As can be seen from this table, nominal NMOS sub-threshold leakage current is expected to increase by 3 orders of magnitude between 2001 and 2016.

Shrinking transistor sizes also allow IC designers to pack more transistors onto a die. The effect of greater sub-threshold leakage current combined with higher transistor counts per die is a significant increase in the I_{DDQ} of defect-free ICs. This increasing level of defect-free I_{DDQ} poses a serious problem for I_{DDQ} testing because as it rises, M_G in Figure 2.10 increases and moves closer to M_D. M_D, however, does not increase with scaling at the same rate as M_G since the resistance of the defects which cause increases in I_{DDQ} do not decrease significantly

Year of Production	2001	2003	2005	2006
Physical gate length (nm)	65	45	32	28
Nominal power supply voltage (V_{DD}) (V)	1.2	1.0	0.9	0.9
Nominal NMOS sub-threshold leakage current at 25°C (μA/μm[a])	0.01	0.07	0.3	0.7
Static power dissipation per (W/L_{gate}=3) device (Watts/Device)	5.6×10^{-9}	1.0×10^{-8}	2.6×10^{-8}	5.3×10^{-8}
Gate oxide thickness (nm)	2.3	2.0	1.9	1.9

Year of Production	2007	2010	2013	2016
Physical gate length (nm)	25	18	13	9
Nominal power supply voltage (V_{DD}) (V)	0.7	0.6	0.5	0.4
Nominal NMOS sub-threshold leakage current at 25°C (μA/μm)	1	3	7	10
Static power dissipation per (W/L_{gate}=3) device (Watts/Device)	5.3×10^{-8}	9.7×10^{-8}	1.4×10^{-7}	1.1×10^{-7}
Gate oxide thickness (nm)	1.4	1.2	1.0	0.9

Table 2.1: ITRS projections for high-performance ICs for 2001 [39]

[a] This is the gate width

with scaling. The result is that the margin of separation between the defect-free and defective portions (M_D - M_G) of the distribution in Figure 2.10 decreases. As device dimensions decrease, variations between one die and another also become more prominent. This has the effect of increasing the standard deviation around means M_D and M_G. These factors serve to create overlapping of the defect-free and defective portions of the I_{DDQ} distribution [40], making it very difficult to set an I_{DDQ} threshold which reliably separates defect-free ICs from defective ones. This is a serious threat to the quality of I_{DDQ} testing. It can be said that the *resolution* of I_{DDQ} testing is decreasing.

As if this was not bad enough news, the probability of a defect occurring increases as feature sizes are scaled down, as previously mentioned. As technology scales down, impurities and particulates that were previously inconsequential may cause catastrophic defects. In particular, maintaining gate oxide quality becomes an increasing concern as oxide thickness scales down into the sub-nanometer region. Gate oxide shorts become more likely as the thickness of the oxide scales down. Oxide thickness projections are also shown in Table 2.1. So, as technology scaling reduces the effectiveness of I_{DDQ} testing, it also increases the likelihood of IC defects. Indeed, this is alarming news for test engineers.

2.4.2 Some Solutions to the Problem of Scaling

Many researchers have tackled this problem in an attempt to extend the usefulness of I_{DDQ} testing as scaling continues. There are essentially two ways to approach this problem. One can either reduce transistor leakage currents or find a method that can differentiate between defective and defect-free I_{DDQ} despite the shrinking difference between the two. The work of this thesis falls into the latter category. In order to place the work of this thesis into context with current research, some other promising solutions are described below.

It has been shown that lowering temperature can reduce sub-threshold leakage current [41]. The general effect of varying temperature on the drain current I_D versus gate voltage V_G curve of an NMOS transistor is shown in Figure 2.11. Lowering temperature has the effect of increasing threshold voltage V_{th} and increasing slope ($\Delta I_D/\Delta V_G$) in the sub-threshold region. As can be seen in the figure, I_D at V_G = 0 V decreases with decreasing temperature. In [41] and [42], drops of 2 orders of magnitude or more in sub-threshold current were reported with a 75°C decrease in temperature. However, the factor which is responsible for the increase in V_{th} with decreased temperature, known as the *V_{th} temperature coefficient*, decreases as transistor oxides become thinner [41]. This means that the rise in V_{th} with lower temperatures will decrease as scaling continues, and that this technique will become less effective.

Another method that has been found to decrease sub-threshold leakage current is the reduction of body (or substrate) voltage, also known as *reverse body bias*

(RBB). Reducing the body voltage causes an increase in threshold voltage which in turn reduces sub-threshold leakage current. Equation 2.6 gives threshold voltage shift, where K is the body effect coefficient, ψ_B is the potential difference between the actual and intrinsic fermi level for a given process, and V_{SB} is the source to body voltage:

$$\Delta V_{th} = K\left(\sqrt{|2\psi_B + V_{SB}|} - \sqrt{|2\psi_B|}\right). \tag{2.6}$$

From this equation it can be seen how a decrease in body voltage leads to an increase in threshold voltage. Figure 2.12 shows the general effect of reducing body voltage on the I_D versus V_G curve of an NMOS transistor. A similar effect occurs for a PMOS transistor if V_{SB} is increased. Drops of 3 orders of magnitude or more in sub-threshold current with a 4 V drop in body voltage were reported in [41] and [42]. This effect has been exploited using a technique known as *multiple-threshold* CMOS. Through manipulation of body voltage, the threshold voltage of logic gate

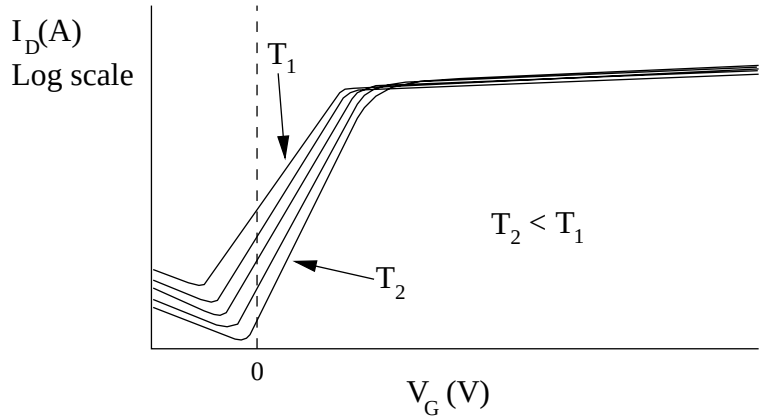


Figure 2.11: Lowered sub-threshold leakage current with lowered temperature

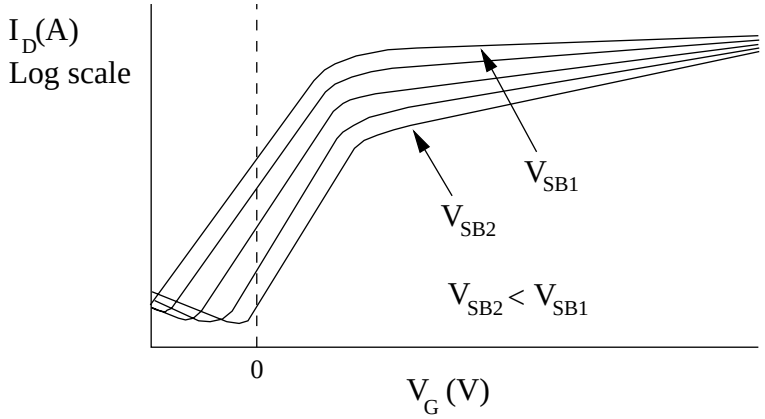


Figure 2.12: Lowered sub-threshold leakage current with lowered body voltage

transistors is raised and lowered in order to minimize leakage current during circuit operation. Transistors in noncritical paths are given higher threshold voltage to decrease leakage current, while those in critical paths are given lower threshold voltage in order to maintain performance. This technique reduces leakage current in both steady and active states. However, implementation of the RBB technique requires a significant change in standard cell library development, since logic gates must be designed with separate n-wells and substrates, and these must be biased by means of additional wiring. This requires an increase in chip area. As well, RBB becomes less effective with scaling since K in Equation 2.6 reduces with technology scaling [43]. This means that RBB becomes less effective with each successive technolgy scaling.

Silicon-on-insulator (SOI) technology has emerged as another method by which leakage currents can be reduced. SOI devices are isolated from the bulk substrate by an insulator, hence leaving each SOI device with a floating body. The major advantage gained from using SOI technology is reduced parasitic capacitances relative to bulk CMOS technology, which allows for reduced delay. Of interest to I_{DDQ} testing is the excellent sub-threshold characteristics that SOI MOSFETs have, which give lower sub-threshold leakage currents. This technology is reviewed in [44].

Other efforts have been made to distinguish defective I_{DDQ} from defect-free I_{DDQ} using data analysis techniques. In [45], it was suggested that the major difficulty in setting a reliable I_{DDQ} threshold was the current variation between one IC to the next. This variation was eliminated by using the difference between the I_{DDQ} measured for one test vector and the next in a process known as ΔI_{DDQ} *testing*. In [46], the I_{DDQ} for a number of test vectors were ordered from lowest to highest current in order to develop what is known as a *current signature*. This signature was shown to be a very sensitive indicator of defects which produced very small increases in I_{DDQ}, and was able to distinguish between defects that are indistinguishable using traditional I_{DDQ} testing.

These techniques are all intended to increase the effectiveness of I_{DDQ} testing in order to extend its usefulness into the deep-submicron era. It should be noted that, in many cases, these techniques can be used in conjunction with each other in order to combine their benefits for I_{DDQ} testing. The goal of this work is to determine whether the application of ionizing radiation can be used as another tool with which to combat the problem of scaling for I_{DDQ} testing.

2.5 Summary

In this chapter, an overview of I_{DDQ} testing was given. The unique strengths of I_{DDQ} testing were explained in order to demonstrate the value of this testing technique to the IC industry. The characteristics of the defects commonly detected by I_{DDQ} testing were described. The problem of increased subthreshold leakage current

caused by scaling was then explained, and some proposed solutions were surveyed. The work of this thesis seeks to determine whether ionizing radiation can be used to alleviate this problem. Thus, in the next chapter, we give an overview of the effects of ionizing radiation on CMOS devices.

Chapter 3

The Effect of Ionizing Radiation on CMOS Devices

Since the work of this thesis involves the investigation into the effect of ionizing radiation on CMOS IC circuitry and defects that are commonly found in CMOS ICs, an overview of radiation and its effects are presented here. Because the interaction of radiation with matter is an extremely broad and complex topic, we seek here only to give a qualitative analysis of how ionizing radiation affects the operation of CMOS circuitry. A description of ionizing radiation and an explanation of the processes by which it interacts with matter is first given. Some of the significant effects that it has on the operation of MOSFETs is then explained. Finally, the quantitative measurement of radiation is discussed.

3.1 Interaction of Ionizing Radiation with Matter

The type of radiation whose effects are explored in this work can be considered as waves of electromagnetic energy whose wavelengths are on the order of $\mathring{A}$ and are known as *x-rays*. This radiation may also be considered as *photons*, or quantized packets of electromagnetic energy, which are not electrically charged, travel at the speed of light, and interact primarily with either free electrons or those that are bound within an atom. The energy of a photon is described by Equation 3.1 where E is the photon's energy, h is Planck's constant, c is the speed of light, and λ is the wavelength:

$$E = \frac{hc}{\lambda}. \tag{3.1}$$

The interaction between x-rays and matter that we are concerned with in this thesis is the freeing of electrons from atoms. Since electrons are negatively charged, an atom with a missing electron has a net positive charge. Therefore, removing an

electron from an atom creates charged particles, also known as *ions*. This type of radiation is therefore known as *ionizing radiation*.

Depending on their energy, photons can interact with matter in one of three ways [47]. (1) A photon can penetrate the innermost electron shell structure of an atom and give up all of its energy. This energy is used by an electron, in the atom's innermost shell, to escape, thereby ionizing the atom. Any such interaction, where an electron is expelled from an atom due to the energy of a photon, is known as the *photoelectric effect*. Another electron within the atom now drops into the vacant energy level previously occupied by the expelled electron, and the difference in energy between the new and old states of this new electron is emitted from the atom in the form of an x-ray. (2) A photon can collide with an electron which is free or weakly bound to an atom. During the collision, only part of the photon's energy is transferred to the electron which is then expelled from the atom, thereby ionizing it. As a result of the collision, the photon is sent off in another direction but with less energy than it had prior to the collision. This is known as the *Compton effect*. (3) A photon can actually create matter by producing an electron and a *positron*, which is a particle with all of the properties of an electron except that it has a positive charge. During this process, known as *pair production*, the photon disappears. However, the energy necessary for pair production is not attainable by the equipment used for our experiment. We will therefore focus on the first two processes.

The photoelectric effect and Compton effect also result in spaces left by these missing electrons, known as *holes*. Holes are not actual particles but are theoretical abstractions which are considered to have a positive charge equal in magnitude to the charge of an electron. It is therefore said that ionizing radiation can generate *electron-hole pairs*. Electrons that are freed through ionization may have sufficient energy to knock another electron out of an atom, and can thus also generate electron-hole pairs themselves.

3.2 Ionizing Radiation Effects in MOSFET Materials

Ionizing radiation primarily affects the operation of MOSFETs by creating charges which are trapped within the insulating material found in and around individual transistors. This is due to the fact that electron and hole mobilities are much lower in insulators than they are in semiconductors or metals and therefore remain in insulators for long enough periods of time to cause noticeable changes [48].

3.2.1 Effect of Radiation-Induced Charges in Gate Oxide

Let us first consider the effect that a burst of ionizing radiation has on the gate oxide of an NMOS transistor with a positive voltage applied to its gate electrode. Figure

3.1 shows the process that takes place when this happens to a MOS capacitor. When ionizing radiation strikes the gate oxide, many electrons are freed from atoms in the oxide via the interactions described above, thereby generating electron-hole pairs. Shortly after this occurs, many of the electrons rejoin positive ions in a process called *recombination*. This reduces the number of free electrons and holes in the oxide. The highly mobile electrons which remain after recombination are accelerated towards the gate polysilicon and swept out of the oxide because they are attracted to the positive charge placed on it. Conversely, the relatively immobile, positively charged holes are repelled from the gate polysilicon and pushed towards the silicon substrate. In insulators, holes can be between 6 to 13 orders of magnitude less mobile than electrons [49], so the holes travel much slower than the electrons. Eventually, they become trapped at the oxide-substrate interface by the force exerted from the positively charged polysilicon, creating a layer of positive charge as indicated in the last frame of Figure 3.1.

The presence of this positive charge in the oxide near the substrate reduces the amount of positive charge that needs to be applied to the gate polysilicon in order to create an inversion layer in the channel of the transistor. This effectively lowers the threshold voltage of the transistor. In severe cases, the threshold voltage can be lowered so much that the transistor conducts with 0 V applied to the gate. The amount by which the threshold voltage is shifted due to ionizing radiation is a complicated function of the voltage bias on the gate during irradiation, the gate insulator material and its thickness, the nature of the method used to attach the gate

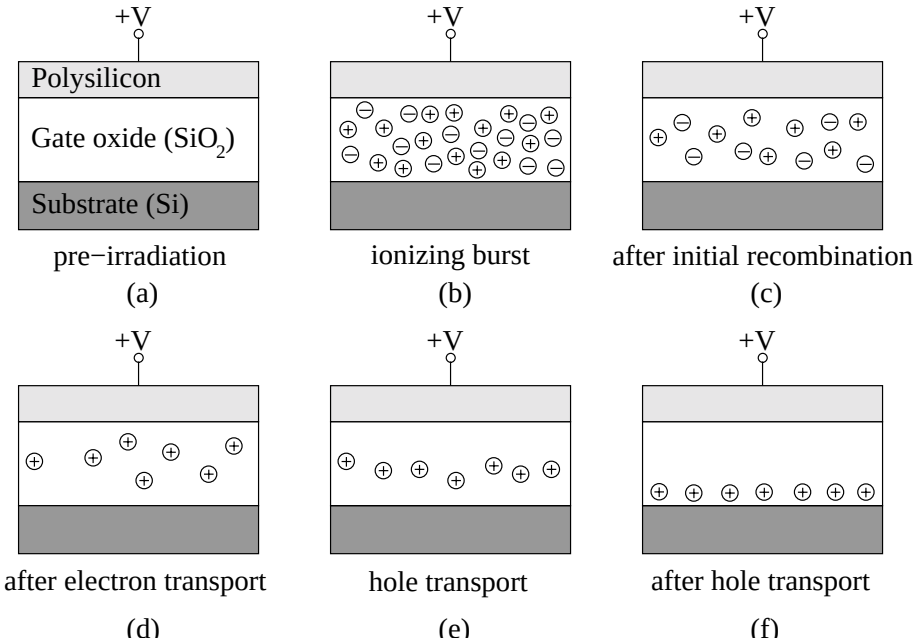


Figure 3.1: Charge trapping in gate oxide due to ionizing radiation (time increases alphabetically from (a) to (f)).

insulator onto the silicon substrate, and the changes to electron and hole mobility caused by irradiation [48].

In PMOS devices, the effect is the same except that, because the gate is negatively biased, electrons are accelerated away from the gate polysilicon and are swept out of the oxide into the substrate, and the holes are trapped in the oxide at the oxide-polysilicon interface. The threshold voltage of a PMOS transistor still undergoes a negative shift. However, the farther away the trapped positive charge is from the channel, the less the threshold voltage is affected [48]. Therefore, PMOS transistors are less susceptible to threshold voltage shift due to irradiation. After irradiation, the positive charges slowly leave the oxide, in a process called *annealing*, which can return the threshold voltage to its original value. The annealing process may even return the threshold voltage to a value above its pre-irradiation value. This behaviour is known as *rebound*.

Phenomena known as *interface traps* are capable of trapping charge carriers (both electrons and holes), and are located at the interface between the gate oxide and silicon substrate [50]. Interface traps are created when the silicon is thermally oxidized in order to create the gate oxide layer. However, additional interface traps can be generated through exposure to ionizing radiation in a process known as *radiation-induced interface trap generation*. Through this process, the threshold voltage of NMOS transistors can experience a positive shift while that of PMOS transistors can experience a negative shift. That is, the absolute value of the threshold voltage increases in both cases. The details of this phenomenon can be found in [51] and [52]. This effect acts at a slower rate than the previously mentioned effect which induces a negative threshold voltage shift due to trapped holes in the oxide. This may explain the initial decrease and later increase in threshold voltage which occurs during rebound. Unfortunately, because of the complexity involved in these effects, it is difficult to predict the sign of the threshold voltage shift in deep-submicron NMOS transistors [52].

A significant by-product of a negative shift in threshold voltage is an increase in subthreshold leakage current of an NMOS transistor since this current varies exponentially with $|V_{GS} - V_{th}|$. It should be noted that since the absolute value of the threshold voltage of a PMOS transistor is increased, the subthreshold leakage current of a PMOS transistor is theoretically lowered.

A second effect of radiation is a reduction of the slope of the logarithmic I_D versus V_G curve in the subthreshold region. The inverse of this slope, known as *subthreshold swing*, is defined by Equation 3.2 where S is the swing, k is Boltzmann's constant, T is temperature, q is electronic charge, C_d and C_{ox} are the capacitances per unit area of the depletion region in the silicon and the gate oxide respectively, and C_{it} is the capacitance asscociated with the charges created by interface traps [52]:

$$S = \frac{kT}{q}\,(ln10)\left(1+\frac{C_d + C_{it}}{C_{ox}}\right). \tag{3.2}$$

Due to radiation-induced interface trap generation, C_{it} varies with radiation. Radiation therefore influences subthreshold swing. The subthreshold swing variation as a function of the radiation-induced change in interface trap density, ΔD_{it}, is expressed in Equation 3.3 [52]:

$$\Delta S = \frac{kT}{q}\,(ln10)\frac{q\Delta D_{it}}{C_{ox}}. \tag{3.3}$$

From this equation, it can be seen that subthreshold slope decreases as ΔD_{it}, which increases with increasing dose, increases. Figure 3.2 illustrates the general trend of the subthreshold current of an NMOS transistor caused by ionizing radiation.

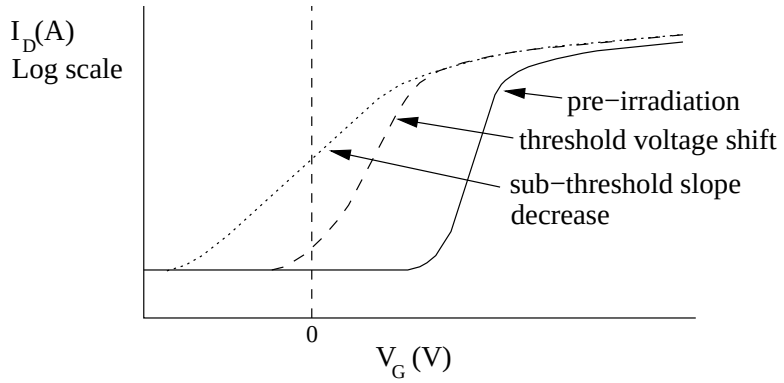


Figure 3.2: The effect of radiation on NMOS subthreshold current

3.2.2 Effect of Radiation-Induced Charges in Field Oxide

As the thickness of gate oxide scales down, its ability to retain positive charges created by ionizing radiation decreases. This is primarily due to the simple fact that there is a smaller volume of oxide where holes can be generated. It has been shown that threshold voltage shift is now proportional to oxide thickness cubed [53]. As shown in Table 2.1, the thickness of the gate oxide in modern deep submicron technology is on the order of a few nanometers or less. This gate oxide is not thick enough to retain a significant amount of positive charge after irradiation. As a result, the threshold voltage-shifting effect is becoming less of a concern. However, in CMOS circuits, the field oxide which separates transistors is significantly thicker than gate oxide and can therefore retain much more positive charge. The effect of positive charge trapping in field oxide is shown in Figure 3.3. As shown in the figure, the positive charge which becomes trapped at the oxide-substrate interface in the field oxide draws electrons towards the outer edges of the conduction channel.

The effect of this is the creation of parasitic current paths outside of the channel as illustrated in the figure. This effect, however, only affects NMOS transistors since only positively charged holes are trapped in the field oxide, which does not attract the positively charged carriers in PMOS transistors.

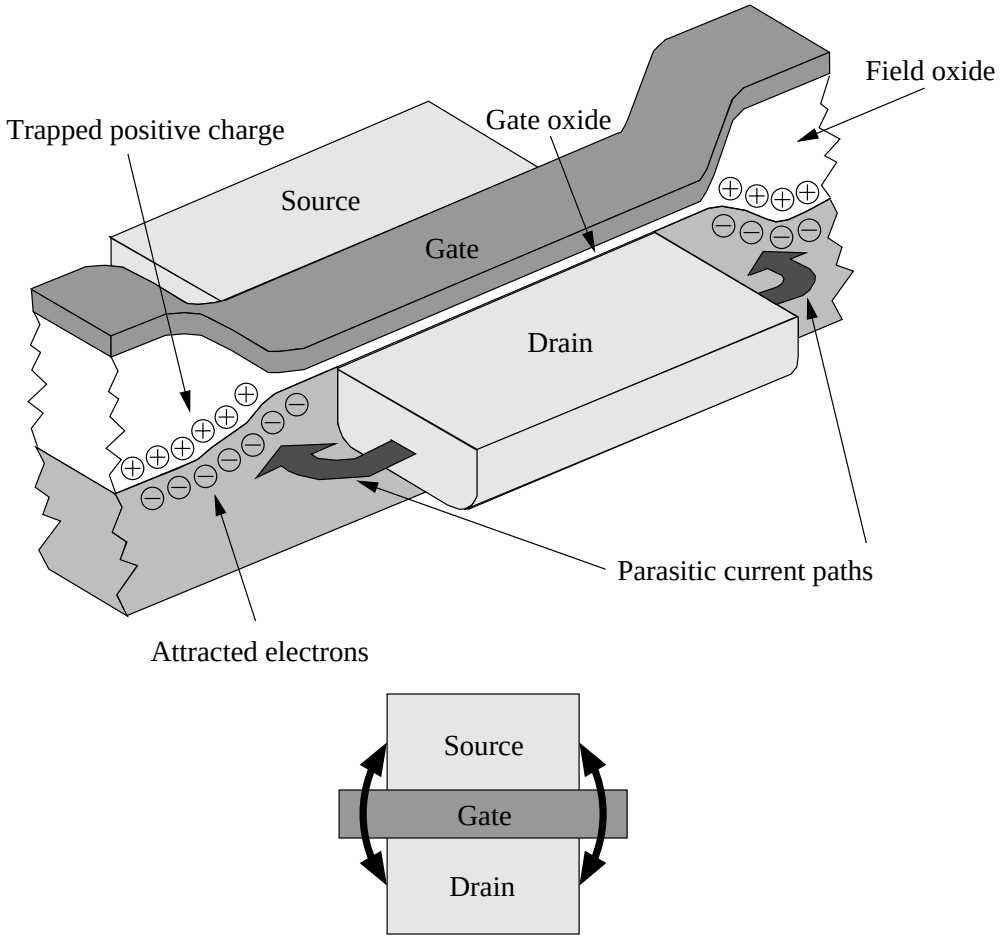


Figure 3.3: Parasitic leakage paths due to charge trapping in field oxide

3.2.3 Radiation Induced Leakage Current

An important phenomenon which affects thin oxide layers is known as *radiation induced leakage current* (RILC). Under normal conditions, when an oxide layer is sufficiently thin, electrons can travel directly from the substrate to the gate contact by a process known as *tunneling*. Radiation increases this substrate-to-gate tunneling leakage current. The mechanisms that are responsible for this behaviour are quite complex and out of the scope of this thesis, but details may be found in [54] and [55]. Basically, electrons tunnel from the substrate to positions in the oxide known as *trap states*, which are induced by the radiation. These electrons then tun-

nel from the trap states to the gate electrode. It has been shown that this leakage current is dependent on oxide thickness and gate bias, and even oxide temperature before irradiation [54], [56].

3.3 Dosimetry

The amount of ionization in an IC due to radiation is thought to be proportional to the dose absorbed by the IC. The experimental portion of this thesis involves the irradiation of electronic devices using various amounts of radiation. A description of how radiation is quantitatively measured is therefore presented here. The term *dosimetry* is usually used to describe the characterization and measurement of radiation. The SI unit of measurement which describes the amount of radiation or *dose* absorbed by a given sample of matter is the *gray* (Gy)[1]. A gray is defined as the amount of radiation which causes 1 joule of energy to be absorbed in one kilogram of matter. This energy can be transferred from the radiation to the matter through processes such as ionization, as described above, or through other processes not covered here. However, since different materials absorb different amounts of energy, because of such things as differing atomic structure, the gray must be qualified by the particular material being studied. For example, a dose of 1 Gy(Si) is the quantity of radiation needed to release 1 joule of energy into 1 kilogram of silicon. *Dose rate* describes how quickly radiation transfers energy to material and is measured in unit of dose per unit of time (i.e. Gy/s).

3.4 Summary

In this chapter, a qualitative overview of the effects of ionizing radiation on CMOS devices has been given. These effects are primarily due to the trapping of liberated charges, due to ionization, in the insulating oxides of an IC. However, due to the scaling of the gate oxide, the threshold voltage-shifting effect of charge trapping in the gate oxide is expected to be minor in deep-submicron MOSFETs. We would therefore expect the effects of charge trapping in the field oxide and radiation-induced interface traps, to be largely responsible for any observed changes in behaviour due to radiation. Consequently, in a deep-submicron NMOS transistor, we would expect to see a decrease in the slope of the logarithmic I_D versus V_G curve in the subthreshold region, and an increase in drain-source current, but only a minor shift in threshold voltage. Since deep-submicron PMOS transistors are immune to effects caused by charge trapping in the field oxide, we would expect them to only be affected by a decrease in subthreshold slope and a minor shift in threshold voltage.

[1] 1 Gy = 100 rad

Chapter 4

Experimental Details

In this chapter, the details concerning the logistics of the experiment central to the work of this thesis are explained. The experimental goals are first defined. The design of the test chip, and the various test circuits on the chip, are then explained and justifications for design decisions are given. Finally, a description of the equipment used and the test procedure followed are given.

4.1 Experimental Goals

As the reader has most likely guessed, radiation effects on electronics have been traditionally studied in order to find ways to prevent radiation from adversely affecting the proper operation of electronic systems. The area of study which seeks to render electronic systems immune to the effects of radiation is known as *radiation hardening*. Radiation-hardened electronics are essential for applications that operate in environments with high levels of radiation such as space exploration, military equipment, instrumentation for nuclear power plants, and high-energy particle accelerators.

However, when the current-altering effect that ionizing radiation has on CMOS circuits is considered by an IC test engineer, a possible benefit of radiation exposure comes to mind. As previously explained in Section 2.4.1, I_{DDQ} testing is made less effective as device scaling causes the I_{DDQ} level of defect-free circuits to approach the I_{DDQ} level found in defective circuits. This makes it increasingly difficult to distinguish defective circuits from defect-free circuits. We surmised that the application of a calculated dose of ionizing radiation could increase the resolution of I_{DDQ} testing, and thus help to alleviate this problem, if radiation were to affect defective and non-defective CMOS circuits in such a way that the difference between their I_{DDQ} levels was increased. Figure 4.1 illustrates this possible scenario. As previously explained in Chapter 3, much is known about the mechanisms by which ionizing radiation can alter current flow through individual MOSFETs. However, in a CMOS IC composed of many interconnected MOSFETs, there are numerous

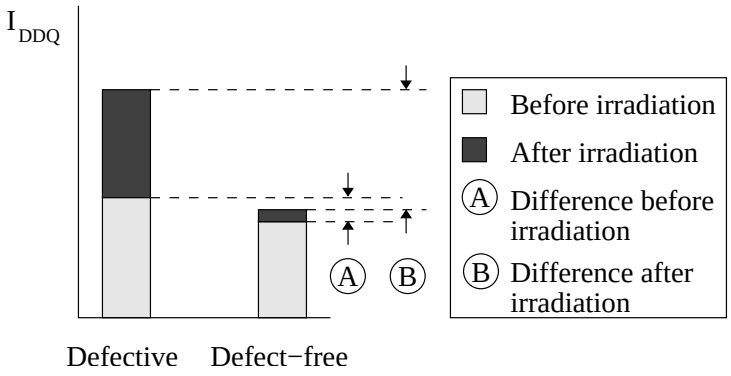


Figure 4.1: Possible beneficial effect of radiation on I_{DDQ}

complex electric fields and charge distributions that are present during its operation. Because these influences can modify the effect of radiation, it is difficult to predict how the behaviour of a CMOS IC as a whole will be altered by ionizing radiation. Inserting the defects described in Chapter 2 into these circuits introduces additional electric fields and charges, which further complicates things. The difficulty in predicting the effect of radiation on defective CMOS ICs through simulation is explained below in Section 4.2. It is therefore not unreasonable to question whether irradiation can result in the beneficial effect on the I_{DDQ} of defective CMOS ICs described above, and to investigate this possibility.

If a certain dose of radiation were to increase the I_{DDQ} level of defective circuits more than that of defect-free circuits, without causing any undesirable permanent changes to the defect-free circuits, it would be easier to distinguish between the two and the effectiveness of I_{DDQ} testing would be augmented. If this was determined to be the case, one could envision an additional step introduced into IC production testing where a given batch of ICs is irradiated using a small dose before the I_{DDQ} of each IC is measured.

The primary motivation and goal of this thesis is therefore to determine if ionizing radiation affects defective and non-defective CMOS circuits differently in a manner that is beneficial to I_{DDQ} testing. An extensive literature survey found no published studies investigating the effects of ionizing radiation on defects commonly found in CMOS circuits. Therefore, a secondary goal of this thesis is simply to report the observed effects of ionizing radiation on the behaviour of the defects being examined. This study is of interest to IC designers who may be unaware of how the electrical behaviour of defects in CMOS ICs may be altered when exposed to radiation.

4.2 Intractability of the Simulation Approach

Simulation was originally considered as a way to determine how radiation would alter the behaviour of defects in CMOS circuits. In order to take this approach, a simulation tool which could accurately model defects causing increased I_{DDQ} would first be needed. Unfortunately, industry standard IC CAD tools are not designed to model manufacturing defects. Although bridging defects can be modeled as resistive connections between two circuit nodes, defects which affect the operation of individual MOSFETs are much more difficult to model. Gate oxide shorts and source-drain shorts caused by incomplete gate polysilicon can not simply be modeled as shorts between MOSFET terminals because these defects alter the structure and operation of the affected device [30]. These defects can alter the distribution of electric potential and charge carrier flow inside the device to the point where it can no longer be described by standard MOSFET models. The simulation tools available in standard IC CAD packages are not able to accurately model such changes in device characteristics.

In addition to this, we would require another simulation model which could accurately describe the effect of ionizing radiation on these modeled defects at the MOSFET and circuit level. Unfortunately, radiation effects in electronics are dependent upon a variety of parameters such as the type of radiation, dose rate, any annealing which takes place, and the complex variety of electric fields which are present in CMOS circuits. The difficulty involved in creating an accurate model which deals with all of these parameters has perhaps prevented the development of a general-purpose model of the effects of ionizing radiation on MOSFETs and CMOS circuits. At the time of writing, no such model was commercially available. Therefore, even if it was possible to accurately model the defects of interest, it would not be possible to model the effects of radiation on the circuit containing these defects. Because of these factors, it was decided that the simulation approach was impractical and that an experimental approach was more suitable.

4.3 Test Chip Description

It was decided that the best course of action would be to obtain a series of identical but separate static CMOS digital logic test circuits, each containing either no defects or a chosen defect type to be studied. Using identical test circuits would eliminate as many extraneous variables as possible, ensuring that any changes observed between the electrical characteristics of one circuit and another would be due solely to the differences in the defects (or lack of defects) unique to each test circuit. These circuits could then be irradiated with varying doses, and any changes in electrical characteristics could be measured after each dose.

Ideally, we would be able to use industry-manufactured static CMOS digital logic circuits with actual defects. However, IC manufacturers do not generally

make their defective products available to the public in order to keep proprietary information confidential. In fact, for this reason, very little data describing the characteristics of IC defects has been made available by industry [11]. It would, in any case, also be extremely difficult to obtain various versions of the exact same industry-manufactured circuit, each containing only one type of defect of interest. It was therefore decided that we should fabricate our own test circuits.

Some requirements and criteria were initially established for the fabrication of our test circuits. The test circuits would each have completely separate power rails and would therefore also require separate power supplies during testing. This would permit the I_{DDQ} of each circuit, and therefore the effect of each defect, to be measured individually without other devices on the chip affecting the device being tested. As well, each test circuit would have its own input and output voltage lines which would allow for sensitization of defects as well as monitoring of the logical behaviour of the circuit. The I_{DDQ} of each circuit could be measured before any irradiation and after varying doses of radiation. These requirements would allow for the unambiguous observation of the effect of each defect on the I_{DDQ} of a CMOS digital logic circuit exposed to varying levels of ionizing radiation. Only then would one be able to directly compare these effects.

4.3.1 Test Chip Design Details

Since the problem of high defect-free I_{DDQ} is one which worsens as minimum feature sizes shrink, it was desirable to use the technology with the smallest feature size available for this experiment. The smallest available technology for this project was a 6-metal layer 0.18 μm CMOS process fabricated by the Taiwan Semiconductor Manufacturing Company (TSMC). The nominal V_{DD} for this process is 1.8 V. This project was allocated a maximum of 1 mm^2 of die area. Each project was also permitted to submit only one chip design for fabrication using this process. These design constraints dictated that all test circuits would need to be designed on the same die.

4.3.2 Deep n-wells

In CMOS circuits, the substrate terminals of NMOS and PMOS transistors are connected to V_{SS} and V_{DD} respectively in order to ensure that the p-n junctions at the source and drain regions are reverse biased. However, doing so effectively shorts the V_{SS} terminals of any two NMOS transistors (or V_{DD} terminals of any two PMOS transistors) which happen to share the same substrate. This violates one of the requirements of our test chip, which is that CMOS circuits on the same die (our different test circuits) must have separate V_{DD} and V_{SS} rails. The sharing of one substrate between multiple test circuits also allows the transistors of one test circuit to affect those of another test circuit, since any change in substrate voltage or any

substrate current caused by one transistor will affect other transistors with the same substrate. This is highly undesirable for our experiment. To achieve the desired isolation for our test chip, a feature known as a *deep n-well* was used. Figure 4.2 shows the structure of a deep n-well. The die in Figure 4.2 (a) shows the crosssection of a standard CMOS process without deep n-wells. As shown in the figure, the two NMOS transistors on this die share the same substrate. The die in Figure 4.2 (b) uses deep n-wells in order to isolate the two NMOS transistors from each other. As can be seen in the figure, extra barriers of n-doped material surround each transistor, keeping their substrates isolated. On the test chip die, each test circuit is built in its own deep n-well, which ensures that the NMOS and PMOS transistors of all test circuits are electrically isolated from each other.

4.3.3 Design and Fabrication of Test Circuits

The total area limit assigned for our chip design imposed restrictions on the area that each test circuit was allowed to occupy on the die, as well as the total number of bonding pads that each test circuit could use, since each bonding pad consumes additional area. Because of these restrictions, a chain of static CMOS inverters was chosen as the "template" circuit to be used. An inverter chain consumes fairly

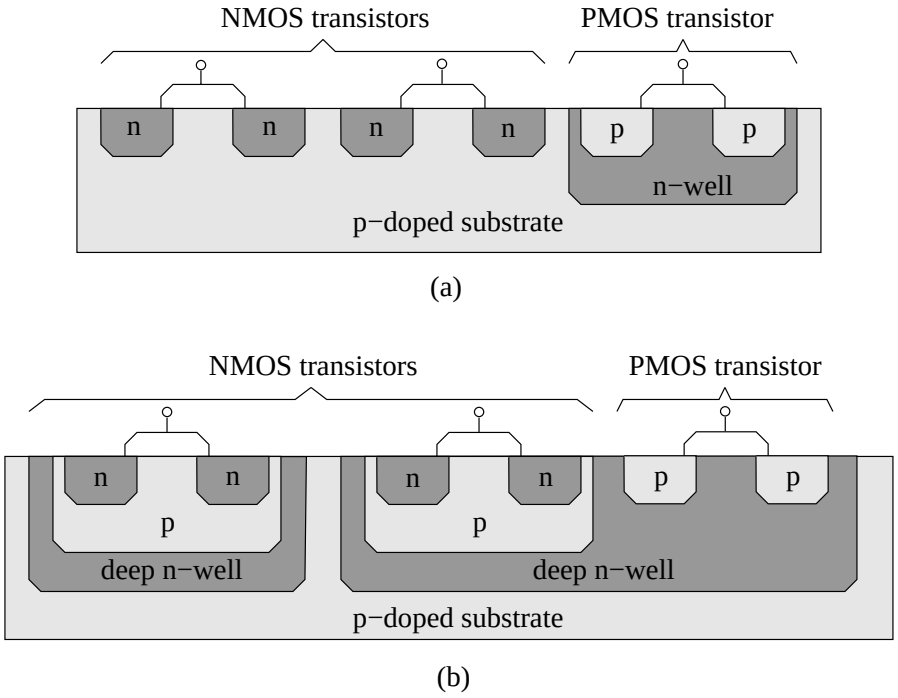


Figure 4.2: Electrical isolation using deep n-wells. (a) Without deep n-wells, the two NMOS transistors share the same p-doped substrate. (b) Using deep n-wells, the two NMOS transistors' substrates are separated by an additional layer of n-doped material.

little area, and allows high controllability and observability of logical function using a minimum number of bonding pads (only two for input and output). Multiple versions of this inverter chain were designed into the test chip: one defect-free version and one version for each defect of interest.

Ideally, an inverter from an industry-designed standard cell library would have been used. However, the layouts of these libraries are not generally made available to academic researchers, and the ability to view and alter the layout was essential in order to introduce defects into the inverter. The inverter layout used in the test chip was one from a cell library originally designed by the Canadian Microelectronics Corporation (CMC) in 0.35 μm technology, and then scaled down to a minimum feature size of 0.18 μm[1]. This was the closest thing to an industry-designed standard cell with a viewable layout that was available.

The layout of this inverter is shown in Figure A.1. As shown in the figure, the layout uses two "fingers" of polysilicon, which allows the design to be more compact. The width to length ratios of the NMOS and PMOS transistor gates are $\frac{8.66\,\mu\text{m}}{0.18\,\mu\text{m}}$ and $\frac{6.72\,\mu\text{m}}{0.18\,\mu\text{m}}$ respectively. The maximum number of inverters that would allow each test circuit to meet area requirements was used. Since each inverter added to the chain increases the chain's total I_{DDQ}, this allows the inverter chain to produce the highest possible I_{DDQ}, which is more easily measurable. 119 inverters were used in the chain, meaning that the defect-free version performs logical inversion since it is composed of an odd number of inverters. The layout of this inverter chain and the input, output, and power supply bonding pads are shown in Figure A.2. The bonding pads used were chosen from a CMC cell library, and were selected to consume as little area as possible. The input and output pads are equipped with ESD protection, which prevents surges above and below V_{DD} and V_{SS} respectively. The metal lines and number of contacts supplying power to the circuit were sized in order to accomodate the maximum allowable current supported by the pads, which is 50 mA. This was calculated from the current ratings for metal layers and contacts found in CMC documentation [57].

Simulations were performed on the extracted view of the defect-free version of the inverter chain using Cadence Analog Environment and Spectre simulation tools. Figure B.1 shows output voltage V_{out} versus input voltage V_{in} and I_{DD} versus V_{in}. As expected of a static CMOS digital logic circuit, I_{DD} is lowest for $V_{in} = V_{SS}$ and V_{DD}, and increases during the transition between the two when both NMOS and PMOS transistors are switched on.

A number of the defects described in Section 2.3 were then chosen to be studied and inserted into the various versions of the aforementioned inverter chain. While the physical features designed into the test chip to approximate actual defects (these will herein be referred to as *designed defects*) are not exact duplicates of real IC defects which occur in industry, they are intended to resemble real defects closely

[1]Thanks to Tyler Brandon from the VLSI lab at the University of Alberta for performing this conversion.

enough that the effects of radiation on these designed defects would closely approximate the effects of radiation on real defects. It is therefore important that not only the electrical characteristics of the designed defects approximate those of real defects as closely as possible, but also that the physical characteristics (shape, material, location in the IC, etc.) of the designed defects, which influence radiation effects, are close approximations as well.

In order to make the effects of radiation on these defects as visible as possible, multiple instances of each designed defect were inserted into each defective inverter chain. However, the increase in I_{DDQ} caused by the defects could not exceed the current limit of the power supply bonding pads. While this limit was calculated to be 50 mA, the influence of radiation on the additional I_{DD} caused by the designed defects was not known at the time of design. Therefore, in order to avoid the possibility of burning out metal lines connected to the bonding pads, a more conservative current limit was imposed. The number of defect instances in each defective inverter chain was kept low enough to limit the maximum I_{DD} to approximately 15 mA. Simulations were performed on the extracted views of each of the inverter chain versions in order to determine the maximum number of instances of each defect that could be included without exceeding this limit. The simulations for each defect type, as well as the number of defect instances used for each defect type, are found in the following sections. It is also desirable that all of the inserted defects in each of the defective inverter chains be sensitized by the same input voltage. This allows all of the defects to contribute to the I_{DDQ} of the circuit simultaneously, and therefore allows their effect on I_{DDQ} to be observed more easily. All of the defect instances in one defective inverter chain were therefore positioned along the inverter chain to allow this simultaneous sensitization.

4.3.3.1 Design of Bridging Defects

Bridging defects were designed at three circuit locations, each implemented in a separate inverter chain. The schematic diagrams of these three defects are shown in Figure 4.3. Figure 4.3(a) shows a designed defect between V_{DD} and the output of one of the inverters in the chain (this defect will herein be referred to as a *V_{DD} bridge*), Figure 4.3(b) shows a designed defect between V_{SS} and the output of one of the inverters in the chain (this defect will herein be referred to as a *V_{SS} bridge*), and Figure 4.3(c) shows a designed defect between the input and output nodes of an inverter (this defect will herein be referred to as an *input/output bridge*). The current paths caused by the V_{DD} bridge and V_{SS} bridge, when they are sensitized, are indicated with dashed arrows. The logic input voltages necessary for sensitization are shown at the input of the leftmost inverter. The current paths caused by the input/output bridge when $X = 0$ and $X = 1$ are indicated with a dashed arrow and a dotted arrow respectively. In the case of the input/output bridge, current paths are created regardless of the logic input voltage. The first two defect locations were

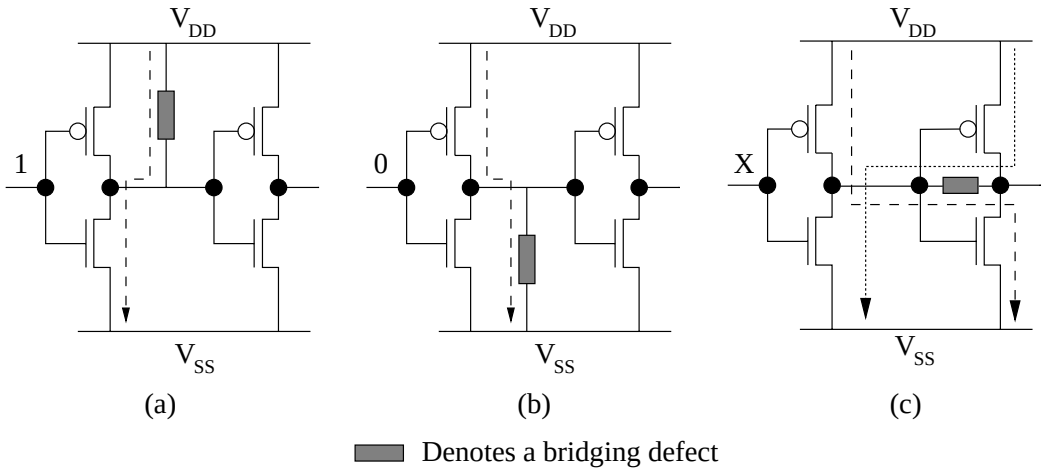


Figure 4.3: Schmatic diagram of designed bridging defects. (a) A bridging defect between a circuit node and the V_{DD} rail, (b) a bridging defect between a circuit node and the V_{SS} rail, and (c) a bridging defect between the input and output nodes of an inverter in the chain.

chosen because each of them enables a current path through a different transistor type. The V_{DD} bridge enables a path from V_{DD}, through the defect and an NMOS transistor to V_{SS}, while the V_{SS} bridge enables a path from V_{DD}, through a PMOS transistor and the defect to V_{SS}. Both of these defects were included in order to investigate the effect of radiation on the current through these two different current paths. These defect locations have been used in previous studies [15], [38]. The input/output bridge was chosen because the defect in this case causes a current path through both an NMOS and a PMOS transistor. As well, this defect involves a different conducting material than the first two, and this could also vary the effect of radiation. This will be further explained below.

Different methods for designing bridging defects were considered during the design of the test chip. A system which would allow for the varying of the resistance of the defect was considered, but it was decided that this would require some kind of an off-chip apparatus, such as a discrete resistor with variable resistance. This would obviously not mimic the physical characteristics of real bridging defects. Since metal and poly have a certain amount of resistance per square, a resistor with a desired resistance can be implemented using a specified area of metal or poly. This technique was therefore also considered in order to create a defect with a specified resistance. However, this could result in unrealisically long lengths of metal and poly which would also not physically resemble real defects.

Ultimately, the bridging defects were implemented by connecting the two affected circuit nodes with small segments of extra conductive material as shown in Figures A.3, A.4, and A.5, which show the layouts of the V_{DD} bridge, V_{SS} bridge, and input/output bridge respectively. Of the methods available to us, it was de-

cided that this would most accurately model a real bridging defect. These designed defects are approximations of bridges that could occur due to mask misalignment during metal and polysilicon deposition, or particulate contaminants with low resistance. While a particulate contaminant could theoretically land anywhere on a die, two nodes that are close together in the layout have a higher probability of being bridged by a defect than two nodes that are farther apart [5]. The segments of material used in the three aforementioned defects are therefore placed at the location in the layout where the two affected nodes are closest in the material layer of interest. The V_{DD} and V_{SS} bridges are composed of metal while the input/output bridge is composed of polysilicon. Both of these conductors were used in defects to explore the possibility that they could be affected by radiation differently. Based on the resistance specification for different materials listed in [57] and the areas of the designed defects, the resistances of the V_{DD} bridge, V_{SS} bridge, and input/output bridge were calculated as being approximately 0.153 Ω, 0.176 Ω, and 45.76 Ω respectively. These resistances all fall well within in the resistance range of the majority of defects reported in [38].

The number of instances of V_{DD} bridge defects, V_{SS} bridge defects, and input/output bridge defects is 3, 6, and 9 respectively. The simulations showing V_{out} and I_{DD} versus V_{in} for the inverter chains with V_{DD} bridge defects, V_{SS} bridge defects, and input/output bridge defects are shown in Figures B.2, B.3, and B.4 respectively. The I_{DD} of the inverter chains with V_{DD} and V_{SS} bridge defects are both higher for V_{in} = 1.8 V than for V_{in} = 0 V. This is because the defects in these two inverter chains are arranged such that all defect instances are sensitized when V_{in} = 1.8 V, while all but one of the defect instances is sensitized when V_{in} = 0 V. The difference in I_{DD} for these two inputs is therefore equal to the amount of current that each defect instance contributes to the overall I_{DD}. By dividing the I_{DD}, for V_{in} = 1.8 V, by the number of defect instances, one can see that one V_{DD} bridge defect instance contributes more current than one V_{SS} bridge defect instance. This is because, as shown in Figures 4.3(a) and (b), the current path caused by a V_{DD} bridge defect goes through an NMOS transistor while the current path caused by a V_{SS} bridge defect goes through a PMOS transistor, and the NMOS transistor in the inverter chain that we used conducts more current than the PMOS transistor. This is, however, dependent on the width-to-length ratios of the transistors and may not be the case in differently sized inverters.

V_{out} of the inverter chain with V_{DD} bridges remains at a logic 1 voltage value regardless of the value of V_{in}. This is due to the positioning of the V_{DD} bridge instance closest to the output, and to the fact that the resistance of the V_{DD} bridges are low enough that they essentially act as shorts to V_{DD}. The V_{DD} bridge instance closest to the output therefore places a logic 1 on the node it is connected to, regardless of the voltage on the input of any of the previous inverters in the chain. V_{out} of the inverter chain therefore also maintains a value of logic 1 because an even number of inverters lies between the node connected to the V_{DD} bridge and

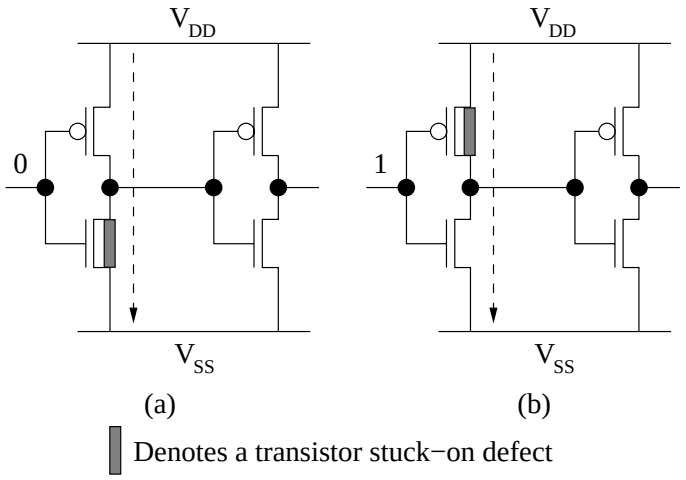


Figure 4.4: Schmatic diagram of designed stuck-on defects. (a) An NMOS stuck-on defect and (b) a PMOS stuck-on defect.

the output of the chain. The output of the inverter chain with V_{SS} bridges remains low for the same reason, except that the bridge to V_{DD} and the logic 1 in the above explanation are replaced by a bridge to V_{SS} and logic 0 respectively.

The I_{DD} of the inverter chain with input/output bridge defects is approximately the same for both V_{in} = 0 V and V_{in} = 1.8 V since, as shown in Figure 4.3(c), the defect is sensitized regardless of the voltage on the digital input of the inverter chain, and both current paths go through an NMOS transistor and a PMOS transistor. The V_{out} versus V_{in} curve for this inverter chain shows the behaviour of an inverter chain with an even number of inverters.

4.3.3.2 Design of Transistor Stuck-on Defects

Transistor stuck-on defects were designed into both NMOS and PMOS transistors, each implemented in a separate inverter chain. The schematic diagrams of these two defects are shown in Figure 4.4. The current paths caused by the defects, when they are sensitized, are indicated with dashed arrows, and logic input voltages necessary for sensitization are shown at the input of the affected inverter. As mentioned in Section 2.3.3, these defects can occur if the active region extends past the polysilicon gate, effectively shorting the source and drain terminals together. This defect was implemented on the test chip by retracting the gate polysilicon from the edge of the active region enough to leave an uncovered portion of the active area which effectively shorts the source and drain regions of the active area. The layout of the NMOS and PMOS stuck-on defects are shown in Figures A.6 and A.7 respectively. The length by which the polysilicon was retracted from the edge of the active region was arbitrarily chosen, as there is no standard length at which this defect occurs. These defects are caused by either particulate contaminants or misalignment

of masks, both of which have random dimensions. The gate of both the NMOS and PMOS transistors were retracted by 0.666 μm from the edge of the active region.

The number of instances of NMOS stuck-on defects and PMOS stuck-on defects is 6 and 4 respectively. The simulations showing V_{out} and I_{DD} versus V_{in} for the inverter chains with NMOS stuck-on defects and PMOS stuck-on defects are shown in Figures B.5 and B.6 respectively. The I_{DD} of both inverter chains is again higher for V_{in} = 1.8 V than for V_{in} = 0 V because all defect instances are sensitized when V_{in} = 1.8 V, while all but one of the defect instances is sensitized when V_{in} = 0 V. Much like the bridging defects, the PMOS stuck-on defects contribute more current than the NMOS stuck-on defects because the PMOS stuck-on defect causes a current path that goes through an NMOS transistor, which conducts more current than the PMOS transistor in the current path caused by the NMOS stuck-on defect. From the V_{out} versus V_{in} curves of both defective inverter chains, it can be seen that V_{out} maintains a logic 0 voltage value regardless of the value of V_{in}. This is again due to the positioning of the defects and their resistances as described in the previous section.

4.3.3.3 Obtaining Gate Oxide Shorts

As mentioned in section 2.3.2, gate oxide shorts occur when the insulating oxide layer beneath the gate polysilicon breaks down, causing a short between the gate terminal and either the source, drain, or substrate terminals. We had initially hoped to be able to design gate oxide shorts into individual transistors in order to have precise control over the location of the short. It was hoped that these defective transistors could then be used in inverter chains as was done with the other types of designed defects. Unfortunately, designing gate oxide shorts in this manner proved to be very problematic.

We first attempted to create gate oxide shorts by specifying missing portions of gate oxide in the layout of a transistor. However, control over the location of the gate oxide independent of the gate polysilicon was not allowed by the available fabrication process. In the process we used, wherever polysilicon is placed, oxide must also be placed under it. This made the creation of gate oxide shorts in the layout stage of the design impossible. Another approach that was considered was to use a *focused ion beam* (FIB) to mill a hole through the gate oxide of a transistor after fabrication. FIBs are commonly used to modify ICs during the debugging phase of production. In this process, ion beams are used to cut through various layers of material and deposit new conducting or insulating material in order to cut and rewire signal lines or create new vias or probe pads [58]. The possibility of creating gate oxide shorts in transistors using a FIB to penetrate the gate oxide layer was therefore investigated. However, this approach presented problems of its own. Using a FIB to create a gate oxide short in an already fabricated IC would require milling through either the gate polysilicon above the gate oxide or the silicon

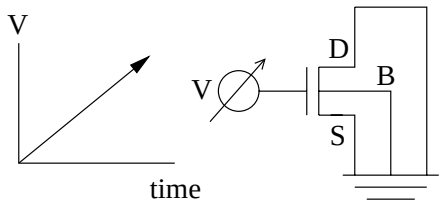


Figure 4.5: Using high voltage to create gate oxide shorts in an NMOS transistor

substrate beneath it in order to access the gate oxide layer, creating a hole in the gate oxide, and then filling this hole with conducting material. This would leave a change in the structure of either the polysilicon or the substrate which does not occur when a gate oxide short is formed by one of the methods described in section 2.3.2. More importantly, the ion doses used by FIBs to mill though typical IC materials have been found to cause oxide charge trapping and interface charge trap effects that result from exposure to ionizing radiation as discussed in section 3.2 [59]. This is highly undesirable since our experiment involves the application of ionizing radiation and we do not want the devices to be "pre-irradiated" before any measurements are taken.

It was ultimately decided that normal non-defective transistors would be fabricated, and gate oxide shorts would then be created by applying high voltage across the gate oxide. This, unfortunately, does not allow for control over the location of the short. In particular, it would most likely not be possible to create a short between the gate and substrate since the gate oxide shorts created in this manner typically occur between the gate and source or drain regions as explained in section 2.3.2. The method we anticipated using to create gate oxide shorts in an NMOS transistor is illustrated in Figure 4.5. During this procedure, the voltage on the gate terminal would be increased from 0 V, while holding the drain, source, and body terminals at ground, until a significant jump in gate current was observed. A large increase in gate current would indicate that the gate oxide has been compromised, and that current is flowing from the gate to one of the other three grounded terminals. The current on each of the three grounded terminals could be measured in order to determine the location of the short. For example, if high gate current and a corresponding high source current were observed, we could infer that the gate oxide short had occurred between the gate and source. A current limit would be imposed in order to prevent damage to the contacts or metal lines connected to the transistor. The procedure for creating a gate oxide short in a PMOS transistor would be identical, except that the gate voltage would be decreased, instead of increased, from 0 V. For reasons that will be explained in section 5.2.1, the procedure we anticipated using to create gate oxide shorts was not required for the most part.

Creating gate oxide shorts using this procedure requires individual access to each of the four terminals of the target transistor in order to determine the location of the short. Thus, if one of these transistors were to be included in an inverter

chain, as was originally intended, it would require a total of 8 pads (4 for the target transistor and 4 for the inverter chain). It was decided that including transistors with gate oxide shorts in inverter chains would require too many pads. Single transistors were therefore designed into the test chip, with pads for each of the terminals. Each single transistor was considered a separate test circuit, so a deep n-well was designed around each transistor for isolation purposes.

One NMOS and one PMOS transistor, each with minimum gate lengths of 0.18 μm, were included in the test chip design. The width for all transistors was chosen to be 6.72 μm. This width was chosen based upon the area restrictions imposed upon each circuit. No ESD protection was designed into these single transistors since our intention was to cause defects using high voltage. Based on the dimensions of the transistor, the number of connected contacts, and the current ratings for the metal layers, the maximum allowable current through each transistor is 6.72 mA.

Since the defective single transistors were not designed into inverter chains like the previously described designed defects, we were not able to simply measure I_{DDQ} before and after exposure to radiation as we would do for the various versions of inverter chains. Instead, the single transistors were characterized by obtaining various I-V curves, which are typically used to characterize transistor behaviour. These measurements are described in detail in Section 5.2.2. Of the packaged die that we received for the experiment, some of the transistors of each type were to be damaged using the procedure described above, while others were to be left undamaged. Data collected from the characteristic curves of defective and non-defective transistors would then be compared before and after various doses of radiation in order to determine how radiation affects transistors with and without gate oxide shorts, and whether radiation aids in distinguishing their currents. The idea of testing defective and non-defective versions of the same test structure, described in Section 4.3 is therefore preserved, since the differences in transistor behaviour would only be caused by the presence of the defect of interest.

4.4 Experimental Equipment and Procedure

All irradiations were performed using the X-ray accelerator located in the Centre for Subatomic Research at the University of Alberta [60]. Irradiations and measurements were performed according to the general recommendations in MIL-STD-883E method 1019.5 [61]. The dose rate produced by the accelerator is controlled by adjusting the tube potential and tube current. For this experiment, the tube potential was set at 320 kV for all irradiations. The tube current and exposure time were varied in order to obtain different dose rates and doses.

Dose measurements were made using a system involving an ion chamber which produces a small current for every photon that passes through the chamber [62].

This current is continuously integrated and converted into pulses (one pulse per nanocoulomb of charge that flows through the ion chamber) which are then counted by a pulse counter. This count can be divided by the exposure time for a given irradiation in order to obtain a *count rate*. This count rate can then be converted to a dose rate by the procedure described in [62]. Because the irradiation setup used in [62] is very similar to that used in this experiment, the dose rates calculated in [62] were adjusted for differences in environmental parameters, and then also used in this work. This is described in detail in Section 5.3.

All irradiations and measurements were performed at room temperature. All measurements were made using an Agilent 4155A Parameter Analyzer. This parameter analyzer was also used to carry out the procedure used to create gate oxide shorts described above. In order to cancel the effects of noise as much as possible, low-noise triaxial cables were used with the parameter analyzer, and the chip was placed in a grounded copper box when measurements were made. Measurements were made on the test circuits in each chip before irradiation and after irradiation with different doses. Measurements were also made 24 hours after irradiation as recommended in [61]. Since annealing occurs during this 24 hour period, as described in Section 3.2.1, this period is referred to as an *annealing period*. The periods of irradiation and the annealing period will herein be referred to as *irradiation periods*.

After each irradiation period, all measurements were made within one hour, and chips were subsequently irradiated for the next irradiation period within two hours. These requirements are stated in [61]. Because each of the chips tested contains multiple test circuits, and therefore requires many measurements to be made after each irradiation period, the parameter analyzer was controlled using a PC via a general purpose interface bus (GPIB) connection in order to speed up the measurement process and ensure that the one hour time limit was met. This allowed measurement data to be transferred directly from the parameter analyzer to the PC for storage, which takes considerably less time than saving measurement data to a floppy disk using the parameter analyzer's floppy drive. A program was written using Labview software to accomplish this.

According to [61], all irradiated circuits should be biased in such a way that the greatest radiation-induced damage is produced. However, this standard is intended to test the performance of microelectronics when a "worst-case" level of radiation effects is applied. For our unique purposes, a worst-case scenario was not necessary. In fact, it is desirable that the application of radiation produces the desired beneficial effect for I_{DDQ} testing without the use of any bias, since biasing requires power consumption. Therefore, the irradiation of some chips was initially done with an applied bias in order to ascertain the maximum effect of radiation, while others were performed without bias. When biased, the V_{GS} of the NMOS transistors was set to 1.8 V and the V_{GS} of the PMOS transistors was set to -1.8 V with V_{DS} and V_{BS} set to 0 V in both cases, while the inverter chains were biased with V_{in} and V_{DD} set

to 1.8 V and V_{SS} set to 0 V. These biasing conditions will herein be referred to as *worst case biasing conditions*. During the annealing period following irradiation, the test circuits were biased as they were during irradiation. A printed circuit board (PCB) and cable were designed and constructed in order to deliver the bias voltages to the chip. Each test circuit on a chip being irradiated was biased using a separate programmable power supply. These programmable power supplies were controlled by a PC via GPIB interface in order to measure the current drawn from each supply once per second during each irradiation period. A program was written in C++ to accomplish this. When not biased, all pins of the chip were shorted together, ensuring no differences in potential between any circuit terminals.

Precautions were followed in order to minimize the chance of damage due to ESD. During transport from the x-ray accelerator to the measurement test bench, all pins of each chip were shorted together. During storage, they were always placed in ESD protective foam. ESD grounding straps were worn whenever the chips were handled.

4.5 Summary

In this chapter, the goals of the experiment have been defined. This experiment primarily seeks to determine whether the difference between the I_{DDQ} generated by defective and non-defective CMOS circuits can be increased, with the application of ionizing radiation, in order to counteract the threat of technology scaling which jeopardizes the usefulness of I_{DDQ} testing. The reasons for the decisions made in the design of the test chip have been given and the approximations of actual CMOS defects designed into the test circuits have been explained. A description of the equipment used in the experiment as well as the test procedure followed has been presented. In the next chapter, the data obtained from the experiment is shown and the analysis of this data is explained.

Chapter 5

Results and Analysis

The methods used to analyze the data obtained from the experiment are first explained here. Because both inverter chains and single transistors were tested, the methods of analysis for each is different. We define the criteria used to divide transistors into defective and non-defective groups. The results of the experiment are then presented and the effects of radiation are analyzed in order to determine their benefit for I_{DDQ} testing. Note that in the plots in this chapter, lines have been drawn between datapoints in order to show trends but the lines do not represent data themselves.

5.1 Analysis of Inverter Chains

As previously mentioned, I_{DDQ} for V_{in} = 0 to 1.8 V was measured for each inverter chain type. However, we have chosen to focus our analysis on the I_{DDQ} for V_{in} = 0 and 1.8 V. The reason for this is based on the so called "regenerative property" of static CMOS circuits [1]. This property ensures that a voltage, which varies from the nominal logic 0 or 1 voltage values, will gradually converge to a nominal voltage value after passing through a series of static CMOS logic gates. This occurs when the gain of a static CMOS gate is greater than one in the transient region of its V_{out} versus V_{in} curve. In a complex static CMOS logic circuit with thousands of logic gates, this means that, in steady state, the input voltage seen by nearly all of the logic gates in the circuit will be either V_{DD} or V_{SS} regardless of the voltage placed on the inputs of the entire circuit. We have therefore chosen to focus our analysis on the points where V_{in} equals nominal V_{DD} or V_{SS} for the technology used - namely 0 and 1.8 V. We will, however, also show sample I_{DDQ} versus V_{in} curves for V_{in} = 0 to 1.8 V in the following sections in order to illustrate the effect of ionizing radiation on I_{DDQ} over the entire input voltage range.

For the $V_{in} = V_{DD}$ and V_{SS}, we show the change in I_{DDQ} for each inverter chain type, as well as the difference between the I_{DDQ} of each defective inverter chain and the I_{DDQ} of the non-defective inverter chain measured before exposure to radiation

and after each radiation period. This difference determines the margin of separation between the defect-free and defective portions of the distribution shown in Figure 2.10. In order to normalize these values for each chip tested, we have expressed the changes in these values as percentages of the values measured before exposure to radiation. The percentages calculated for each chip tested are then averaged over a number of tested chips where appropriate.

V_{out} versus V_{in} curves were also obtained during the experiment in order to monitor the effects of radiation on logical behaviour. Although this work is focused on current testing, we show sample V_{out} versus V_{in} curves in order to show these effects.

5.2 Analysis of Single Transistors

Due to the greater number of variables typically involved in the characterization of single transistors, their analysis is more complex than that of the inverter chains. We first explain how the transistors were divided into "low gate current" and "high gate current" groups. We then explain how the data obtained from measurements was used to compare the behaviour of these two groups after exposure to radiation.

5.2.1 Classification of Transistors Based on Gate Current

Since the transistor defect we are interested in is the gate oxide short, measurements were initially made on the single transistors, before exposure to any radiation, in order to determine the level of gate current inherent in each transistor type, and to determine whether any transistors had been damaged during fabrication or during the handling of the packaged die. This was a possibility since no ESD protection circuitry had been designed into the transistors (purposely). For measurements on NMOS transistors, gate current, I_G, drain current, I_D, source current, I_S, and body current, I_B, were measured for V_G = 0 to 1 V, while keeping drain voltage, V_D, source voltage, V_S, and body voltage, V_B, grounded at 0 V. For measurements on PMOS transistors, the above setup was the same except that V_G was varied from 0 to -1 V. These measurements will herein be referred to as *I_G measurements*. In [63], the gate current density due to electron tunneling in defect-free transistors was reported for a variety of gate oxide thicknesses. Gate current density was shown to decrease as oxide thickness increases, with gate current density measured to be on the order of 10^{-9} A/cm^2 for a gate oxide thickness slightly less than that of the process used for our test chip. Multiplying this by the area of the gates used in our fabricated transistors, we obtain a gate current on the order of 10^{-17} A for V_G = 1 V. However, gate current measurements on transistors previously fabricated using the same process indicated that we should expect gate current levels to be on the order of 10^{-12} A.

5.2.1.1 NMOS Transistors

Upon making these measurements, it was discovered that most of the NMOS transistors had a gate current which far exceeded that expected of a non-defective transistor of the designed size. The order of magnitude of I_G of the measured NMOS transistors for V_G = 1 V ranged from 10^{-8} A to 10^{-4} A. This indicated that gate oxide damage of some extent was present in all the NMOS transistors tested, which allowed for an abnormally high gate current. Figure 5.1 shows a histogram which classifies the NMOS transistors according to the order of magnitude of their gate currents measured at V_G = 1 V during the I_G measurements. NMOS transistors with comparatively higher gate current were considered as "more defective" than those with comparatively lower gate current. That is, the magnitude of gate current was used as a measure of the "defectiveness" of a transistor. NMOS transistors with I_G on the order of 10^{-7} A or lower measured at V_G = 1 V in the I_G measurement described above were classified as having "low" gate current, while those with I_G on the order of 10^{-6} A or higher measured at V_G = 1 V were classified as having "high" gate current. The former will be herein referred to as *low I_G NMOS transistors*, and the latter will be herein referred to as *high I_G NMOS transistors*. In the comparisons of transistors described in the following sections, low I_G NMOS transistors are compared against high I_G NMOS transistors.

Figure 5.2 shows the current on each terminal versus V_G for two sample NMOS transistors. In these plots, positive current values imply that current is leaving the node (i.e. flowing from the bonding pad to the transistor), while negative current values imply that current is entering the node (ie. flowing from the transistor to the bonding pad). Figure 5.2(a) shows a plot of a sample low I_G NMOS transistor. In this plot, as I_D increases in the positive direction, I_S changes with almost identical magnitude but in the negative direction, suggesting that current is flowing from drain to source. This behaviour is not fully understood since both drain and source

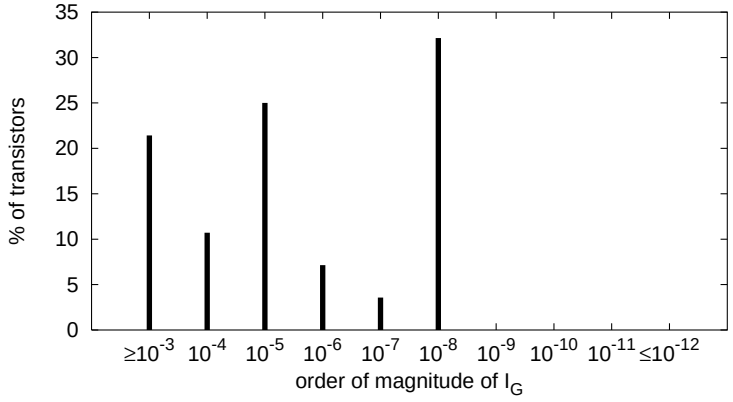
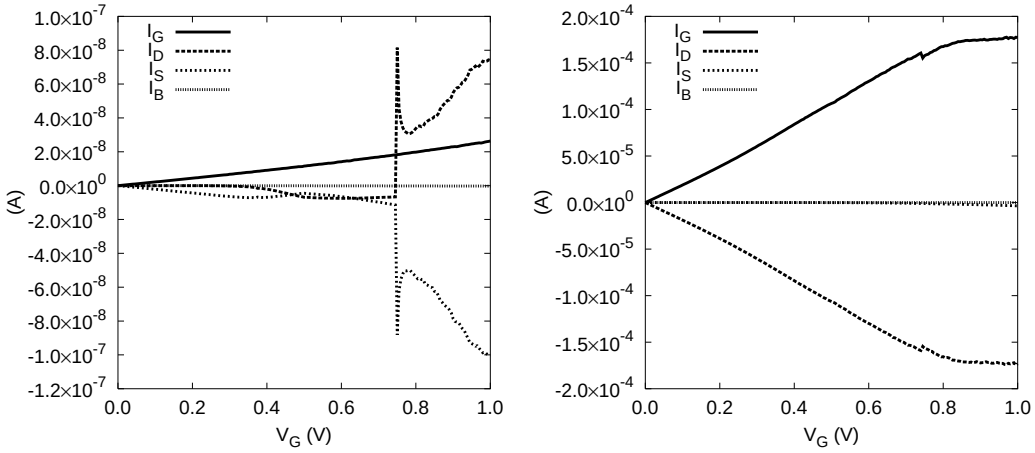


Figure 5.1: Histogram classifying NMOS transistors by order of magnitude of I_G measured at V_G = 1 V during the I_G measurement.



(a) Low I_G NMOS transistor

(b) High I_G NMOS transistor

Figure 5.2: Curves obtained from I_G measurements of (a) a sample low I_G NMOS transistor and (b) high I_G NMOS transistor.

terminals were kept at the same potential during this measurement. Nonetheless, this behaviour was consistently observed in the low I_G NMOS transistors. Note that, as can be seen in Figure 5.2(a), I_G does increase with V_G. In Section 5.2.2, we will show that this gate current flows to one of the source or drain terminals more than the other.

Figure 5.2(b) shows a plot of a sample high I_G NMOS transistor. In this plot, as I_G increases in the positive direction, I_D changes with identical magnitude but in the negative direction, while I_S remains relatively constant. This is evidence of a gate oxide short between the gate and drain. This behaviour, showing evidence of a short between the gate and either source or drain, was consistently observed in high I_G NMOS transistors. It should be noted that no NMOS transistors exhibited evidence of a short between the gate and substrate. This suggests that these gate oxide shorts were created by ESD or EOS, as explained in Section 2.3.2. The evidence of source-drain current characteristic of low I_G transistors, described above, was not seen in high I_G transistors. Therefore, along with the magnitude of I_G, this difference in behaviour between high and low I_G NMOS transistors was also used as a means of differentiating between the two.

5.2.1.2 PMOS Transistors

The gate current measurements performed on the PMOS transistors revealed that these transistors had gate currents closer to what was expected. The order of magnitude of I_G of the measured PMOS transistors for V_G = -1 V ranged from 10^{-12} A to 10^{-6} A, with the vast majority falling in the low end of this range. Figure

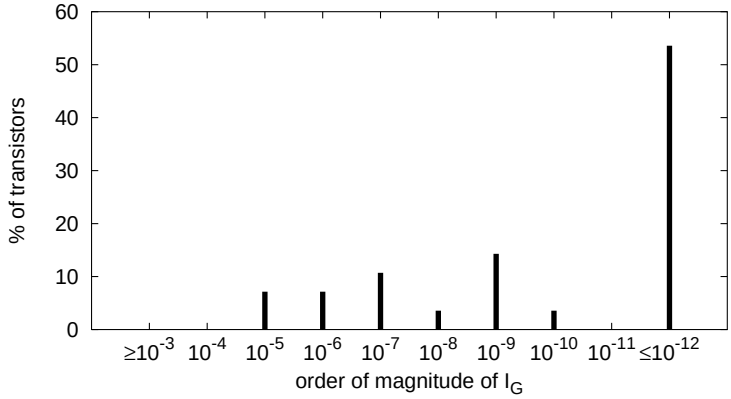
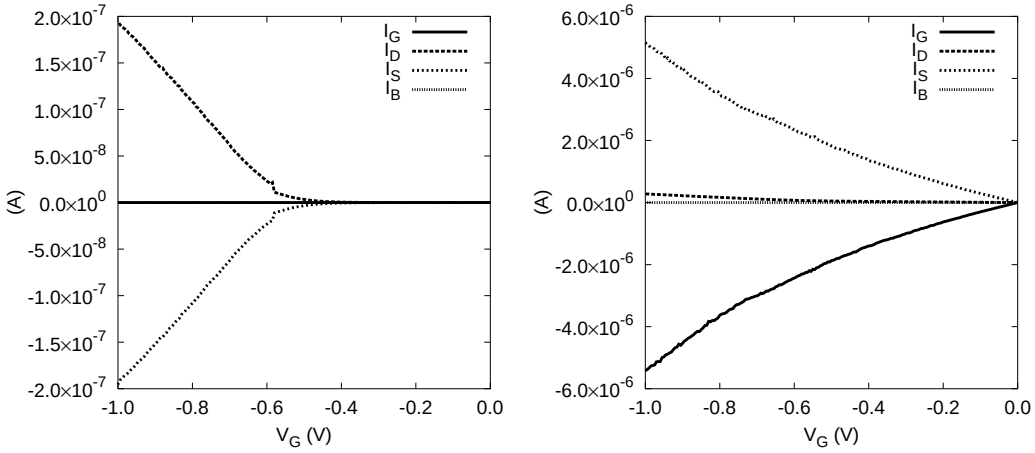


Figure 5.3: Histogram classifying PMOS transistors by order of magnitude of I_G measured at V_G = -1 V during the I_G measurement.

5.3 shows a histogram which classifies the PMOS transistors according to the order of magnitude of their gate currents measured at V_G = -1 V during the I_G measurements. PMOS transistors with I_G on the order of 10^{-12} A or lower for V_G = 1 V were classified as having "low" gate current, while those with I_G on the order of 10^{-7} A or higher for V_G = 1 V were classified as having "high" gate current. The former will be herein referred to as *low I_G PMOS transistors*, and the latter will be herein referred to as *high I_G PMOS transistors*. Figure 5.4 shows the current on each terminal versus V_G for two sample PMOS transistors.

Figure 5.4(a) shows a plot of a sample low I_G PMOS transistor. As was the case with the NMOS transistors, I_D and I_S vary with equal magnitude but opposite direction as V_G is decreased, suggesting a drain to source current. This behaviour was consistently observed in the low I_G PMOS transistors. Figure 5.4(b) shows a plot of a sample high I_G PMOS transistor. This plot is similar to that of the high I_G NMOS transistors. As I_G increases in the negative direction, I_S changes with identical magnitude but in the positive direction, while I_D remains relatively constant, suggesting a gate to source short. This behaviour, showing evidence of a short between the gate and either source or drain, was consistently observed in the high I_G PMOS transistors. Again, no PMOS transistors exhibited evidence of a short between the gate and substrate, suggesting that these gate oxide shorts were created by ESD or EOS. The evidence of source-drain current characteristic of low I_G transistors, described above, was not seen in high I_G transistors. Therefore, along with the magnitude of I_G, this difference in behaviour between low and high I_G PMOS transistors was also used as a means of differentiating between the two.

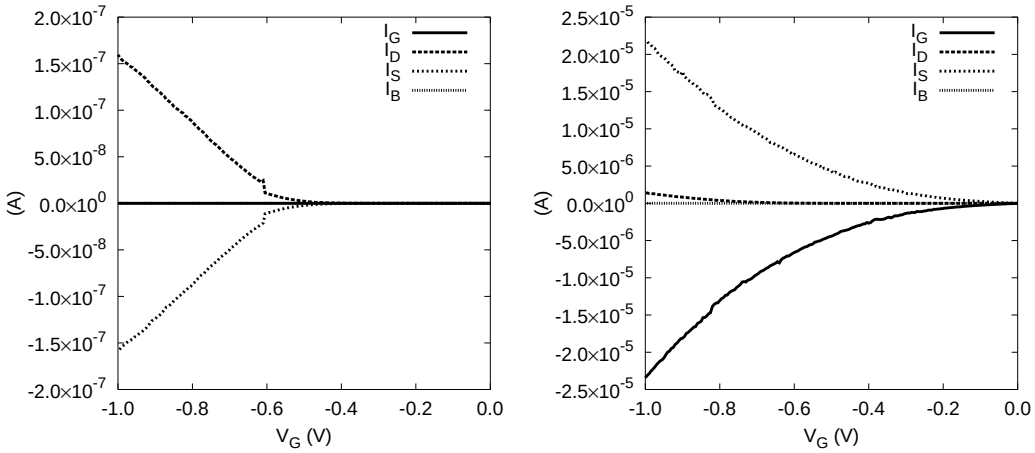
Of the fabricated PMOS transistors, those with low I_G far outnumbered those with high I_G. Therefore, in order to obtain more PMOS transistors with high gate current, the procedure for creating gate oxide shorts described in Section 4.3.3.3 was used to damage the gate oxide of some PMOS transistors with low gate current. Figure 5.5 shows plots of a sample PMOS transistor, on which the procedure was



(a) Low I_G PMOS transistor

(b) High I_G PMOS transistor

Figure 5.4: Curves obtained from I_G measurements of (a) a sample low I_G PMOS transistor and (b) high I_G PMOS transistor.



(a) Low I_G PMOS transistor before gate oxide damage

(b) Low I_G PMOS transistor after gate oxide damage

Figure 5.5: Curves obtained from I_G measurements (a) before and (b) after the gate oxide of a sample PMOS transistor was damaged by applying high gate voltage.

performed, before and after the gate oxide was damaged. The current behaviour after damaging the gate oxide, shown in Figure 5.5(b), indicates that a short between the gate and source was created. These plots are typical of the PMOS transistors that were damaged using the high voltage procedure. Some transistors showed evidence of a short between the gate and source, while others showed evidence of a short between the gate and drain. Note that the plot in 5.5(b) is very similar to the one

shown in Figure 5.4(b). This suggests that the physical nature of the gate oxide damage in both cases is similar. However, as will be shown in Section 5.5.2.2, their behaviour after exposure to ionizing radiation differed.

5.2.2 Comparison of High and Low I_G Transistors

In order to characterize transistor behaviour, a series of measurements were made on each transistor tested. For each measurement, the currents on all four transistor terminals were measured while varying different terminal voltages. The biasing scheme for each measurement is shown in Figure 5.6. These will herein be referred to as *transistor biasing schemes* (a) through (h). For each measurement, V_1 was varied from -0.2 to 1.8 V or 0.2 to -1.8 V when connected to a gate terminal and 0 to 1.8 V or 0 to -1.8 V when connected to a source or drain terminal, with a step size of 20 mV or less. This was done for each value of V_2, which was stepped through 3 or 4 values, also between -0.2 and 1.8 V or 0.2 to -1.8 V when connected to a gate terminal and 0 to 1.8 V or 0 to -1.8 V when connected to a source or drain terminal. Terminal currents were measured for each step of V_1. For NMOS transistors, V_1 and V_2 were varied from -0.2 to 1.8 V when connected to a gate terminal and 0 to 1.8V when connected to a source or drain terminal. For PMOS transistors, V_1 and V_2 were varied from 0.2 to -1.8 V when connected to a gate terminal and 0 to -1.8V when connected to a source or drain terminal. The substrate was kept at the

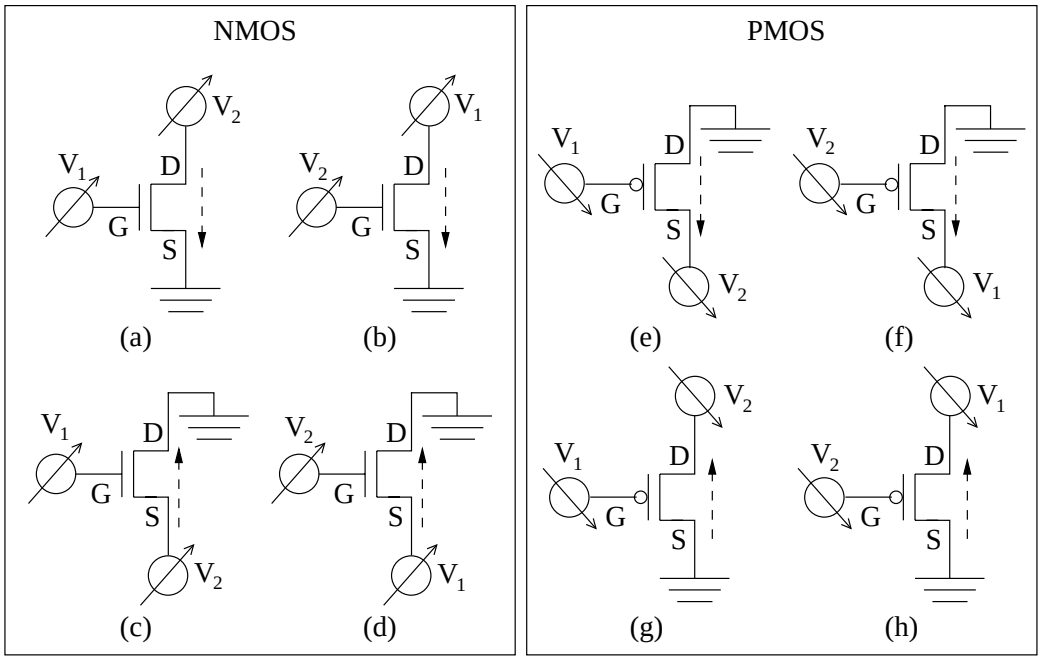


Figure 5.6: ((a) to (d)) Biasing schemes for NMOS and ((e) to (h)) PMOS transistor measurements.

lowest and highest potential for NMOS and PMOS transistors respectively (ground in both cases), as is typically done in digital static CMOS circuits. The dashed arrows show the direction of the drain-source current resulting from the biasing of each scheme. These measurements were taken in order to produce the families of I_D versus V_G and I_D versus V_D curves which are typically used to characterize transistors. Samples of these curves will be shown in order to illustrate the effect of radiation over the voltage ranges used.

Note that the biasing schemes shown in Figure 5.6(c), (d), (g), and (h) are identical to those shown in (a), (b), (e), and (f) respectively, except that the source and drain terminals are switched. We will herein refer to the biasing schemes shown in (a), (b), (e), and (f) as being in the *drain orientation* (since the biasing is such that current flows from drain to source) and those shown in (c), (d), (g), and (h) as being in the *source orientation* (since the biasing is such that current flows from source to drain). Measurements were taken for both possible orientations of each transistor. Typically, measurements are only taken for one orientation of a transistor because it is assumed that transistors are perfectly symmetric, and that the measurements taken by biasing the transistor in the drain orientation will be identical to those taken by biasing the transistor in the source orientation. However, the measurements described in Section 5.2.1 clearly showed that many of the transistors had gate oxide damage which rendered them asymetrical. We therefore expected that, if, for example, an NMOS transistor had a gate oxide short between the gate and drain, the measurements made while applying transistor biasing scheme (a) would differ from those made while applying transistor biasing scheme (c).

While measurements were made for terminal voltages varying between 0 V and 1.8 V, our analysis was once again focused on the conditions that occur during steady state. We analyzed the changes in transistor currents due to radiation when they were biased as they would be in a static CMOS inverter in steady state. As previously explained, the regenerative property of static CMOS gates ensures that the majority of the logic gates in a given complex static CMOS circuit will see an input voltage of either V_{DD} or V_{SS}. We therefore analyzed transistor currents biased in the two biasing conditions corresponding to both of these possible input voltages. These biasing conditions are shown in Figure 5.7, and will herein be referred to as *inverter biasing conditions* (a) through (d). The inverter biasing conditions occur during the application of the transistor biasing schemes, so the inverter biasing conditions were also applied for both source and drain orientations.

We were interested in seeing how the current flowing from V_{DD} to V_{SS} through transistors (the I_{DD} through the transistors) in the inverter biasing conditions changed with exposure to radiation. As explained in Section 2.3.2, gate oxide shorts cause increased I_{DDQ} in static CMOS circuits when a voltage difference (usually equal to V_{DD}) is placed across the short, causing current to flow through it. Therefore, if radiation is to significantly increase the I_{DD} through a transistor with a gate oxide short, it must increase the current flowing through the short.

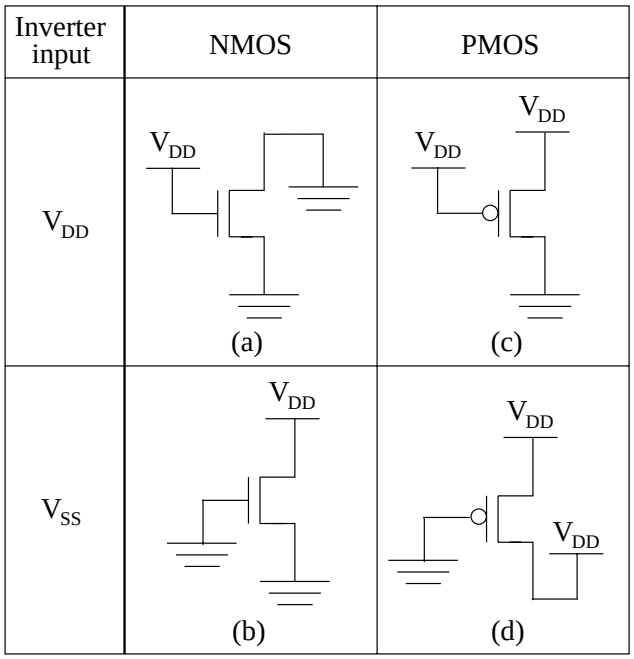


Figure 5.7: Biasing conditions for transistors in a static CMOS inverter in steady state

In order to determine the change in this current, we considered high I_G transistors biased in the inverter biasing condition which places a voltage difference of V_{DD} across the gate oxide short in the transistor. Figure 5.8 shows the inverter biasing conditions used for high I_G transistors and the direction of the current through the gate oxide short due to this biasing. These will be herein referred to as *high I_G inverter biasing conditions* (a) through (d). The transistor terminal to which the gate was shorted (either source or drain) was determined by visually inspecting the plots obtained from the I_G measurements described in Section 5.2.1. As previously explained, for high I_G transistors, these plots clearly show the terminal to which gate current flows. This terminal has been labeled as *F* in Figure 5.8, while the other terminal has been labeled *NF*. In high I_G inverter biasing conditions (a) and (d) the current measured at terminal F (I_F) is equal to the I_{DD} through the transistor composed only of the current flowing between the gate and terminal F, since the source and drain terminals are at the same potential. In high I_G inverter biasing conditions (b) and (c) I_F is equal to the I_{DD} through the transistor composed of both the current flowing from the gate to terminal F and the subthreshold leakage current, since a voltage difference of V_{DD} occurs between the source and drain terminals and the gate voltage is such that the transistor is cutoff.

The difference between the I_{DD} measured in high I_G transistors, biased in the high I_G inverter biasing conditions, and the I_{DD} measured in low I_G transistors in the same biasing conditions is, in effect, the margin of separation between the I_{DDQ} of defect-free static CMOS circuits and those containing gate oxide shorts. Thus,

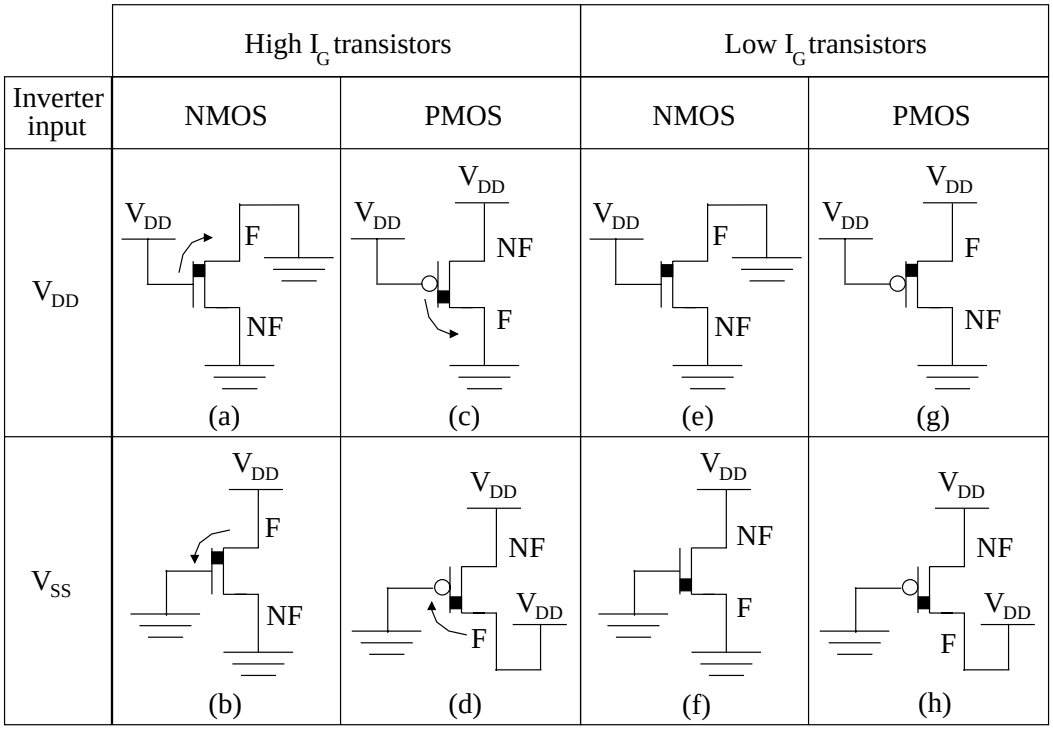


Figure 5.8: Biasing conditions for high and low I_G transistors.

if radiation is to aid in the detection of gate oxide shorts, this difference must be increased.

For a perfectly symmetrical defect-free transistor, it would not matter which orientation of the transistor we applied these biasing conditions to. However, as previously mentioned, the low I_G NMOS transistors exhibited higher gate current through one of the source/drain terminals more than the other, implying asymmetry. While this is not immediately apparent from the plots obtained from the I_G measurements, we see evidence of this in Figure 5.9, which shows plots for a sample low I_G NMOS transistor. The I_D versus V_G and I_G versus V_G curves shown in Figure 5.9(a) and (c) respectively were obtained while applying transistor biasing scheme (a) (in the drain orientation), and the I_S versus V_G and I_G versus V_G curves shown in Figure 5.9(b) and (d) respectively were obtained by applying transistor biasing scheme (c) (in the source orientation).

As can be seen, I_S in (b) is much higher than I_D in (a) for values of V_G below approximately 0.3 V, which is approximately equal to V_{th} of the NMOS transistors. For values of V_G below V_{th}, any current between the source and drain should be due to subthreshold leakage current, and should therefore be quite small. We can infer that the increased I_S in (b) is due to the contribution of current flowing from the source to gate through a gate oxide short. Note that subthreshold I_S in (b) is much

higher when V_S = 1.8 V, causing a larger voltage difference between the source and gate, and allowing more current to flow through the short. This is confirmed by inspecting plots (c) and (d). I_G in (c) stays relatively constant regardless of the value of V_D. This suggests that there is no oxide damage between the gate and drain, since, if such damage existed, we would expect I_G to increase as the potential difference between drain and gate increased. However, I_G in (d) increases as V_S is increased and shows a dramatic increase for V_S = 1.8 V. This suggests the presence of gate oxide damage between the gate and source, since we see I_G increasing as the potential difference between source and drain increases.

Given this asymmetry, we decided to bias these transistors in the inverter biasing conditions which placed a voltage difference of V_{DD} across the gate and the terminal through which the least gate current was observed. Doing so causes the least possible amount of current to flow through the gate oxide, thus minimizing the contribution of gate current to the I_{DD} flowing through the transistor. This allows us to approximate, as closely as possible, a transistor without gate oxide damage. The terminal through which the least gate current flows in a low I_G NMOS transistor will also herein be referred to as terminal *NF* while the other terminal will herein be referred to as terminal *F*. This terminal was determined for each low I_G NMOS transistor tested by examining the curves shown in Figure 5.9. For example, in the low I_G NMOS transistor, from which the curves in Figure 5.9 were obtained, the terminal through which the least gate current flows is the drain. The biasing conditions applied to low I_G transistors are shown in Figure 5.8 (e) to (h) and will herein be referred to as *low I_G inverter biasing conditions* (e) through (h). In low I_G inverter biasing conditions (e) and (h) the current at terminal NF (I_{NF}) is equal to the I_{DD} through the transistor composed only of the current flowing between the gate and terminal NF, since the source and drain terminals are at the same potential. In low I_G inverter biasing conditions (f) and (g) I_{NF} is equal to the I_{DD} through the transistor composed of both the current flowing between the gate and terminal NF and the subthreshold leakage current, since a voltage difference of V_{DD} occurs between the source and drain terminals and the gate voltage is such that the transistor is cutoff.

As previously mentioned, the low I_G PMOS transistors exhibited much less gate current than the low I_G NMOS transistors. In the PMOS transistors, there was no evidence of an inbalance of current between the gate and source and the gate and drain in plots obtained from transistor biasing schemes (e) and (g), as there was in the plots obtained from transistor biasing schemes (a) and (c) for NMOS transistors (as shown in Figure 5.9). Terminal NF was therefore arbitrarily chosen in low I_G PMOS transistors.

In the following sections, we analyze the change caused by exposure to radiation in the differences between I_F, measured in high I_G transistors biased in high I_G inverter biasing conditions (a) through (d), and I_{NF}, measured in low I_G transistors biased in low I_G inverter biasing conditions (e) through (h) respectively. These

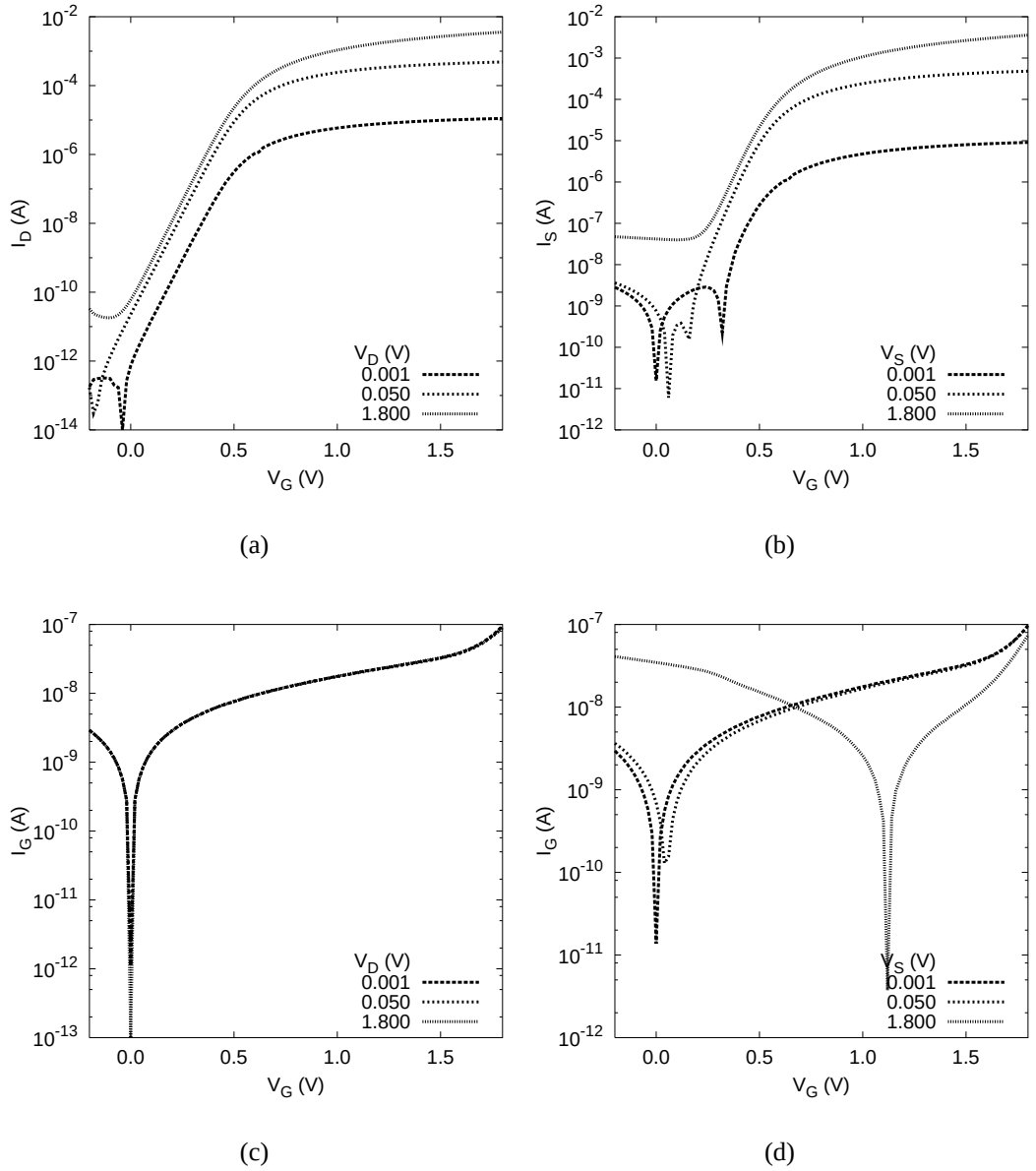


Figure 5.9: Curves of a sample low I_G NMOS transistor obtained from biasing in ((a) and (c)) the drain orientation and ((b) and (d)) source orientation.

are the differences between the I_{DD} flowing through high I_G transistors and the I_{DD} flowing through low I_G transistors, when these transistors are biased as they would be in an inverter chain with an input voltage of V_{DD} and V_{SS}. As previously explained, this difference must be increased for radiation to aid in the detection of gate oxide shorts.

5.3 Dose Calculations

In order to the determine the doses absorbed by the irradiated devices during irradiations, equation 5.1 [62] was used, where D_{die} is the dose rate absorbed by the microelectronic die on which the test circuits were fabricated, N_{NB} is the count rate obtained when no material except air is placed between the x-ray source and the ion chamber, C_{cal} is a calibration constant, C_{X2D} is a constant which converts exposure to dose in air, C_{PTH} is a constant that accounts for the environmental condition under which the measurements are done, C_{pos} is a constant that accounts for the position of the die relative to the position of the ion chamber, W_i' is the fraction of the dose in some material C due to photons of discrete energy E_i, $C_{atten}(E_i)$ is a conversion factor that corrects for the attenuation of the x-ray photons through a given material, and $C_{mat}(E_i)$ is a conversion factor that converts the dose of one material to another. Details of this equation and the determination of the constants used can be found in [62]:

$$D_{die} = N_{NB} \cdot C_{cal} \cdot C_{X2D} \cdot C_{PTH} \cdot C_{pos} \cdot \sum_i \left(W_i' \cdot C_{atten}(E_i) \cdot C_{mat}(E_i) \right). \qquad (5.1)$$

Because the irradiation test setup used in our experiments is very similar to that used in [62], we have reused many of the constants in Equation 5.1 determined in [62]. We have assumed that the calibration constant C_{cal} applies for our experiments and have reused it. The constant C_{X2D} which converts exposure to dose in air is also applicable for our experiment. Because the materials and material thicknesses used in the die package and PCB for this experiment are essentially identical to those used in [62], we have also reused the value of $\sum_i (W_i' \cdot C_{atten}(E_i) \cdot C_{mat}(E_i))$.

The count rate N_{NB} was obtained by performing test runs of the x-ray accelerator, with no material except air between the x-ray source and the ion chamber, at tube currents corresponding to each dose rate used. These are given in the sections below describing the irradiation experiments performed. The constant C_{PTH} was calculated from the recorded pressure, P, and temperature, T, at which the irradiations were done. This constant is given by Equation 5.2 [62], where P_{ref} = 705 mmHg and T_{ref} = 22.7°C:

$$C_{PTH} = \frac{P_{ref}}{P} \cdot \frac{T + 273.2}{T_{ref} + 273.2} \cdot 0.997. \qquad (5.2)$$

There were two environmental conditions under which the irradiations were done, so two values of C_{PTH} were calculated and are given in the sections below. The constant C_{pos} was calculated from the distance between the x-ray source and the die, z, and the distance between the x-ray source and the ion chamber, $z_{chamber}$.

This constant is given by Equation 5.3 [62] and was calculated as being 2.42 for this experiment:

$$C_{pos} = \left(\frac{z_{chamber}}{z} \right)^2 . \tag{5.3}$$

The dose rate calculated in [62] (0.46 Gy(SiO_2)) was therefore divided by the values of N_{NB}, C_{PTH}, and C_{pos} used in [62], and then multiplied by the values for these constants calculated for our experiment. This effectively readjusts the dose rate calculated in [62] to account for the differences in environmental parameters. The readjusted dose rates are used in the sections below.

5.4 Exposure To High Doses

The stated goal of this work is to determine whether ionizing radiation can be used to influence the current flowing through defective and non-defective CMOS circuits in a manner that is beneficial to I_{DDQ} testing. For this to occur, a dose of radiation that does not cause any undesirable permanent changes to non-defective circuits must be applied. In order to determine the dose at which these changes occur, a series of irradiation tests were done using a set of doses within a relatively large range. For these doses, the x-ray accelerator was run at a tube current of 10 mA. The temperature and atmospheric pressure during these irradiations were measured to be 22.2 °C and 762 mmHg respectively. The count rate at this tube current was recorded as 23.85 counts/s and the dose rate was computed to be 0.779 Gy(SiO_2)/s. This dose rate will herein be referred to as the *high dose rate*. The cumulative exposure times and doses used are listed in Table 5.1. These doses will herein be referred to as *high doses*. The cumulative doses will be used when referring to the total amount of radiation a test circuit absorbed prior to making a set of electrical measurements.

Cumulative Exposure Times (min)	Cumulative Doses (Gy(SiO_2))
5	230
15	700
30	1400
90	4200

Table 5.1: Cumulative exposure times and doses using high dose rate.

During these irradiations, test circuits were biased in the worst case biasing conditions described in Section 4.4 and the power supply currents of each test circuit were measured during irradiation. The effects of these doses on the test circuits are presented and analyzed here. As well, we examine the effects of these doses on the

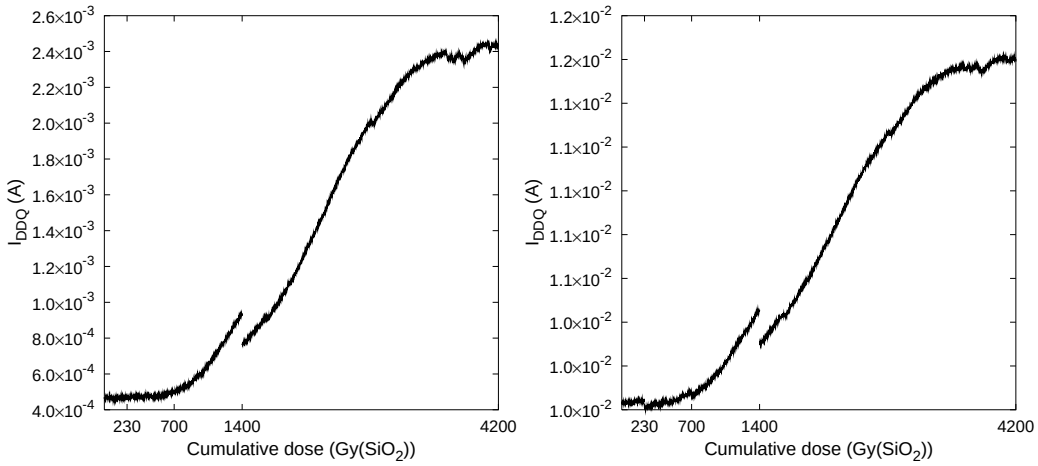
differences between the currents of defective and non-defective inverter chains and transistors as described in Sections 5.1 and 5.2.2. Henceforth, the multiple copies of a given test circuit located on different test chips will be referred to as *instances*.

5.4.1 Inverter Chains

For logistical reasons, only the inverter chain types with no defects, with V_{DD} bridges, with V_{SS} bridges, and with input/output bridges were irradiated using high dose rates. Curves showing I_{DDQ} versus time for sample defect-free, V_{DD} bridge, V_{SS} bridge, and input/output bridge inverter chains obtained during irradiation are shown in Figure 5.10. These values were measured once per second during irradiation. As can be seen, the I_{DDQ} of these four inverter chains all increase in the same manner. An increase of approximately 2 mA is seen after an absorbed dose of 4200 Gy(SiO_2), with steady increase beginning after approximately 700 Gy(SiO_2). As previously mentioned, irradiation was stopped for approximately one hour for parameter analyzer measurements after absorbed doses of 230, 700, 1400, and 4200 Gy(SiO_2). A noticeable drop in I_{DDQ} is seen after the stoppage at 1400 Gy(SiO_2).

Plots of I_{DDQ} versus V_{in} curves for sample inverter chains of these four types, measured before irradiation and after each irradiation period (including the 24 hour annealing period labeled as *Post-rad* in the legend) are shown in Figure 5.11. The pre-irradiation curves closely match those generated by simulation found in Appendix B. As can be seen in the plot for the defect-free inverter chain shown in (a), when both NMOS and PMOS transistors are on ($V_{tn} \leq V_{in} \leq V_{tp}$), the level of I_{DDQ} is not significantly affected by irradiation. However, for values of V_{in} closer to V_{SS} and V_{DD}, I_{DDQ} is greatly increased. This shows that the subthreshold leakage current of the transistors are affected much more by radiation than the current of the transistors in triode and saturation regions of operation, as expected. This also indicates that this dose is too high to be useful for I_{DDQ} testing, since it is highly undesirable for the I_{DDQ} of defect-free circuits to experience such an increase in subthreshold current. The I_{DDQ} of the 3 defective inverter chains tested also increase but do not experience jumps of orders of magnitude as is the case with the defect-free inverter chain. It can be seen that for each inverter chain type, the current increases with increasing dose, and then decreases, but does not return to the pre-irradiation value, after the annealing period.

Plots of V_{out} versus V_{in} curves for sample inverter chains of these four types, measured before irradiation and after each irradiation period, are shown in Figure 5.12. From these curves, it can be seen that these doses had no discernible effect on the logical behaviour of the defect-free inverter chain. The V_{out} of the inverter chain with V_{DD} bridges experienced a decrease with increasing dose, and an increase after the annealing period. Conversely, V_{out} of the inverter chain with V_{SS} bridges experienced an increase with increasing dose, and a decrease after the annealing period. However, in both these cases, V_{out} was not affected enough to cause a



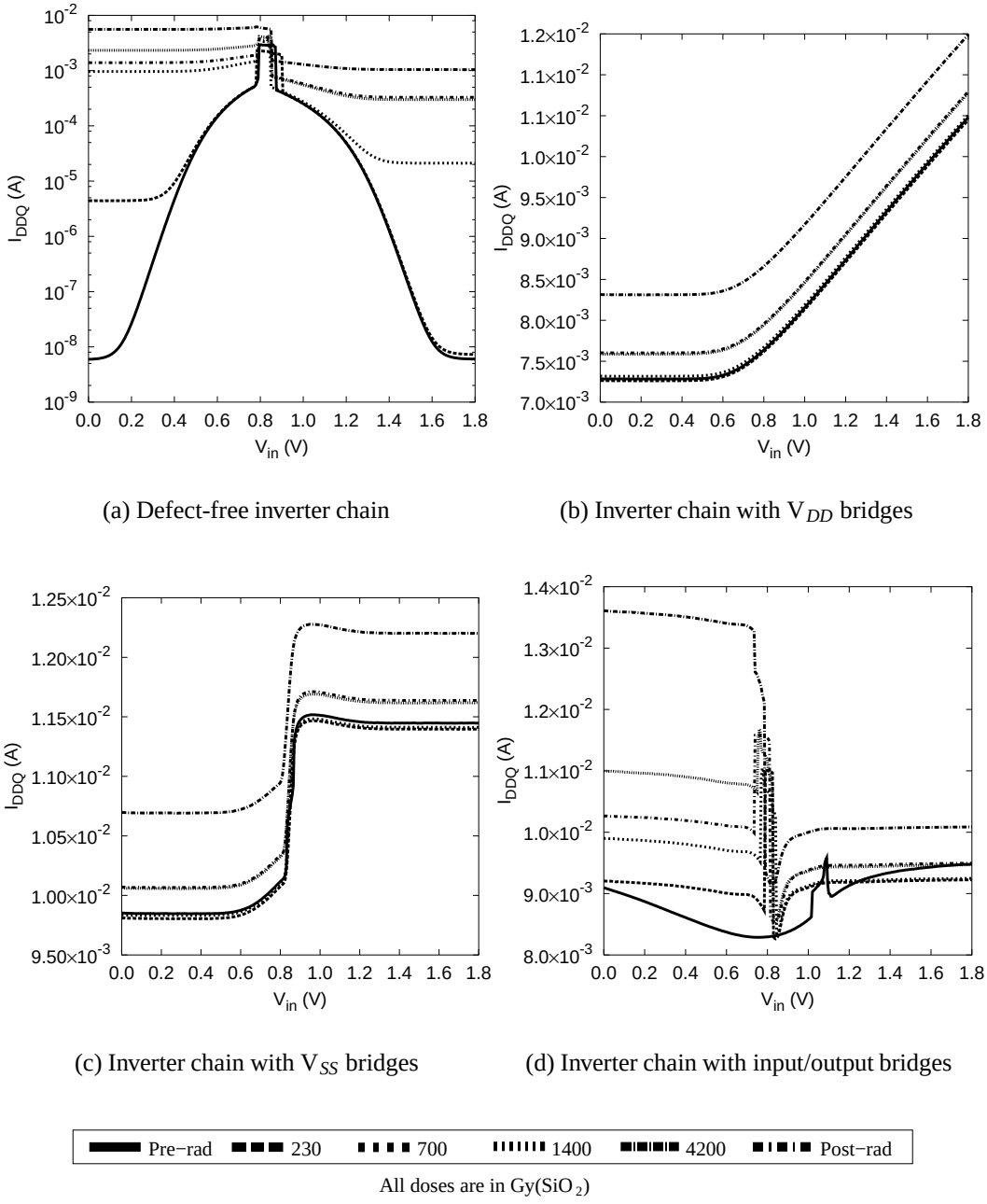
(a) Defect-free inverter chain

(b) Inverter chain with V_{DD} bridges

(c) Inverter chain with V_{SS} bridges

(d) Inverter chain with input/output bridges

Figure 5.10: I_{DDQ} of sample inverter chains (a) with no defects, (b) with V_{DD} bridges, (c) with V_{SS} bridges, (d) and with input/output bridges measured during irradiation.



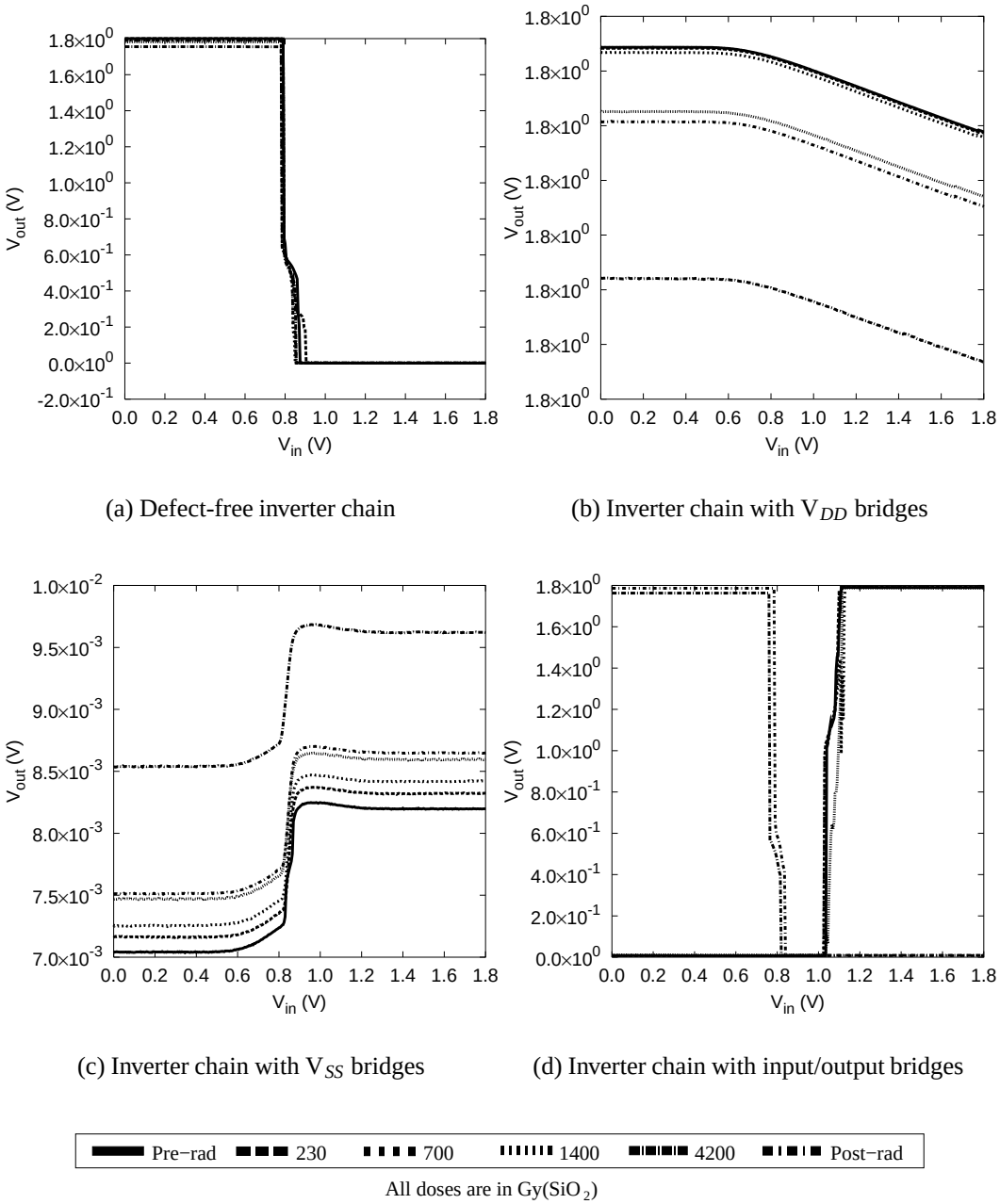
(a) Defect-free inverter chain

(b) Inverter chain with V_{DD} bridges

(c) Inverter chain with V_{SS} bridges

(d) Inverter chain with input/output bridges

Figure 5.11: I_{DDQ} versus V_{in} curves of sample inverter chains (a) with no defects, (b) with V_{DD} bridges, (c) with V_{SS} bridges, and (d) with input/output bridges measured before irradiation and after each irradiation period.



(a) Defect-free inverter chain

(b) Inverter chain with V_{DD} bridges

(c) Inverter chain with V_{SS} bridges

(d) Inverter chain with input/output bridges

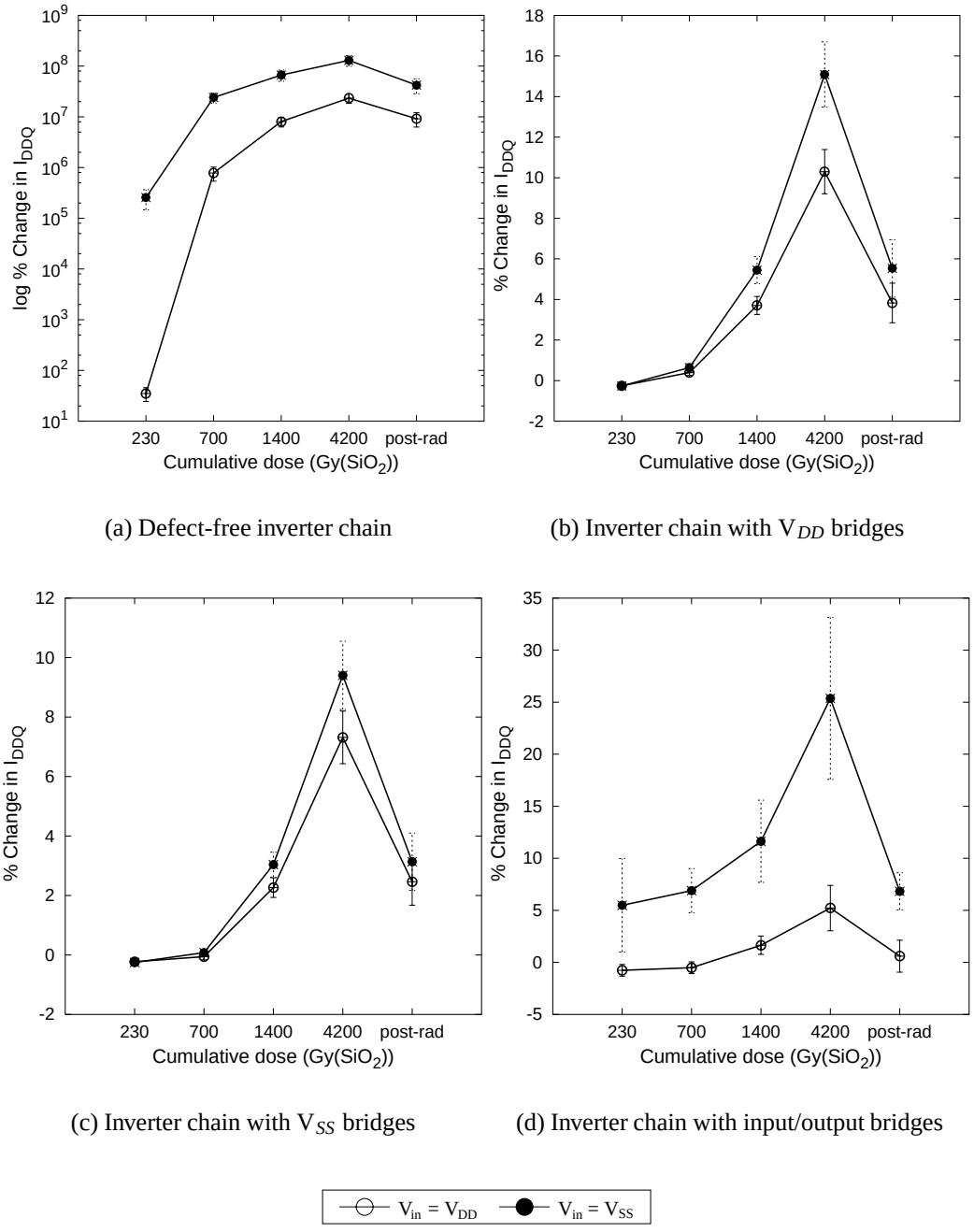
Figure 5.12: V_{out} versus V_{in} curves of sample inverter chains (a) with no defects, (b) with V_{DD} bridges, (c) with V_{SS} bridges, and (d) with input/output bridges measured after each irradiation period.

change in logic state. Interestingly, the inverter chain with input/output bridges experienced an inversion of logical behaviour after the entire 4200 Gy(SiO_2) dose. In another instance of this inverter chain, this inversion occurred after an absorbed dose of 230 Gy(SiO_2). Unfortunately, the reasons for this are difficult to determine.

As previously mentioned, we are most interested in the effect of radiation on the I_{DDQ} of each inverter chain type for $V_{in} = V_{DD}$ and V_{SS}. In order to determine this, the I_{DDQ} measured after each irradiation period was subtracted from the pre-irradiation value of I_{DDQ} for $V_{in} = V_{DD}$ and V_{SS}, and this difference was then expressed as a percentage of the pre-irradiation value of I_{DDQ}. That is, the percent change in the pre-irradiation I_{DDQ} was found for each irradiation period. The term *percent change* will herein be used to refer to the results of this calculation for a given value of interest. This was done for 4 instances of each inverter chain type irradiated to high doses. The mean and standard error[1] over these 4 instances was then calculated. Figure 5.13 shows the mean values, calculated over the 4 instances of each inverter chain type, and the standard error, indicated by errorbars. We can again see the increase in I_{DDQ} with increasing dose, and a subsequent decrease after annealing. As can be seen from this figure, the I_{DDQ} of the defect-free inverter chain increases far more than that of the 3 defective inverter chain types. Unfortunately, this is the opposite of the behaviour that would be beneficial for I_{DDQ} testing as shown in Figure 4.1, where the I_{DDQ} of defect-free circuits do not increase with radiation and that defective circuits do.

The percent change in the difference between the I_{DDQ} of each defective inverter chain type and the defect-free inverter chain, after each irradiation period, for $V_{in} = V_{DD}$ and V_{SS}, was also calculated. This difference is, in effect, the margin of separation between the defect-free and defective portions of the distribution shown in Figure 2.10. This was done for 4 instances of each inverter chain type irradiated to high doses. That is, the I_{DDQ} of the first instance of each of the defective inverter chain types was subtracted from the first instance of the defect-free inverter chain, the I_{DDQ} of the second instance of each of the defective inverter chain types was subtracted from the second instance of the defect-free inverter chain, etc. The mean and standard error over the 4 differences (one for each instance) was then calculated for each defective inverter chain type. Figure 5.14 shows the mean values of these differences and the standard errors, indicated by the errorbars. As can be seen, this difference for each of the defective inverter chain types irradiated to high doses remains relatively constant for $V_{in} = V_{DD}$ but decreases after each irradiation period for $V_{in} = V_{SS}$. This again shows behaviour contrary to what would be beneficial for I_{DDQ} testing.

[1] Standard error, in layman's terms, is defined as the standard deviation of the mean, which we have obtained, from the mean we would expect to obtain by repeatedly performing the experiment. Mathematically, it is the standard deviation of a data set divided by the square root of the number of samples in the data set.



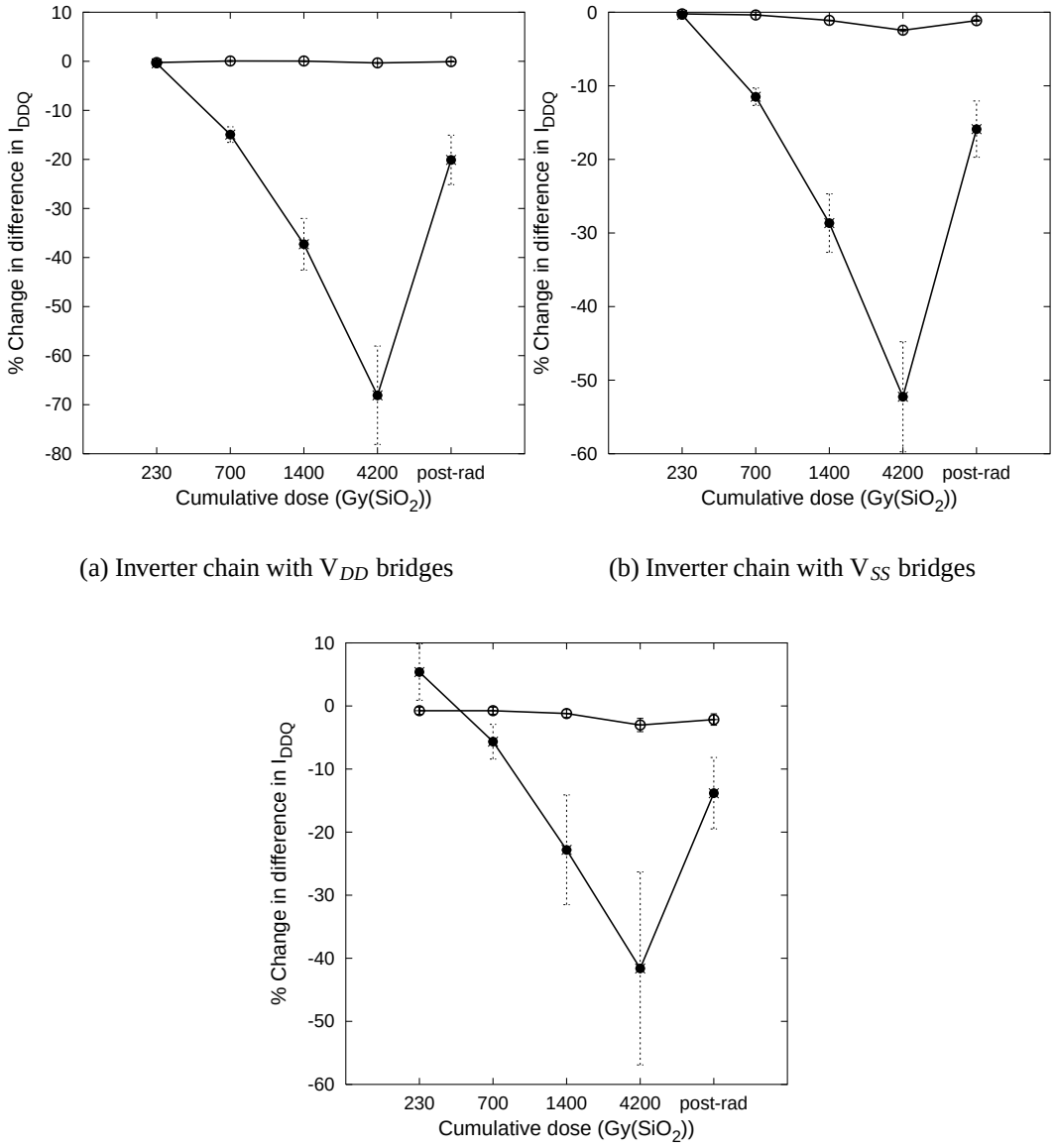
(a) Defect-free inverter chain

(b) Inverter chain with V_{DD} bridges

(c) Inverter chain with V_{SS} bridges

(d) Inverter chain with input/output bridges

Figure 5.13: Changes, as a percentage of the pre-irradiation values, in I_{DDQ} of inverter chains (a) with no defects, (b) with V_{DD} bridges, (c) with V_{SS} bridges, and (d) with input/output bridges computed for each irradiation period.



(a) Inverter chain with V_{DD} bridges

(b) Inverter chain with V_{SS} bridges

(c) Inverter chain with input/output bridges

Figure 5.14: Changes, as a percentage of the pre-irradiation values, in the difference between I_{DDQ} of inverter chains with no defects and (a) inverter chains with V_{DD} bridges, (b) with V_{SS} bridges, and (c) with input/output bridges computed for each irradiation period.

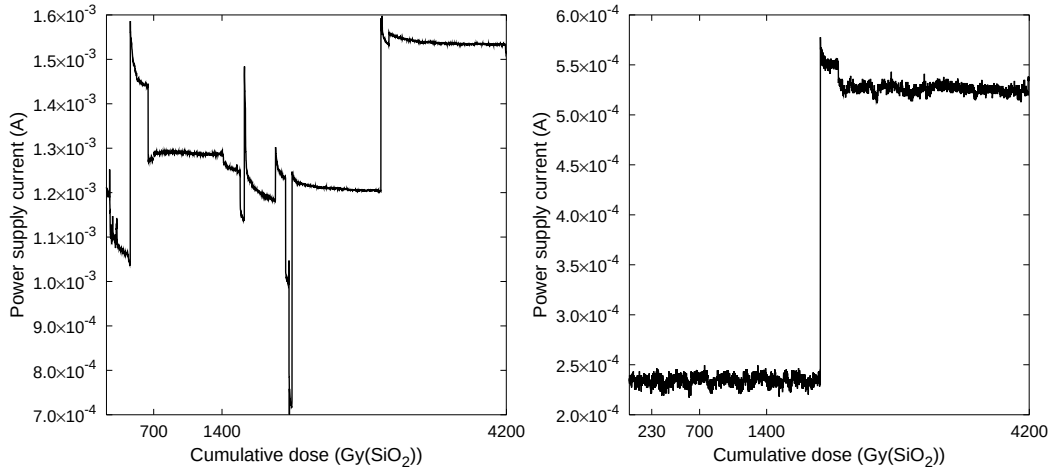
5.4.2 Transistors

Curves showing power supply current versus time for sample NMOS and PMOS transistors obtained during irradiation are shown in Figure 5.15. This current is the gate current measured with the gate biased at V_{DD} and all other transistor terminals biased at V_{SS} for NMOS transistors, and the gate biased at V_{SS} and all other transistor terminals biased at V_{DD} for PMOS transistors. These values were measured once per second during irradiation.

5.4.2.1 NMOS Transistors

One high I_G NMOS transistor and one low I_G NMOS transistor were irradiated to high doses. Figure 5.16 shows curves obtained from these two transistors before irradiation and after each irradiation period. Figure 5.16(a) and (b) show a logarithmic I_S versus V_G curve obtained by biasing the low I_G NMOS transistor in transistor biasing scheme (c) with V_S = 1.8 V, and an I_S versus V_S curve obtained by biasing the low I_G NMOS transistor in transistor biasing scheme (d) with V_G = 0.9 V, respectively. For this low I_G NMOS transistor, terminal NF is the source. Figure 5.16(c) and (d) show a logarithmic I_D versus V_G curve of the high I_G NMOS transistor with V_D = 1.8 V, and an I_D versus V_D curve of the high I_G NMOS transistor with V_G = 0.9 V, respectively. For this high I_G NMOS transistor, terminal NF is the drain.

It can be seen in (a) that the subthreshold current of the low I_G NMOS transistor increases by more than 5 orders of magnitude from before radiation to after irra-



(a) NMOS transistor

(b) PMOS transistor

Figure 5.15: Power supply current of a sample (a) NMOS transistor and (b) PMOS transistor measured during irradiation.

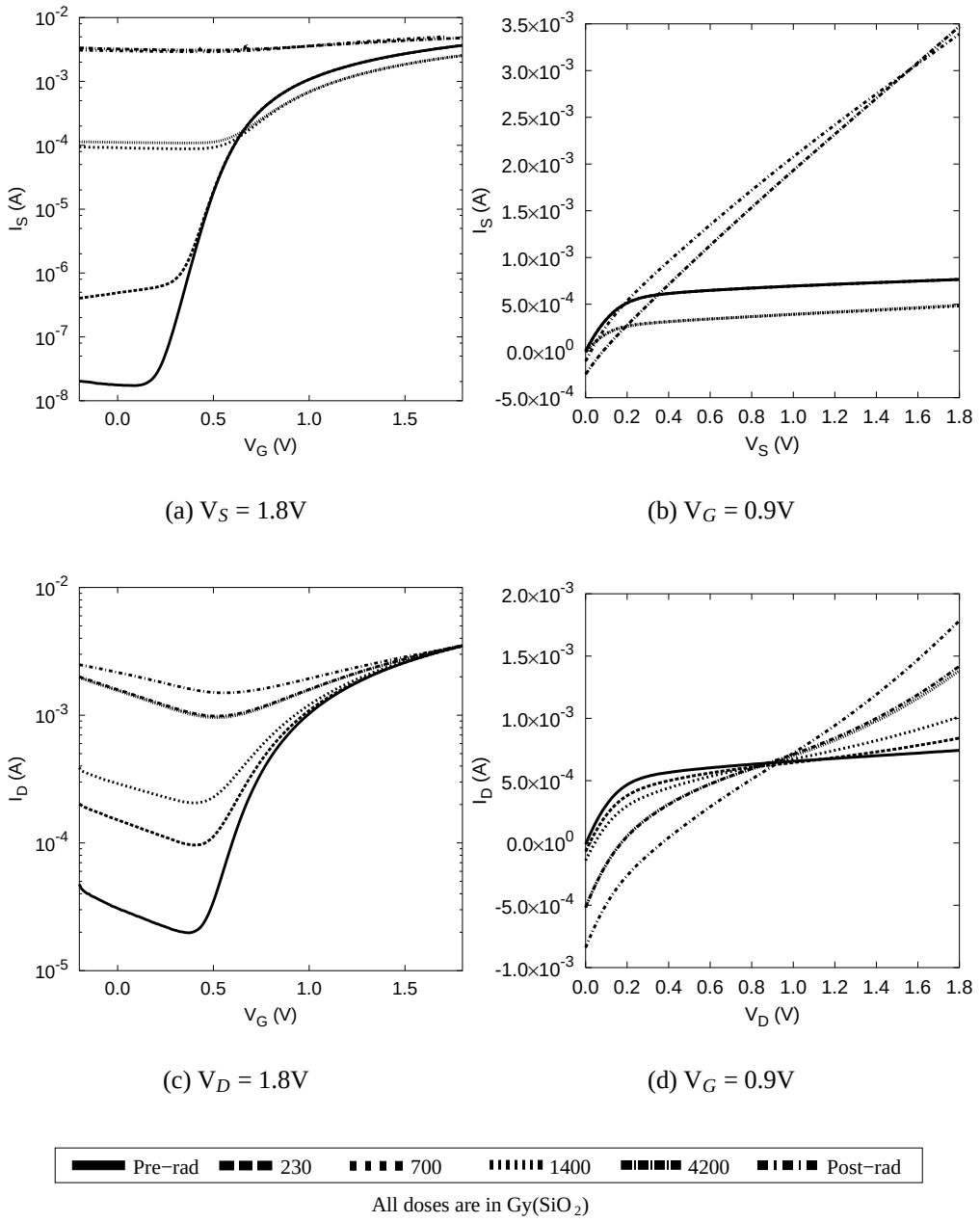


Figure 5.16: (a) I_S versus V_G and (b) I_S versus V_S curves of a low I_G NMOS transistor, and (c) I_D versus V_G and (d) I_D versus V_D curves of a high I_G NMOS transistor, measured before irradiation and after each irradiation period.

diation is complete. The plot in (a) shows a decrease in slope in the subthreshold region, but no apparent leftward shift of the curve in the subthreshold region, which would be caused by a negative threshold voltage shift. This is consistent with what we would expect, as stated in Section 3.4, for a deep-submicron NMOS transistor

whose gate oxide is too thin to enable a significant threshold voltage shift. We see a similar increase in subthreshold current for the high I_G NMOS transistor in (c). The current in (c) is much higher than in (a) due to the contribution of the current flowing from the source to the gate through the gate oxide short.

Of particular interest is the behaviour shown in the I_D versus V_D plot of the high I_G NMOS transistor shown in (d). If we were to draw a straight line between the values of I_D for V_D = 0 and 1.8 V, we would see that the slope of this line increases with each irradiation period. Note that the curves measured at each irradiation period all intersect at approximately V_D = 0.9 V, which is the value of V_G at which these curves were obtained. The I_S versus V_S plot of the low I_G NMOS transistor shown in (b) experiences a small decrease (but maintains the same shape) after an absorbed dose of 1400 Gy(SiO_2), and then increases after irradiation is complete, but does not exhibit the same behaviour seen in (d). We inferred that this behaviour is due to an increase in the current flowing between the drain and gate through the gate oxide short of the high I_G NMOS transistor. Note that after each irradiation period, a decrease in I_D is observed for $V_D < V_G$ and an increase in I_D is observed for $V_D > V_G$. Figure 5.17 shows I_G versus V_D curves of the high I_G NMOS transistor, with V_G also set at 0.9 V. Note that this plot closely resembles the inverse of the plot shown in Figure 5.16(d). In Figure 5.17, we clearly see that no current flows through the gate when $V_D = V_G$ (which is 0.9 V), and that the current, flowing out of the gate when $V_D < V_G$ and into the gate when $V_D > V_G$, increases with exposure to radiation. One could say that the "resistance" of the gate oxide short decreases with increasing doses of radiation. This confirms that the behaviour seen in Figure 5.16(d) is due to a change in the current flowing between the gate and drain. This behaviour implies that the use of radiation could be beneficial for the detection of gate oxide shorts using I_{DDQ} testing, since the current level that reveals the presence of the gate oxide short increases with exposure to radiation.

As previously mentioned, a dose of radiation must not adversely affect non-defective transistors in order to be of use to I_{DDQ} testing. In order to determine the effects of the high doses on a non-defective NMOS transistor, the I_{NF} of the low I_G NMOS transistor biased as it would be in an inverter with $V_{in} = V_{DD}$ and V_{SS} was measured after each irradiation period. The plot in Figure 5.18 shows the percent change in this current after each irradiation period. As can be seen in this plot, I_{NF} measured for an inverter input of both V_{DD} and V_{SS} increase dramatically after each irradiation period. This indicates that the high doses are too high to be of use for I_{DDQ} testing.

Nonetheless, since we have seen that the current through a gate oxide short increases with dose, we wanted to see if the high doses induced an increase in the difference between I_F of the high I_G NMOS transistor biased in the high I_G inverter biasing conditions and the I_{NF} of the low I_G NMOS transistor biased in the low I_G inverter biasing conditions. Again, this difference determines the margin of separation between the defect-free and defective portions of the I_{DDQ} distribution

of a given lot of ICs, and thus must be increased if the application of radiation is to benefit I_{DDQ} testing. The plot in Figure 5.19 shows the percent change in this difference after each irradiation period. As can be seen in the plot, the percent change in this difference increases by up to 3 orders of magnitude, indicating that, despite the increase in non-defective transistor current, radiation could aid in the detection of gate oxide shorts.

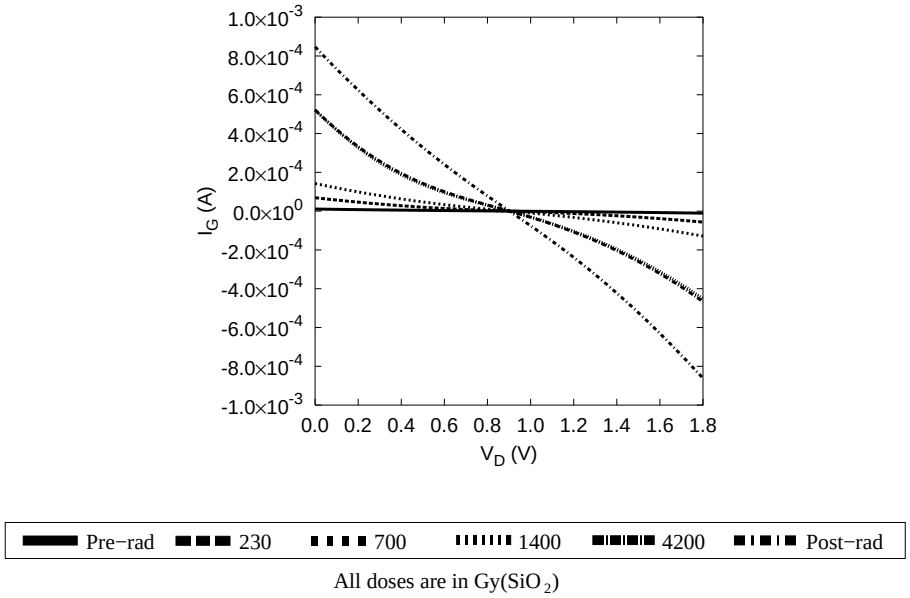


Figure 5.17: I_G versus V_D curves of a high I_G NMOS transistor for V_G = 0.9 V, measured before irradiation and after each irradiation period.

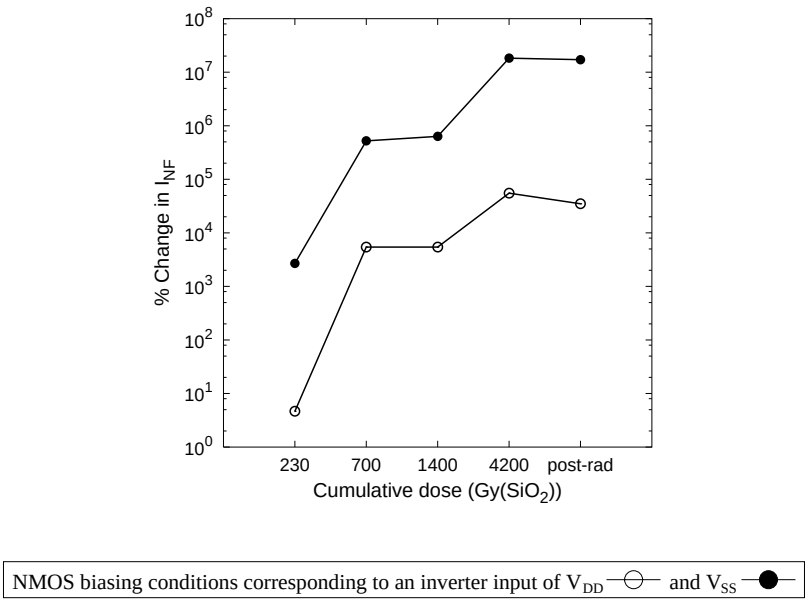


Figure 5.18: Changes, as a percentage of the pre-irradiation values, of the I_{NF} of a low I_G NMOS transistor biased as it would be in an inverter with V_{in} = V_{DD} and V_{SS}, computed for each irradiation period.

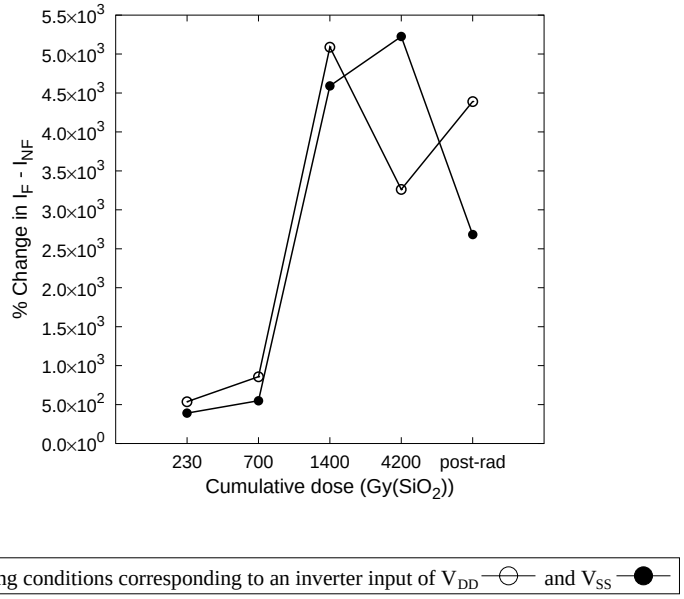


Figure 5.19: Changes, as a percentage of the pre-irradiation values, in the difference between I_F of a high I_G NMOS transistor and I_{NF} of a low I_G NMOS transistor, computed for each irradiation period.

5.4.2.2 PMOS Transistors

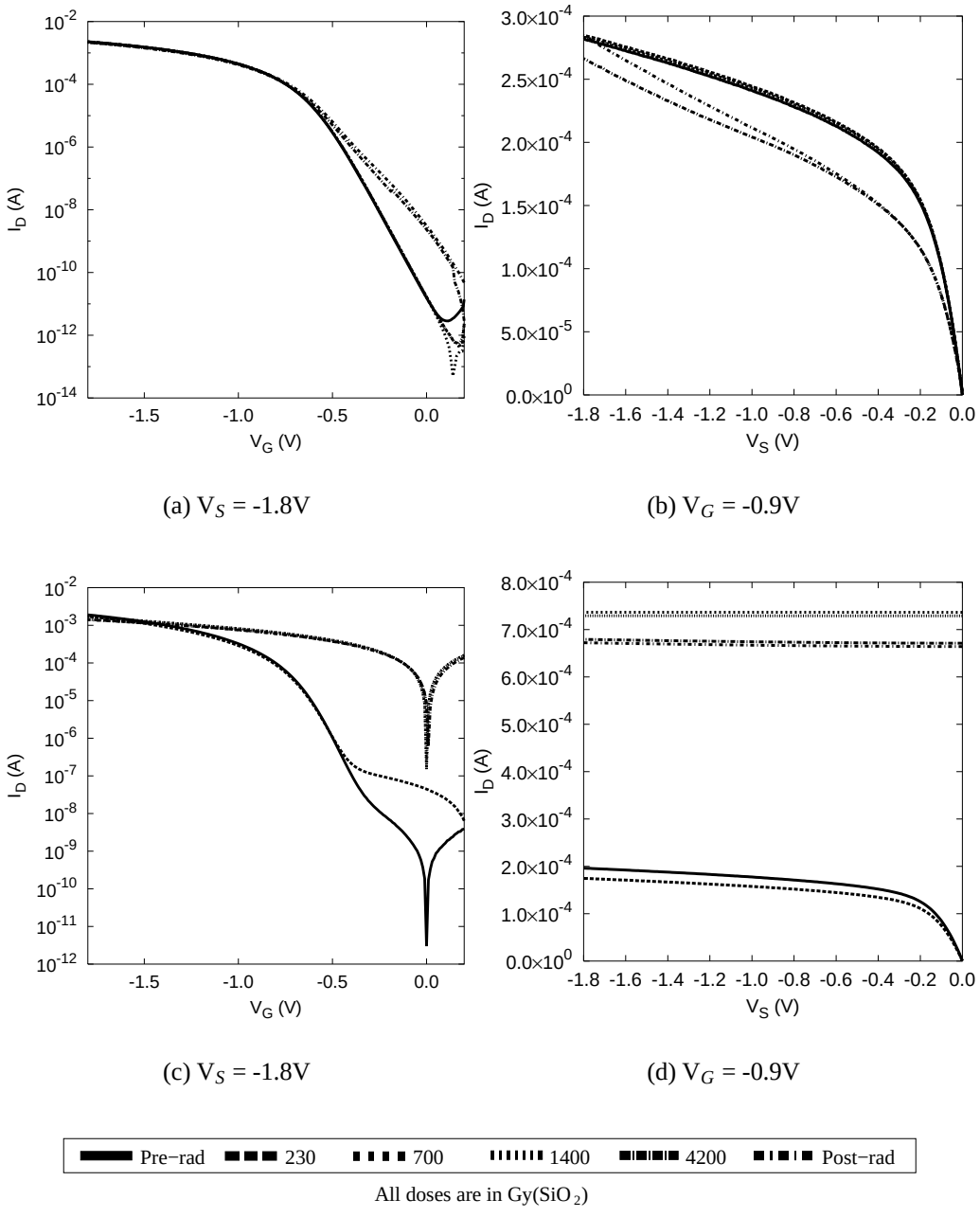
One high I_G PMOS transistor and one low I_G PMOS transistor were also irradiated to high doses. Figure 5.20 shows curves obtained from these two transistors before irradiation and after each irradiation period. Figure 5.20(a) and (b) show a logarithmic I_D versus V_G curve of the low I_G PMOS transistor with V_S = 1.8 V, and an I_D versus V_S curve of the low I_G PMOS transistor with V_G = -0.9 V, respectively. For this low I_G PMOS transistor, terminal NF is the drain. Figure 5.20(c) and (d) show a logarithmic I_D versus V_G curve of the high I_G PMOS transistor with V_S = 1.8 V, and an I_D versus V_S curve of the high I_G PMOS transistor with V_G = -0.9 V, respectively. For this high I_G PMOS transistor, terminal F is the drain.

It can be seen in (a) that the subthreshold current of the low I_G PMOS transistor does not undergo a noticeable increase after an absorbed dose of 1400 Gy(SiO_2). An increase is only seen after irradiation is complete. This is consistent with the high radiation tolerance that we would expect, as stated in Section 3.4, for a deep-submicron PMOS transistor. We see a greater increase in subthreshold current for the high I_G PMOS transistor in (c), which, as we will again show, can be attributed to the contribution of the current flowing from drain to gate through the gate oxide short.

Of interest, again, is the behaviour shown in the plot for the high I_G PMOS transistor shown in (d). After an absorbed dose of 230 Gy(SiO_2), the I_D curve increases and its shape changes from that of the pre-irradiation curve, becoming flat. Figure 5.21 shows the I_G versus V_D curves of the high I_G PMOS transistor with V_G also set to -0.9 V. As was the case in the high I_G NMOS transistor, the shape of this plot closely resembles the inverse of the plot in Figure 5.20(d). However, unlike the plot of the high I_G NMOS transistor, shown in Figure 5.17, the value of I_G after each irradiation period in Figure 5.21 remains constant regardless of the magnitude of the voltage difference between gate and source. This difference in behaviour could be the result of a difference in the physical nature of the gate oxide shorts in the high I_G NMOS and PMOS transistors. Nonetheless, Figure 5.21 shows that the current flowing through the gate oxide short increases with increased absorbed dose. This behaviour again implies that the use of radiation could be beneficial for the detection of gate oxide shorts using I_{DDQ} testing, since the current level that reveals the presence of the gate oxide short increases with exposure to radiation.

In order to determine the effect of the high doses on a non-defective PMOS transistor, I_{NF} of the low I_G PMOS transistor, biased as it would be in an inverter with $V_{in} = V_{DD}$ and V_{SS}, was measured after each irradiation period. The percent change of this current after each irradiation period is shown in Figure 5.22. As was the case with the high I_G NMOS transistor, we again see large increases, indicating that the high doses are too high to be of use for I_{DDQ} testing.

To see if the high doses induced an increase in the differences between I_F of the high I_G PMOS transistor biased in the high I_G inverter biasing conditions and the



(a) V_S = -1.8V

(b) V_G = -0.9V

(c) V_S = -1.8V

(d) V_G = -0.9V

Figure 5.20: (a) I_D versus V_G and (b) I_D versus V_S curves of a low I_G PMOS transistor, and (c) I_D versus V_G and (d) I_D versus V_S curves of a high I_G PMOS transistor, measured before irradiation and after each irradiation period.

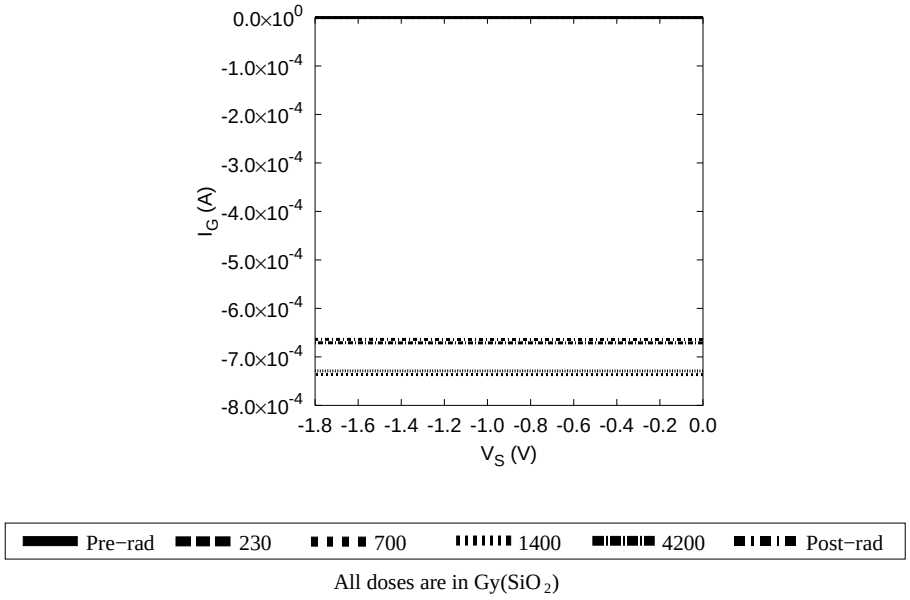


Figure 5.21: I_G versus V_S curves of a high I_G PMOS transistor for V_G = -0.9 V measured before irradiation and after each irradiation period.

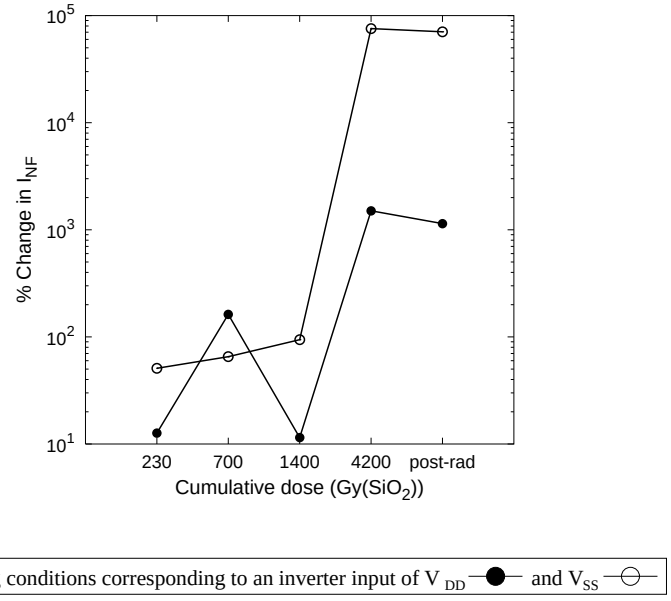


Figure 5.22: Changes, as a percentage of the pre-irradiation values, of I_{NF} of a low I_G PMOS transistor biased as it would be in an inverter with $V_{in} = V_{DD}$ and V_{SS}, computed after each irradiation period.

I_{NF} of the low I_G PMOS transistor biased in the low I_G inverter biasing conditions, the percent changes in these differences were determined after each irradiation period. These are plotted in Figure 5.23. As can be seen in the plot, the percent change in this difference increases up to approximately 5 orders of magnitude, indicating that, despite the increase in non-defective transistor current, radiation can aid in the detection of gate oxide shorts.

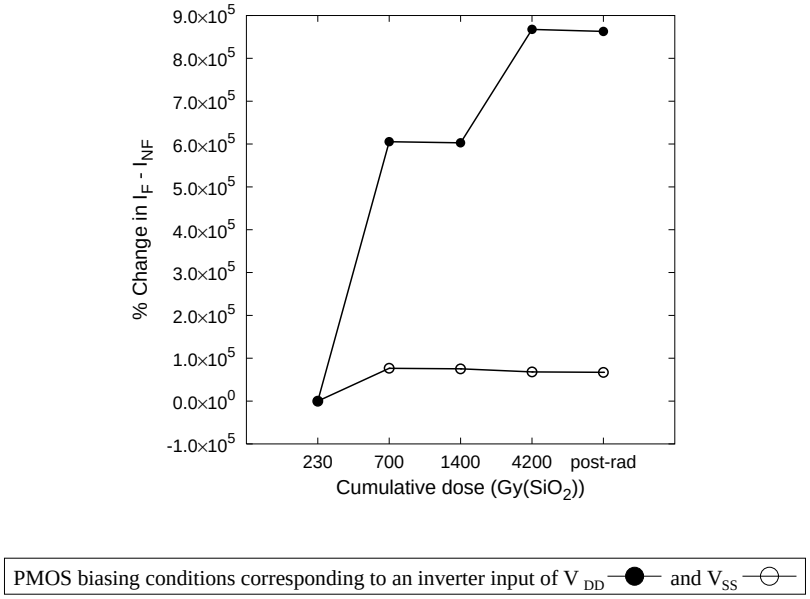


Figure 5.23: Changes, as a percentage of the pre-irradiation values, in the difference between I_F of a high I_G PMOS transistor and I_{NF} of a low I_G PMOS transistor, computed after each irradiation period.

5.5 Exposure To Low Doses

As evidenced by Figures 5.11, 5.18, and 5.22, the high doses caused an undesirable increase in the current of non-defective transistors. We therefore wanted to use lower doses that would not cause such increases. If such a dose could still cause an increase in the difference between the currents of defective and non-defective circuits, the ideal scenario as stated in Section 4.1, would be achieved.

Figures 5.11(a) and 5.16(a) show increases in current after an absorbed dose of 230 Gy(SiO_2). We therefore wanted to use a total cumulative dose less than this. However, the x-ray accelerator used in this experiment was prone to suddenly ceasing operation during irradiation and it was feared that this might cause unpredictable fluctuation in doses if very short irradiation times (such as 30 seconds) were used. Therefore, the count rate, and hence the dose rate, of the x-ray accelerator was low-

ered in order to allow for reasonable irradiation times and still allow for low doses. This was done by lowering the tube current of the x-ray machine. It was decided that lowering the count rate by a factor of 4 would be sufficient. Test runs were then done and it was found that lowering the tube current to 3 mA decreased the count rate by approximately 4 times. The temperature and atmospheric pressure during irradiations with this lower dose rate were measured to be 24°C and 767.08 mmHg respectively. The count rate at this tube current was recorded as 6.58 counts/s and the dose rate was computed to be 0.214 Gy(SiO_2)/s. This dose rate will herein be referred to as the *low dose rate*. The cumulative exposure times and doses used at this low dose rate are listed in Table 5.2. These doses will herein be referred to as *low doses*. The cumulative exposure times will be again be used when referring to the total amount of radiation a test circuit was exposed to prior to making a set measurements.

Cumulative Exposure Times (min)	Cumulative Doses (Gy(SiO_2))
1	12
3	38
6	77
10	130

Table 5.2: Cumulative exposure times and doses using low dose rate.

As previously mentioned, it is desirable that any beneficial effects of radiation occur without biasing during irradiation, since biasing requires additional power consumption. Therefore, during irradiations to low doses, no biasing was applied in order to determine whether beneficial effects could still be obtained. The pins of all test circuits were shorted together to ensure that no differences in potential occurred between any circuit terminals. The effects of the low doses on the test circuits are presented and analyzed here. We again examine the effects of these doses on the differences between defective and non-defective currents described in Sections 5.1 and 5.2.2.

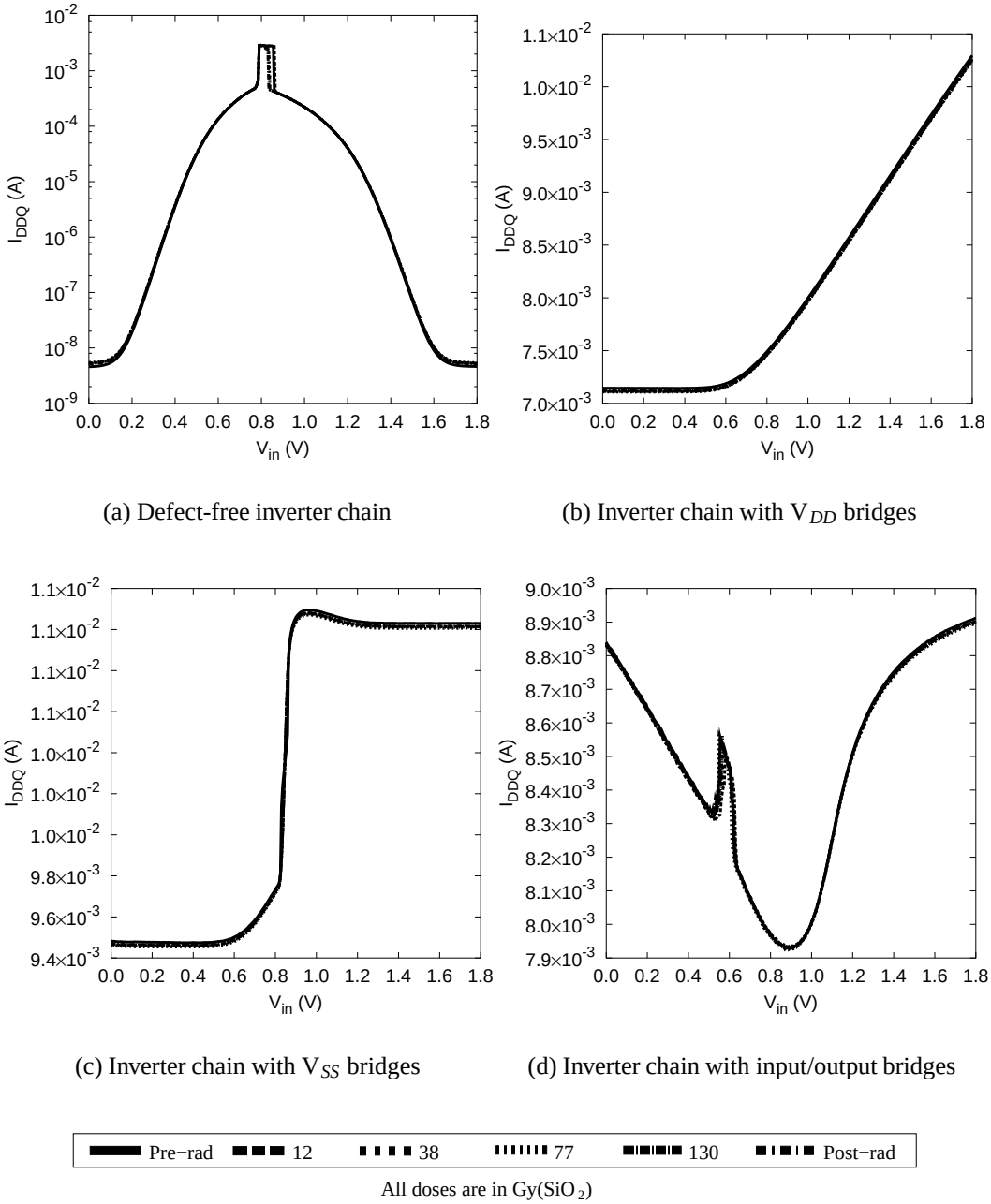
5.5.1 Inverter Chains

Plots of I_{DDQ} versus V_{in} curves for sample inverter chains with no defects, with V_{DD} bridges, with V_{SS} bridges, with input/output bridges, with NMOS stuck-on defects, and with PMOS stuck-on defects, measured before irradiation and after each irradiation period, are shown in Figures 5.24 and 5.25. As can be seen in these plots, the low doses have a much smaller effect on the I_{DDQ} of all inverter chains than the high doses. The lack of an increase in the I_{DDQ} of the defect-free inverter chain indicates that the low doses do not elevate the currents of defect-free transistors.

Plots of V_{out} versus V_{in} curves for all inverter chain types, measured before irradiation and after each irradiation period, are shown in Figures 5.26 and 5.27. Note that the low doses also have a noticeably smaller effect on the logical behaviour of the inverter chains with V_{DD} bridges, with V_{SS} bridges, and with input/output bridges than the high doses.

The percent change in the I_{DDQ} of 4 instances of each inverter chain type was calculated for $V_{in} = V_{DD}$ and V_{SS} for each irradiation period. Figures 5.28 and 5.29 show the means of these values, calculated over the 4 instances of each inverter chain type, as well as the standard error, indicated by the errorbars. As can be seen from these figures, the increase in I_{DDQ} of the defect-free inverter chain is far less than that induced by the high doses, but still increases by a greater amount than the I_{DDQ} of the defective inverter chain types.

The percent change in the difference between the I_{DDQ} of each defective inverter chain type and the defect-free inverter chain, after each irradiation period, for $V_{in} = V_{DD}$ and V_{SS}, is shown in Figures 5.30 and 5.31. This was again calculated for 4 instances of each inverter chain type irradiated to low doses, where the I_{DDQ} of the first instance of each of the defective inverter chain types was subtracted from the first instance of the defect-free inverter chain, the I_{DDQ} of the second instance of each of the defective inverter chain types was subtracted from the second instance of the defect-free inverter chain, etc. The mean and standard error of these 4 differences (one for each instance) was then calculated for each defective inverter chain type. The figures show the mean values of these differences and the standard errors, indicated by the errorbars. As can be seen, this difference for each of the defective inverter chain types remains relatively constant for $V_{in} = V_{DD}$ and V_{SS}, indicating that the low doses would not aid in differentiating the I_{DDQ} of these defective and non-defective inverter chains.



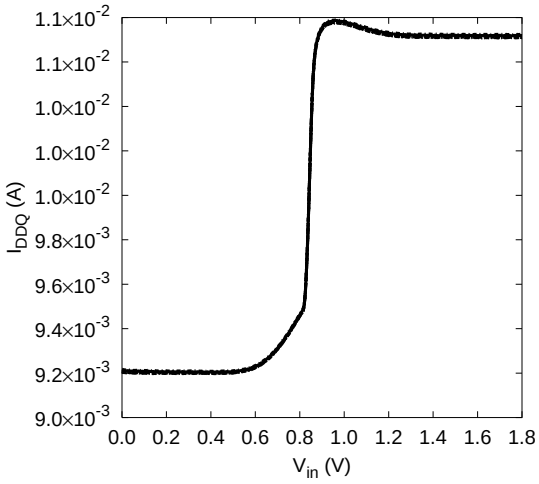
(a) Defect-free inverter chain

(b) Inverter chain with V_{DD} bridges

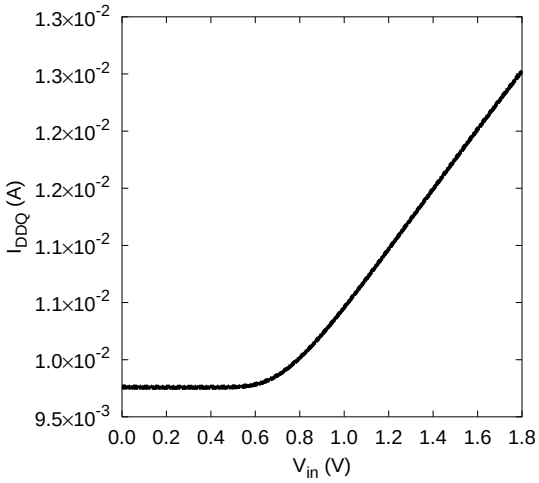
(c) Inverter chain with V_{SS} bridges

(d) Inverter chain with input/output bridges

Figure 5.24: I_{DDQ} versus V_{in} curves of sample inverter chains (a) with no defects, (b) with V_{DD} bridges, (c) with V_{SS} bridges, and (d) with input/output bridges measured before irradiation and after each irradiation period.



(a) Inverter chain with NMOS stuck-on defects



(b) Inverter chain with PMOS stuck-on defects

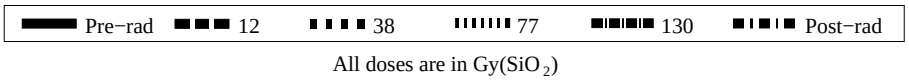
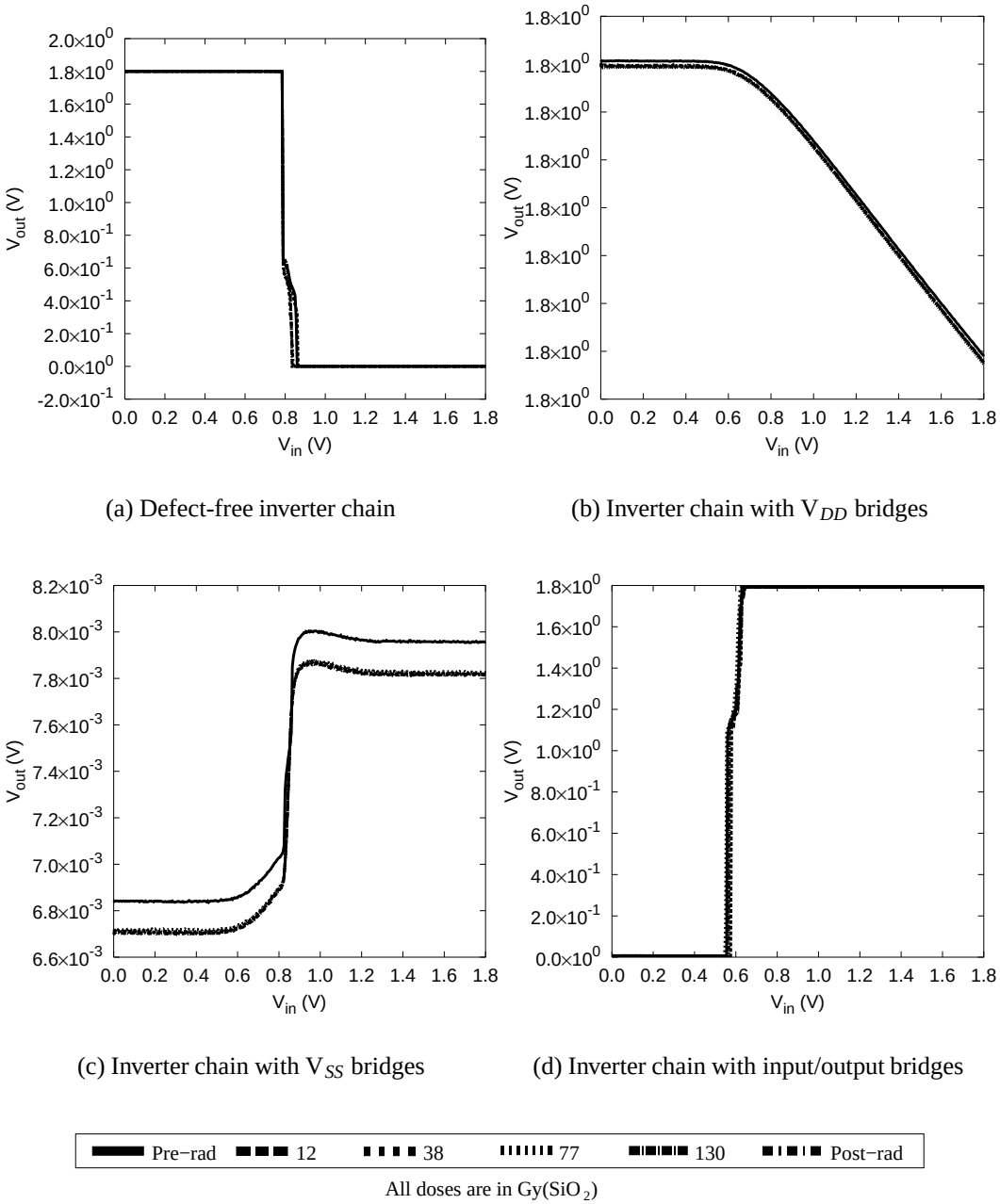


Figure 5.25: I_{DDQ} versus V_{in} curves of sample inverter chains (a) with NMOS stuck-on defects and (b) with PMOS stuck-on defects measured before irradiation and after each irradiation period.



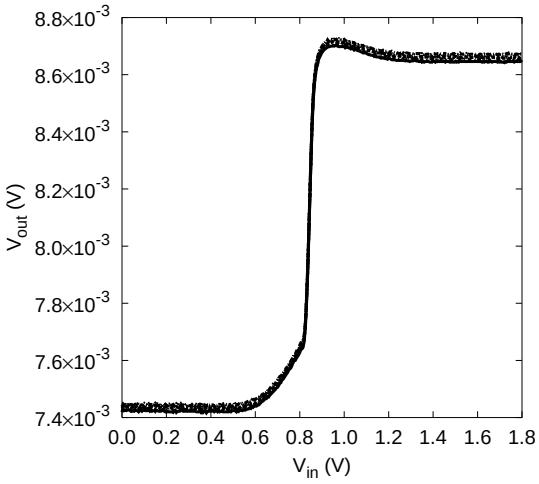
(a) Defect-free inverter chain

(b) Inverter chain with V_{DD} bridges

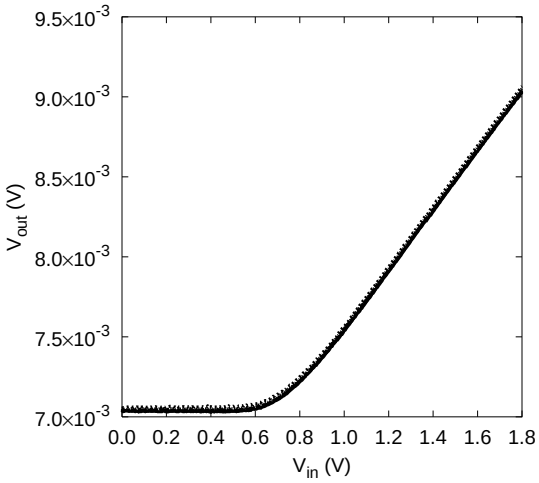
(c) Inverter chain with V_{SS} bridges

(d) Inverter chain with input/output bridges

Figure 5.26: V_{out} versus V_{in} curves of sample inverter chains (a) with no defects, (b) with V_{DD} bridges, (c) with V_{SS} bridges, and (d) with input/output bridges measured after each irradiation period.



(a) Inverter chain with NMOS stuck-on defects



(b) Inverter chain with PMOS stuck-on defects

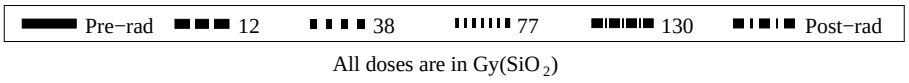
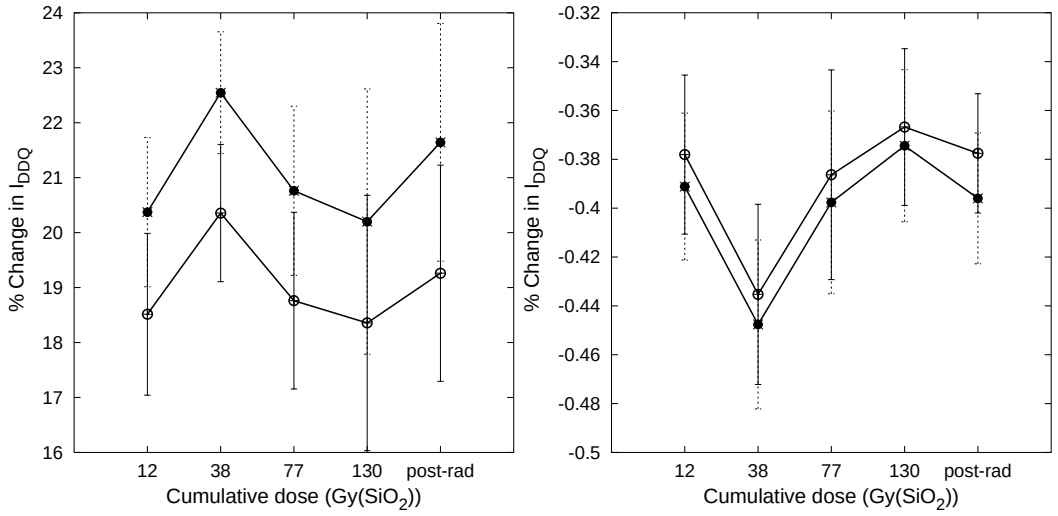
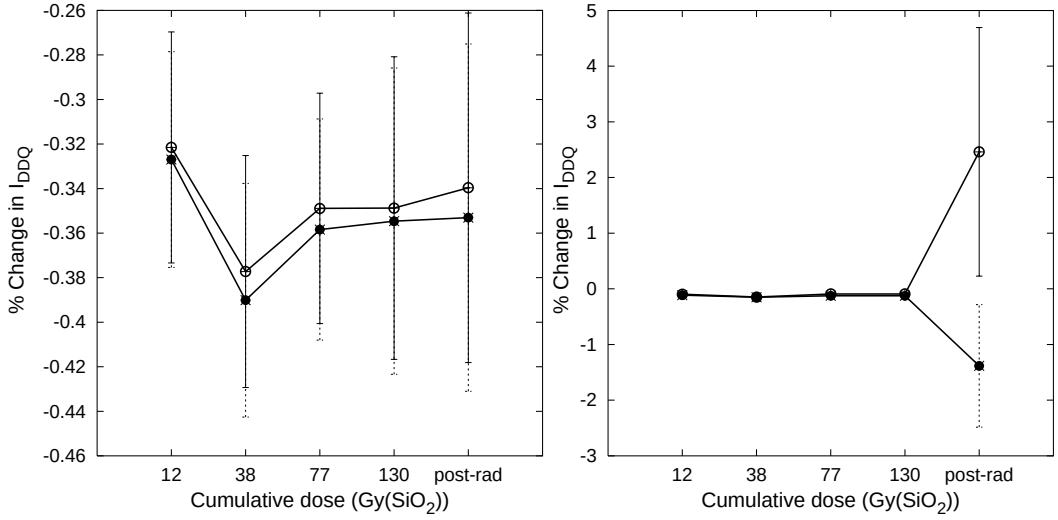


Figure 5.27: V_{out} versus V_{in} curves of sample inverter chains (a) with NMOS stuck-on defects and (b) with PMOS stuck-on defects measured after each irradiation period.



(a) Defect-free inverter chain

(b) Inverter chain with V_{DD} bridges



(c) Inverter chain with V_{SS} bridges

(d) Inverter chain with input/output bridges

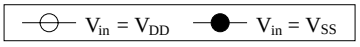
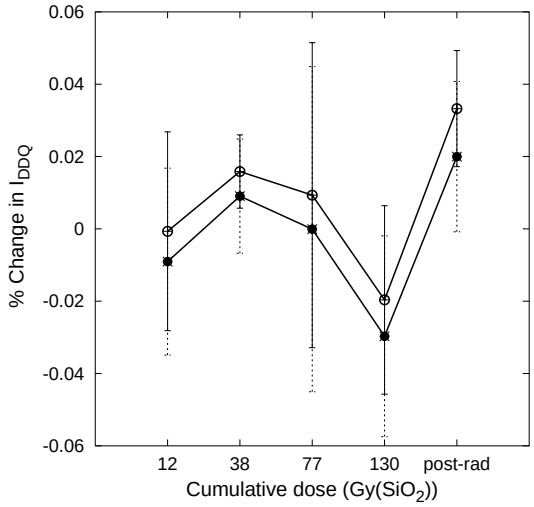
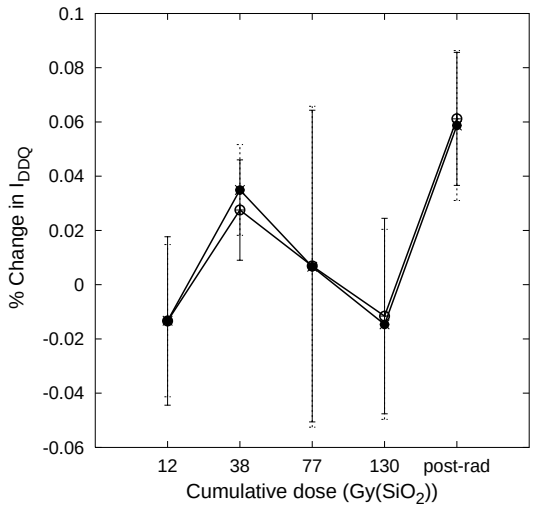


Figure 5.28: Changes, as a percentage of the pre-irradiation values, in I_{DDQ} of inverter chains (a) with no defects, (b) with V_{DD} bridges, (c) with V_{SS} bridges, and (d) with input/output bridges computed for each irradiation period.



(a) Inverter chain with NMOS stuck-on defects



(b) Inverter chain with PMOS stuck-on defects

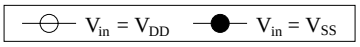
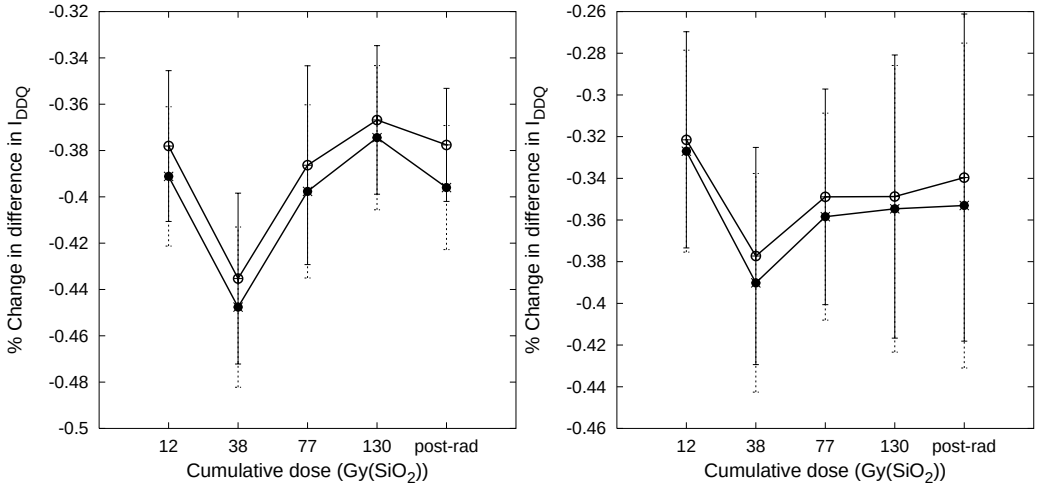
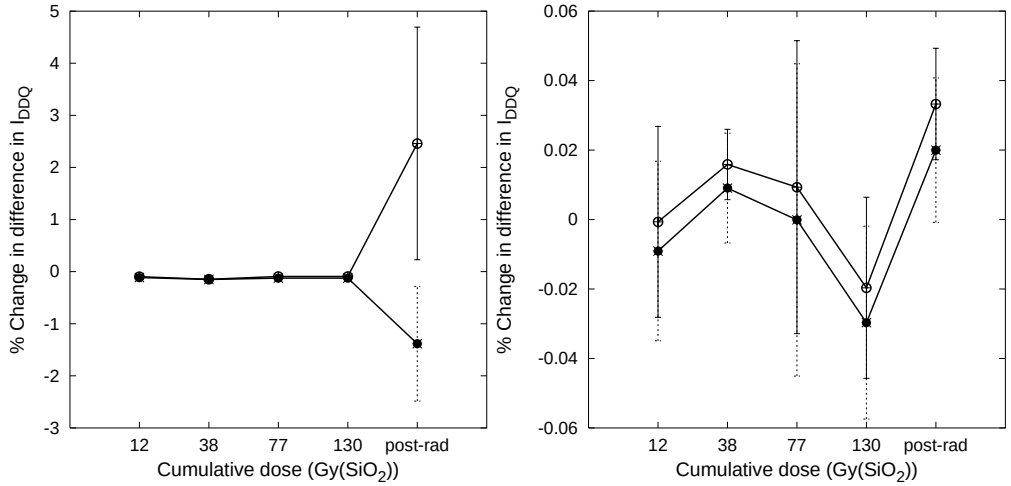


Figure 5.29: Changes, as a percentage of the pre-irradiation values, in I_{DDQ} of inverter chains (a) with NMOS stuck-on defects and (b) with PMOS stuck-on defects computed for each irradiation period.



(a) Inverter chain with V_{DD} bridges

(b) Inverter chain with V_{SS} bridges



(c) Inverter chain with input/output bridges

(d) Inverter chain with NMOS stuck-on defects

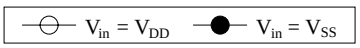


Figure 5.30: Changes, as a percentage of the pre-irradiation values, in the difference between I_{DDQ} of inverter chains with no defects and inverter chains (a) with V_{DD} bridges, (b) with V_{SS} bridges, (c) with input/output bridges, and (d) with NMOS stuck-on defects computed for each irradiation period.

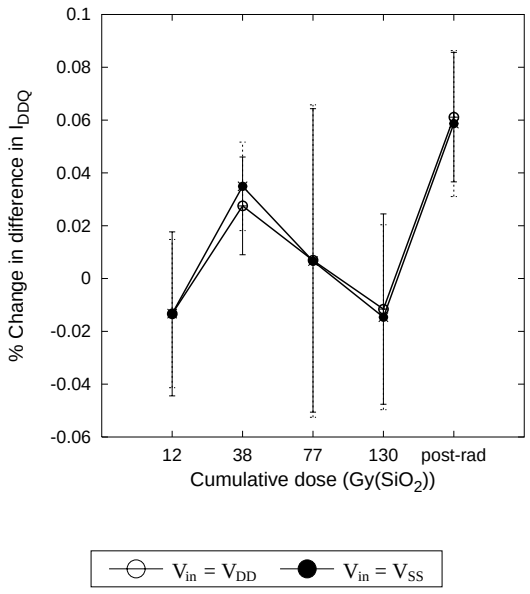


Figure 5.31: Changes, as a percentage of the pre-irradiation values, in the difference between I_{DDQ} of inverter chains with no defects and inverter chains with PMOS stuck-on defects computed for each irradiation period.

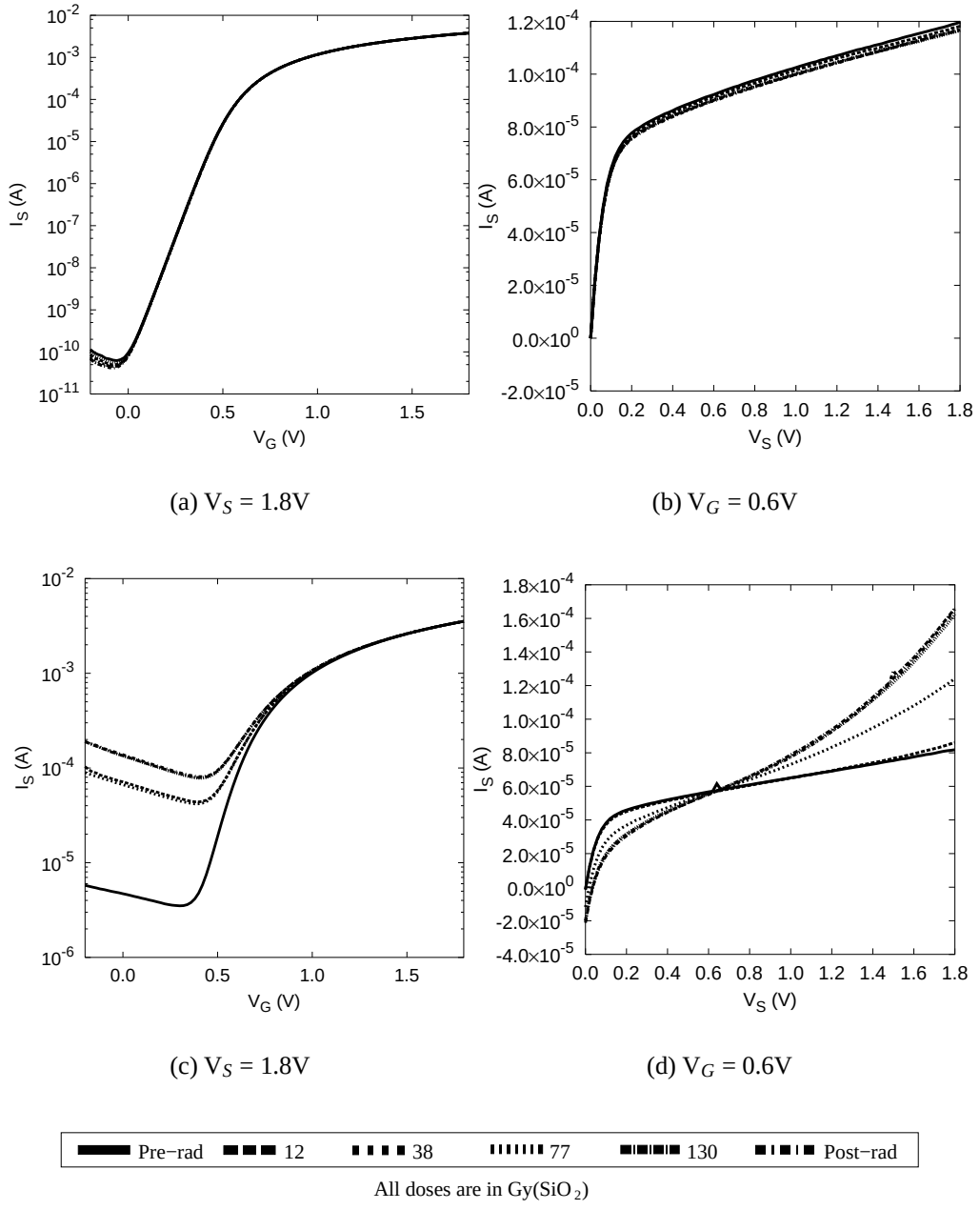
5.5.2 Transistors

5.5.2.1 NMOS Transistors

Six high I_G NMOS transistors and 4 low I_G NMOS transistors were irradiated to low doses. Figure 5.32 shows curves obtained from two of these transistors before irradiation and after each irradiation period. Figure 5.32(a) and (b) show a logarithmic I_S versus V_G curve of a sample low I_G NMOS transistor with V_S = 1.8 V, and an I_S versus V_S curve of this low I_G NMOS transistor with V_G = 0.6 V, respectively. For this low I_G NMOS transistor, terminal NF is the source. Figure 5.32(c) and (d) show a logarithmic I_S versus V_G curve of a sample high I_G NMOS transistor with V_S = 1.8 V, and an I_S versus V_S curve of this high I_G NMOS transistor with V_G = 0.6 V, respectively. For this high I_G NMOS transistor, the terminal F is the source.

It can be seen in (a) and (b) that the current of the low I_G NMOS transistor is left virtually unaffected by the low doses. These curves are noticeably different than those obtained from the low I_G NMOS transistor irradiated to high doses shown in Figure 5.16. This shows that the low doses do not adversely affect the operation of non-defective NMOS transistors.

The subthreshold current of the high I_G NMOS transistor, shown in Figure 5.32(c), shows an increase of approximately an order of magnitude. Since the subthreshold current of the low I_G NMOS transistor does not show such an increase, we can infer that the increase in the high I_G NMOS transistor is due to a radiation-



(a) V_S = 1.8V (b) V_G = 0.6V

(c) V_S = 1.8V (d) V_G = 0.6V

Figure 5.32: (a) I_S versus V_G and (b) I_S versus V_S curves of a low I_G NMOS transistor, and (c) I_S versus V_G and (d) I_S versus V_S curves of a high I_G NMOS transistor, measured before irradiaiton and after each irradiation period.

induced increase in the current flowing through its gate oxide short. This is also suggested by the behaviour of the plot shown in Figure 5.32(d), which was also previously seen in the plot of the high I_G NMOS transistor irradiated to high doses, shown in Figure 5.16(d). We again see that the slope of the imaginary straight line, drawn between the values of I_S for V_S = 0 and 1.8 V, increases with each irradiation period. The curves measured after each irradiation period again intersect at the voltage for which V_G was set to obtain these curves. Figure 5.33 shows I_G versus V_S curves obtained from the transistor biasing scheme used to obtain the plot shown in Figure 5.32(d), with V_G also set at 0.6 V. Again, note that this plot closely resembles the inverse of the plot shown in Figure 5.32(d). This confirms that the behaviour seen in Figure 5.32(d) is due to a change in the current flowing between the gate and source. In 5.33, we clearly see that no current flows through the gate when $V_S = V_G$ (which is 0.6 V), and that the current, flowing out of the gate when $V_S < V_G$ and into the gate when $V_S > V_G$, increases with exposure to radiation. This behaviour again shows a decrease in the "resistance" of the gate oxide short, and implies that the use of radiation could be beneficial for the detection of gate oxide shorts using I_{DDQ} testing, since the current level that reveals the presence of the gate oxide short increases with exposure to radiation. This result, obtained when irradiating to low doses, is particularly encouraging because it suggests that a dose of radiation that does not increase the drain-source current in a defect-free transistor still increases the current flowing through a gate oxide short in a defective transistor.

The plot in Figure 5.34 shows the percent change in I_{NF} of the 4 low I_G NMOS

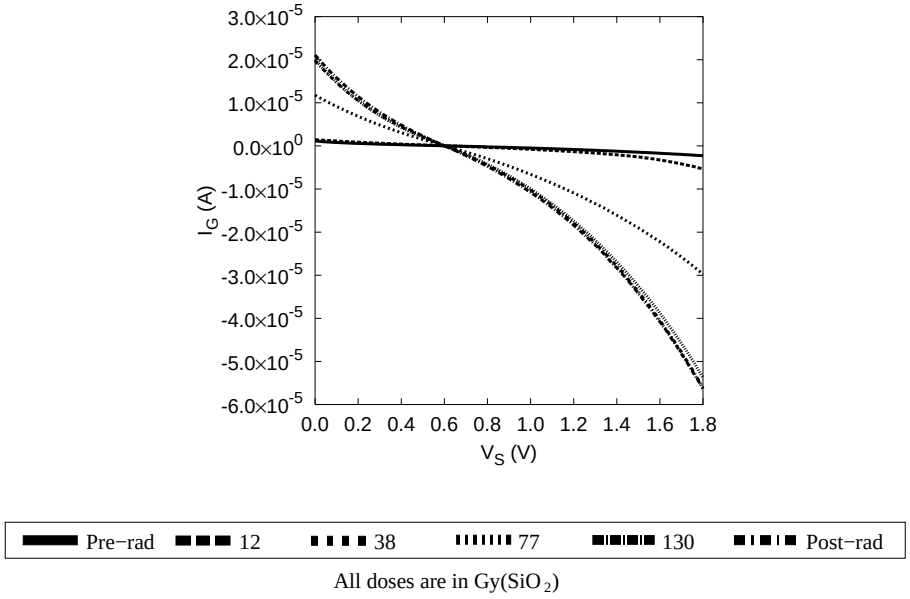


Figure 5.33: I_G versus V_S curves of a high I_G NMOS transistor for V_G = 0.6 V, measured before irradiation and after each irradiation period.

transistors biased as they would be in inverters with $V_{in} = V_{DD}$ and V_{SS}, measured after each irradiation period. The means and standard errors of these values, calculated over the 4 transistors, are shown in the plot. As can be seen in this plot, I_{NF} measured for an inverter input of both V_{DD} and V_{SS} do not show significant increases as they did with exposure to the high doses as shown in Figure 5.18. The currents measured after each irradiation period are all in fact less than the pre-irradiation values. This again suggests that the low doses do not adversely affect defect-free transistors and could thus potentially be of use for I_{DDQ} testing.

We again want to see how the difference, between I_F of the high I_G NMOS transistors biased in the high I_G inverter biasing conditions and the I_{NF} of the low I_G NMOS transistors biased in the low I_G inverter biasing conditions, changes with exposure to radiation. The percent change in this difference between each of the 6 high I_G NMOS transistors and each of the 4 low I_G NMOS transistors, irradiated to low doses, was computed. One plot has been made for each high I_G NMOS transistor, and the mean and standard error over the differences, between each high I_G NMOS transistor and each of the 4 low I_G NMOS transistors, are shown in each plot. That is, each of these plots compares one high I_G NMOS transistor with all of the low I_G NMOS transistors. These plots are found in Figures 5.35 and 5.36. As can be seen in these figures, the majority of the data indicates an increase in the current difference due to radiation, indicating that exposure to radiation to low doses can aid in distinguishing between defective and non-defective NMOS transistors. The percentages, by which this difference increases, varies widely from one high I_G NMOS transistor to the next. This is likely due to differences in the physical nature of the defects in these transistors.

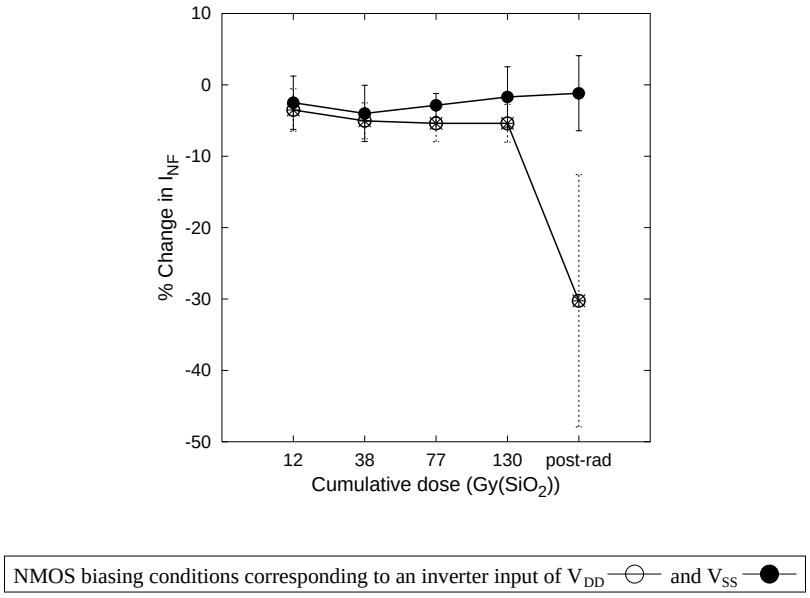


Figure 5.34: Changes, as a percentage of the pre-irradiation values, of I_{NF} of low I_G NMOS transistors biased in low I_G inverter biasing conditions (e) and (f) computed for each irradiation period.

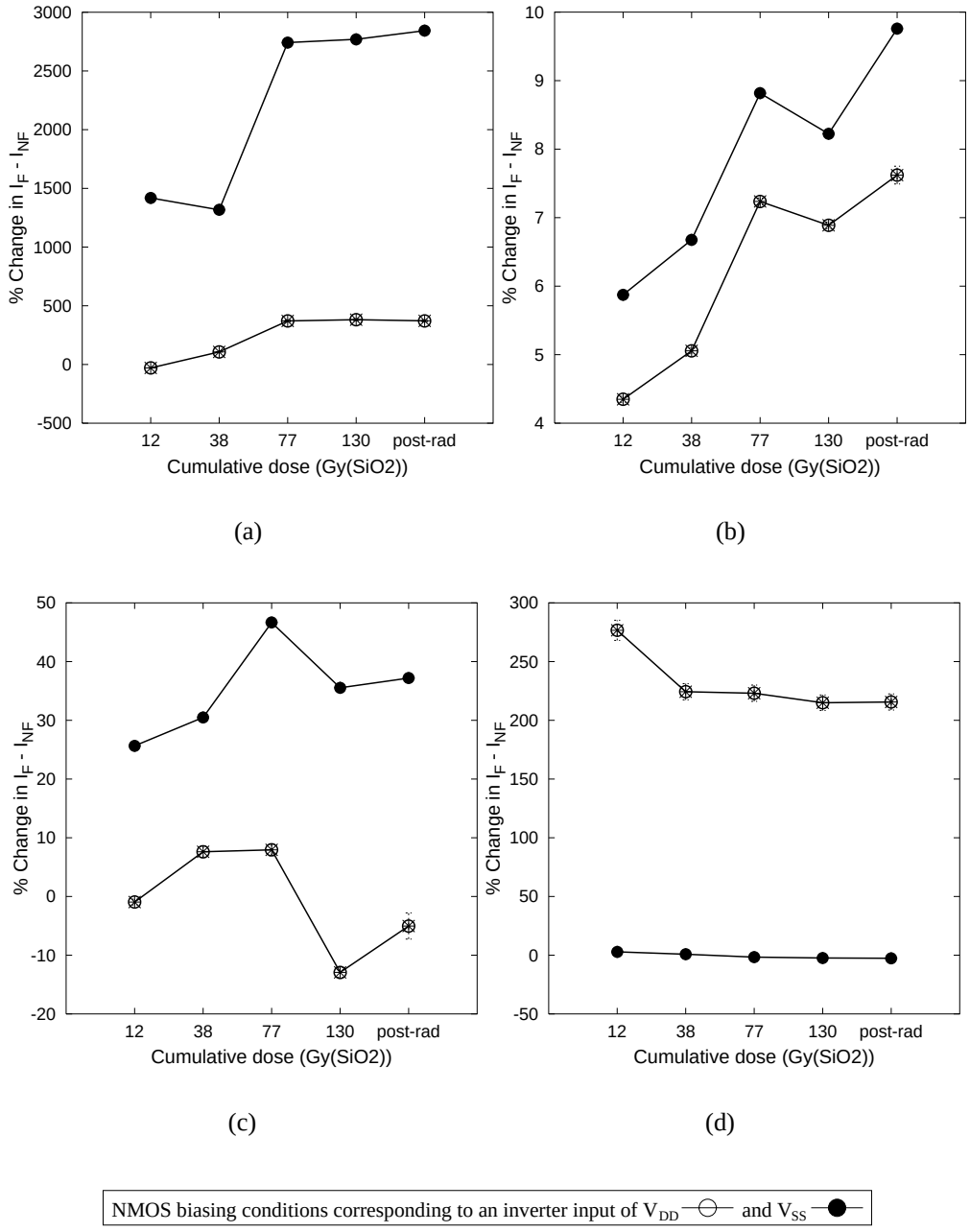


Figure 5.35: Changes, as a percentage of the pre-irradiation values, in the difference between I_F of a high I_G NMOS transistor and I_{NF} of low I_G NMOS transistors computed for each irradiation period.

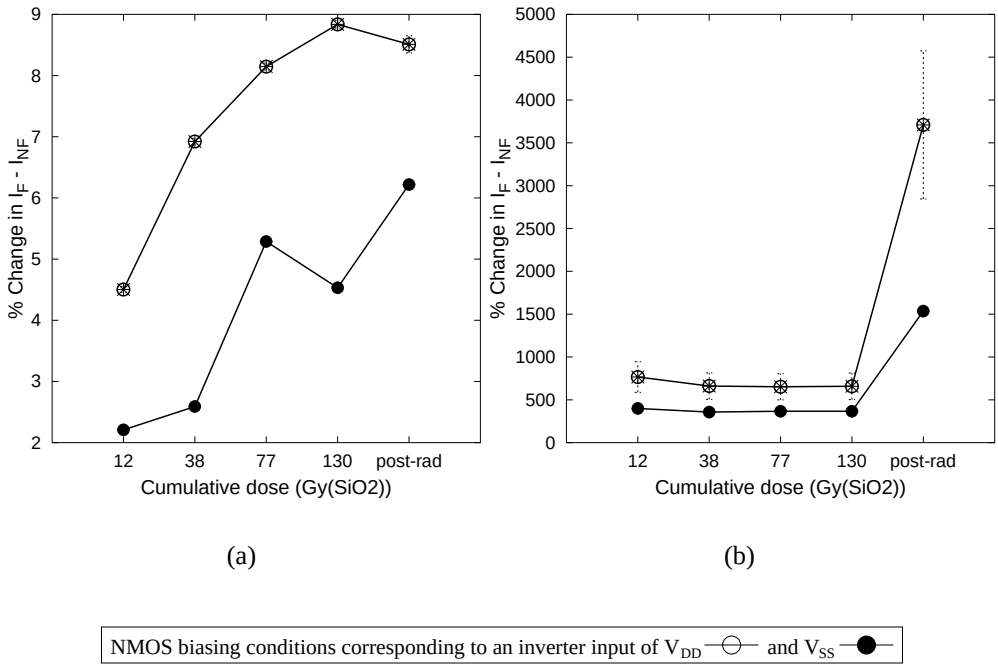


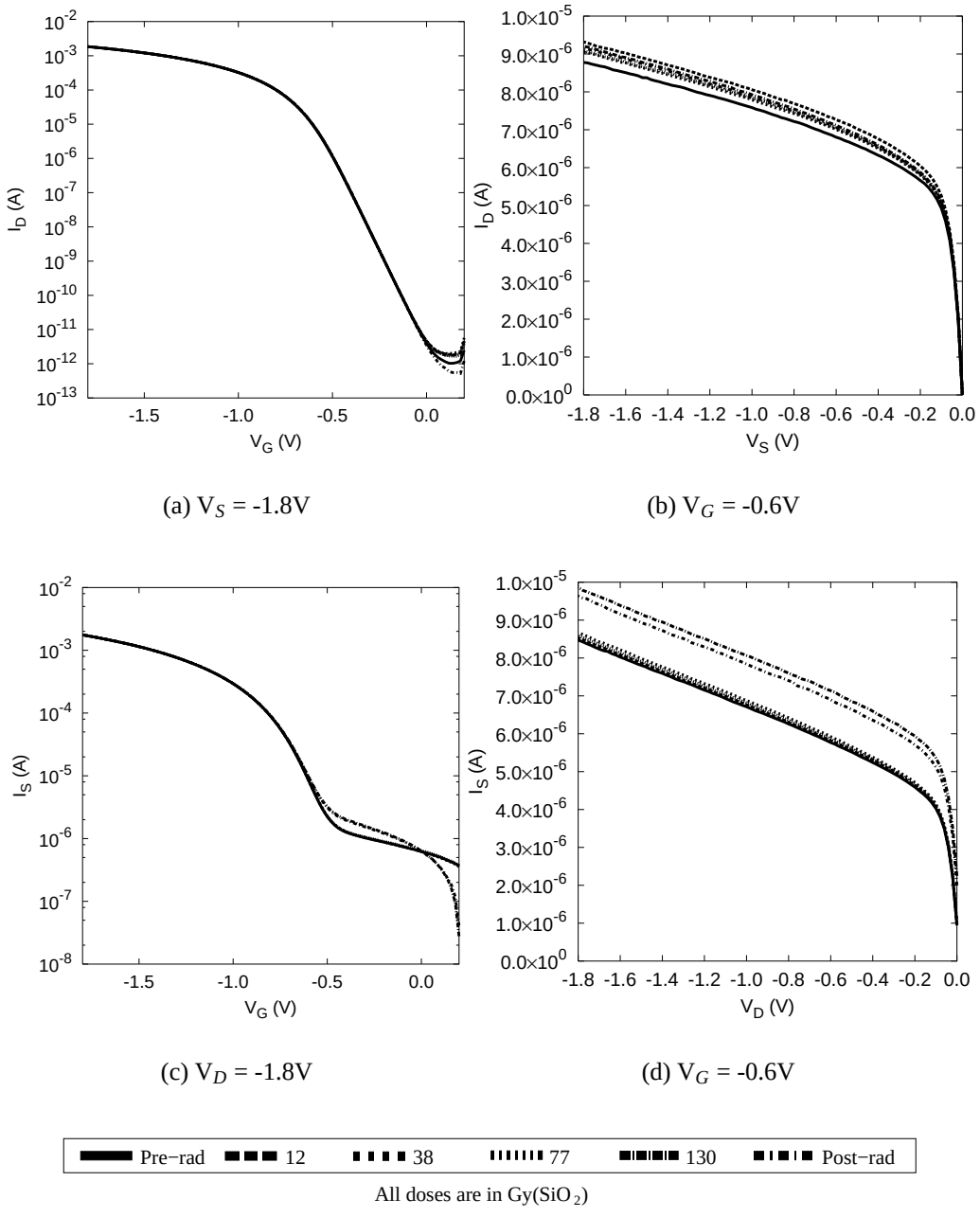
Figure 5.36: Changes, as a percentage of the pre-irradiation values, in the difference between I_F of a high I_G NMOS transistor and I_{NF} of low I_G NMOS transistors computed for each irradiation period.

5.5.2.2 PMOS Transistors

As previously mentioned in Section 5.2.1.2, of the PMOS transistors we fabricated, those with low I_G far outnumbered those with high I_G. In order to obtain more PMOS transistors with high gate current, the procedure for creating gate oxide shorts described in Section 4.3.3.3 was used to damage the gate oxide of some PMOS transistors with low gate current. Five high I_G PMOS transistors and four low I_G PMOS transistors were irradiated to low doses. Of these five high I_G PMOS transistors, four of them were damaged using the aforementioned technique.

Figure 5.37 shows curves obtained from the one high I_G PMOS transistor, on which the technique was not used, and a sample low I_G PMOS transistor, before irradiation and after each irradiation period using low doses. Figure 5.37(a) and (b) show a logarithmic I_D versus V_G curve of the low I_G PMOS transistor with V_S = 1.8 V, and an I_D versus V_S curve of the low I_G PMOS transistor with V_G = -0.6 V, respectively. For this low I_G PMOS transistor, terminal NF is the drain. Figure 5.37(c) and (d) show a logarithmic I_S versus V_G curve of the high I_G PMOS transistor with V_D = -1.8 V, and an I_S versus V_D curve of the high I_G PMOS transistor with V_G = -0.6 V, respectively. For this high I_G PMOS transistor, terminal F is the drain.

It can be seen in (a) and (b) that the current of the low I_G PMOS transistor is left



(a) V_S = -1.8V

(b) V_G = -0.6V

(c) V_D = -1.8V

(d) V_G = -0.6V

Figure 5.37: (a) I_D versus V_G and (b) I_D versus V_S curves of a low I_G PMOS transistor, and (c) I_S versus V_G and (d) I_S versus V_D curves of the high I_G PMOS transistor, on which the gate oxide damaging procedure was not performed, measured before irradiation and after each irradiation period.

virtually unaffected by the low doses. These curves are noticeably different than those obtained from the low I_G PMOS transistor irradiated to high doses shown in Figure 5.20. This shows that the low doses do not adversely affect the operation of non-defective PMOS transistors.

The subthreshold current of the high I_G PMOS transistor, shown in Figure 5.37(c), does not show a significant increase. An increase is, however, seen in the I_S versus V_D curves shown in Figure 5.37(d). Upon inspection of Figure 5.38, which shows I_G versus V_D curves obtained from the transistor biasing scheme used to obtain the plot in Figure 5.37 (d), with V_G also set at -0.6 V, this increase can again be attributed to a radiation-induced increase in the current flowing through the gate oxide short. As was the case for the high I_G PMOS transistor irradiated to high doses, we see that the the value of I_G after each irradiation period remains relatively constant regardless of the magnitude of the voltage difference between gate and drain.

The plot in Figure 5.39 shows the percent change in I_{NF} of the 4 low I_G PMOS transistors biased as they would be in an inverter with V_{in} = V_{DD} and V_{SS}, measured after each irradiation period. The means and standard errors of these values, calculated over the 4 transistors, are shown in the plot. As can be seen in this plot, I_{NF} measured for an inverter input of V_{SS} does not increase, and even decreases, after an absorbed dose of 130 Gy(SiO_2), but I_{NF} measured for an inverter input of V_{DD} does increase significantly. This indicates that the low doses adversely affect non-defective PMOS transistors, and are therefore too high to be useful for I_{DDQ}

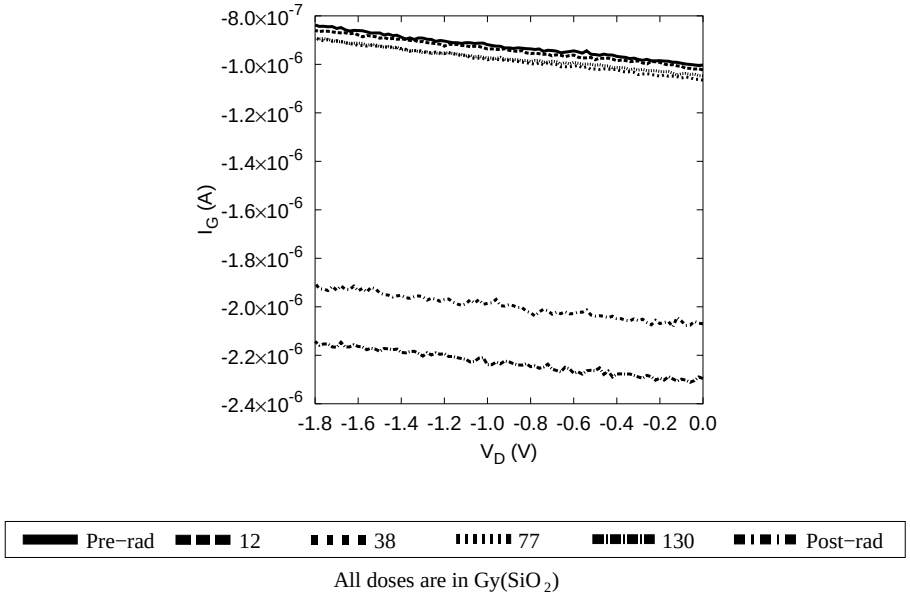


Figure 5.38: I_G versus V_D curve of a high I_G PMOS transistor for V_G = -0.6 V, measured before irradiation and after each irradiation period.

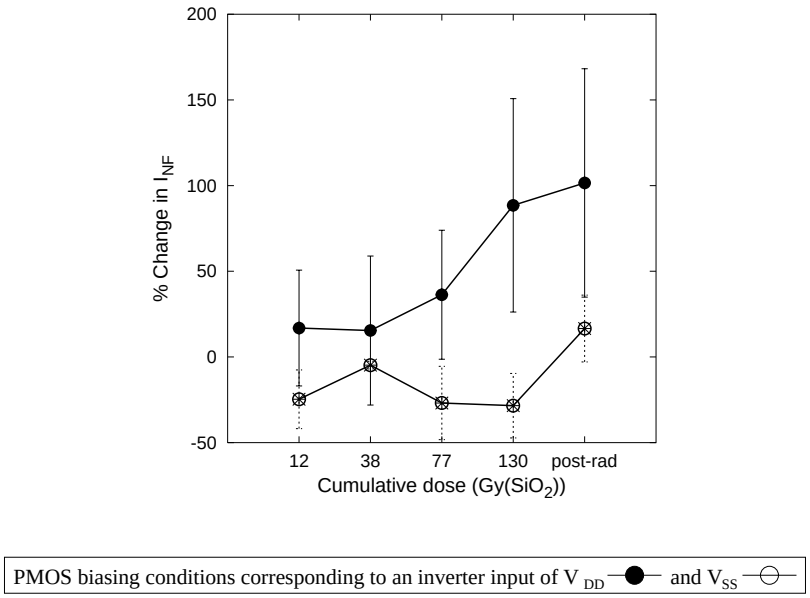


Figure 5.39: Changes, as a percentage of the pre-irradiation values, of I_{NF} of low I_G PMOS transistors biased as they would be in an inverter with V_{in} = V_{DD} and V_{SS}, computed after each irradiation period.

testing. This is a strange result, since we would expect that a dose of radiation that does not increase the current in an NMOS transistor would also not increase the current in a PMOS transistor due to its higher radiation tolerance.

The percent change, after each irradiation period, in the difference between I_F of the high I_G PMOS transistor on which the gate oxide damaging procedure was not performed, biased in the high I_G inverter biasing conditions, and the I_{NF} of each of the 4 low I_G PMOS transistors, biased in the low I_G inverter biasing conditions, is shown in Figure 5.40. The mean and standard error over these 4 differences have been calculated and are shown in the figure. As can be seen, this difference does increase, again indicating that radiation does aid in the detection of the gate oxide short in this high I_G PMOS transistor.

The percent change, after each irradiation period, in the differences between I_F of the 4 high I_G PMOS transistors on which the gate oxide damaging procedure was performed, biased in the high I_G inverter biasing conditions, and the I_{NF} of each of the 4 low I_G PMOS transistors, biased in the low I_G inverter biasing conditions, is shown in Figure 5.41. One plot has been made for each high I_G PMOS transistor, where the mean and standard error over the differences between the I_F of the high I_G PMOS transistor and the I_{NF} of all of the low I_G PMOS transistors are shown in each plot. That is, each of these plots compares one high I_G PMOS transistor with all of the low I_G PMOS transistors. As can be seen in these figures, the current difference, for the most part, decreases with exposure to radiation. This is in contrast with the

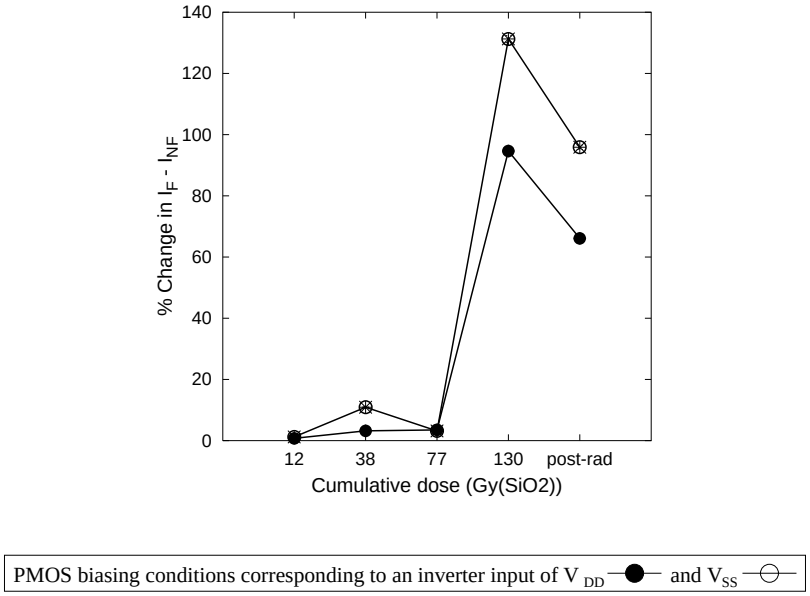


Figure 5.40: Changes, as a percentage of the pre-irradiation values, in the difference between I_F of the high I_G PMOS transistor, on which the gate oxide damaging procedure was not performed, and I_{NF} of low I_G PMOS transistors computed after each irradiation period.

result shown in Figure 5.40, in which an increase in the current difference is seen.

These plots show that the current through the gate oxide short of the high I_G PMOS transistor, on which the oxide damaging procedure was not performed, increases far more with exposure to radiation, than the current through the gate oxide short of the high I_G PMOS transistor, on which the oxide damaging procedure was performed. This suggests that the gate oxide damage in these two cases is different.

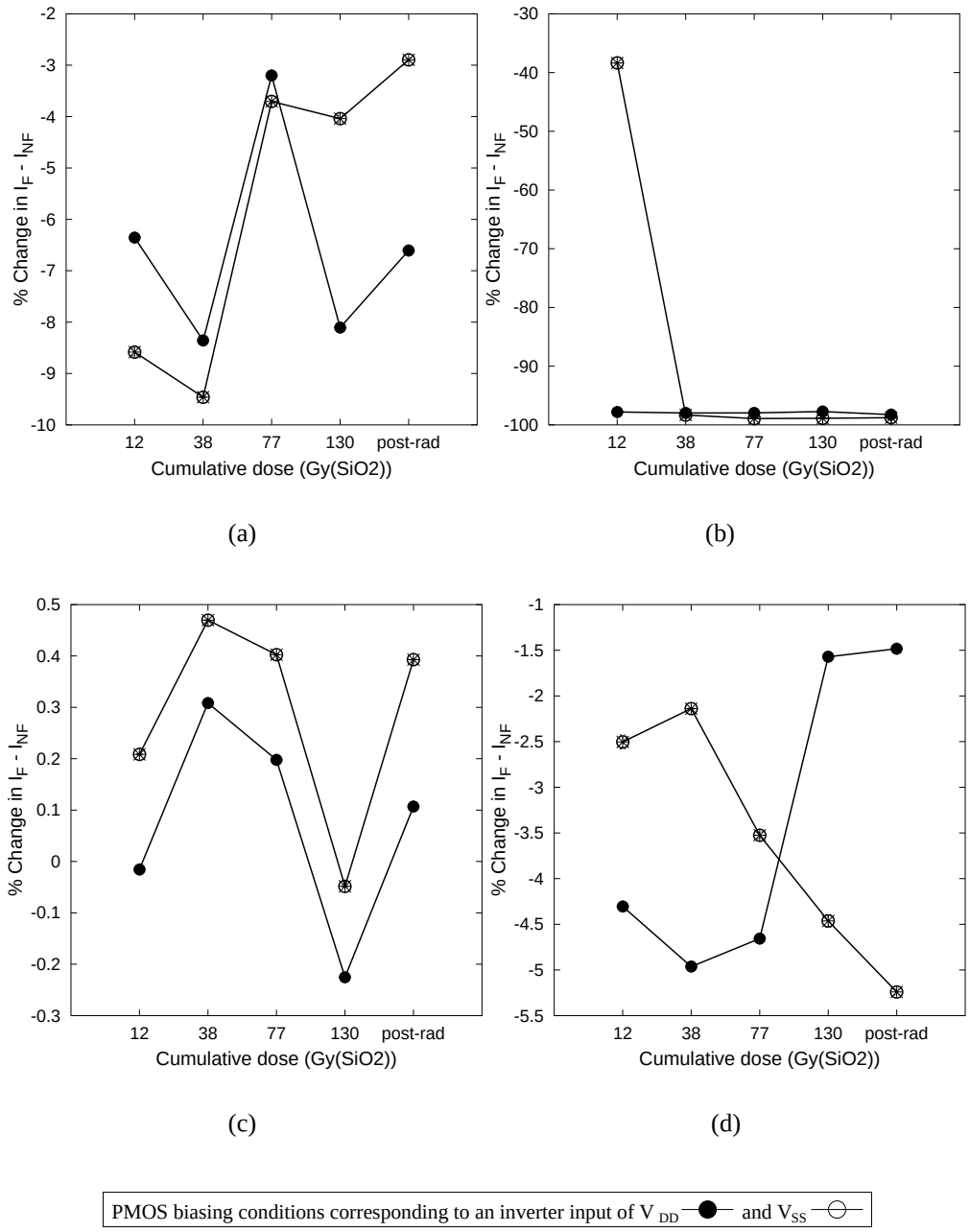


Figure 5.41: Changes, as a percentage of the pre-irradiation values, in the difference between I_F of a high I_G PMOS transistor, on which the gate oxide damaging procedure was performed, and I_{NF} of low I_G PMOS transistors computed after each irradiation period.

5.6 Summary

In this chapter, we first explained how the data obtained from the tests performed on inverter chains and transistors was analyzed. Transistors were divided into two groups based on the magnitude of their gate currents and the behaviour observed in their I_G measurements. Irradiation tests were done using two different sets of doses. The first set of doses was used to gauge the dose at which the non-defective inverter chain and low I_G transistors begin to be adversely affected, and to allow observation of any beneficial effects of exposure to radiation.

This set of doses increased the subthreshold leakage current of transistors with low gate current, and was thus considered to be too high to be beneficial for I_{DDQ} testing. We have shown that the difference in the I_{DDQ} of defective and non-defective inverter chains was not increased with exposure to radiation. However, radiation was shown to increase the current flowing through gate oxide shorts. This behaviour was shown in Figures 5.17 and 5.21. This increased the difference in current which can be used to differentiate transistors with high and low gate currents, as was shown in Figures 5.19 and 5.23.

Based upon observation of the effects caused by the first set of doses, a second set of doses was chosen which would not adversely affect non-defective inverter chains and low I_G transistors. Although the difference in the I_{DDQ} of defective and non-defective inverter chains was not increased, it was shown that the second set of doses still caused an increase in the current flowing through gate oxide shorts. This behaviour is shown again in Figures 5.33 and 5.38. This again increased the difference in current used to differentiate transistors with high and low gate currents, as was shown in Figures 5.35 and 5.40. This result is significant because it suggests that an amount of radiation that does not adversely affect non-defective transistors can still increase the current flowing through gate oxide shorts, and thus aid in the detection of their presence. Figures 5.34 and 5.39 show the low levels of change in the currents of low I_G transistors. Thus, these doses are potentially beneficial to I_{DDQ} testing. However, this beneficial effect was only observed for transistors with high gate current on which the gate oxide damaging procedure was not performed. We have inferred that this is due to a difference in the physical nature of the gate oxide damage in the transistors with high gate current, on which the gate oxide damaging procedure was not performed, and the transistors with high gate current, on which the gate oxide damaging procedure was performed. A general summary of the experimental results is shown in Table 5.3.

	230 to 4200 Gy(SiO_2)	12 to 130 Gy(SiO_2)
I_{DDQ} of defect-free inverter chain for $V_{in} = V_{DD}$ & V_{SS}	Large increase	Small increase
I_{DDQ} of defective inverter chain for $V_{in} = V_{DD}$ & V_{SS}	Small increase	No significant change
Difference between I_{DDQ} of defective and defect-free inverter chains for $V_{in} = V_{DD}$ & V_{SS}	No change or decrease	No significant change
I_{NF} of low I_G NMOS	Large increase	Small decrease
Difference between I_F of high I_G NMOS and I_{NF} of low I_G NMOS	Large increase	Varying increases
I_{NF} of low I_G PMOS	Large increase	Small increase
Difference between I_F of high I_G PMOS and I_{NF} of low I_G PMOS	Large increase	Increase or decrease

Table 5.3: Summary of current changes due to irradiation.

Chapter 6

Conclusions

The usefulness of I_{DDQ} testing is lowered as integrated circuit feature sizes are scaled down and leakage currents are consequently increased. This problem threatens to render this valuable testing technique obsolete. This work presents the results of research into the effects of ionizing radiation on CMOS circuits and defects commonly found in these circuits. These effects have been investigated in order to determine whether the application of ionizing radiation can be used to increase the difference in current that is used by I_{DDQ} testing to differentiate between defective and non-defective static CMOS circuits, and thus improve its effectiveness.

An experiment has been constructed in order to determine the effects in question. A test chip containing a series of test circuits has been designed and implemented. This chip contains multiple versions of a static CMOS inverter chain: One non-defective version and other versions containing physical approximations of various defects that are commonly found in CMOS circuits. As well, the test chip contains minimum length single NMOS and PMOS transistors which were classified as being representative of defective or non-defective transistors based on the magnitude of the gate current measured in each transistor. These test circuits have been irradiated using two sets of doses and the resulting effects on their behaviour have been analyzed.

In Chapter 4, the logistical details of the experiment were described. The design decisions involved with the design of the test chip were explained. These decisions were influenced by area restrictions, the need to electrically isolate each test circuit, and the need to emulate not only the electrical characteristics but also the physical characteristics of actual circuit defects that largely determine the effects of radiation.

In Chapter 5, the data obtained from the experiment was analyzed. Because we are interested in the effects of radiation as they pertain to I_{DDQ} testing, the test circuits were analyzed when they were biased as they would be if they were part of a large digital static CMOS IC in steady state, meaning that all logic gates in the circuit would see a gate voltage of either V_{DD} or V_{SS}. Transistors were analyzed when biased as they would be in an inverter chain in steady state.

It has been found that the difference in the I_{DDQ} of the defective and non-defective inverter chains was not increased with exposure to radiation. However, it has also been found that exposure to ionizing radiation can increase the current flowing through gate oxide shorts, and can thus aid in revealing the presence of these shorts using I_{DDQ} testing. The difference in power supply current flowing through MOSFETs classified as having high and low gate current was increased by up to an order of magnitude after exposure to radiation. Furthermore, this beneficial effect occurs for doses of radiation that apparently do not adversely affect non-defective NMOS transistors. PMOS transistors were observed to be adversely affected under certain biasing conditions. These results imply that a calibrated dose of radiation could possibly be used to aid in the detection of gate oxide shorts in an IC without fear of causing undesirable permanent damage to non-defective parts of the circuit.

However, it was found that the amount by which the current flowing through a gate oxide short increases is likely dependent on the nature of the damage in the oxide. Some transistors whose gate oxide was damaged by applying high voltage drops across the oxide did not show an increase in this current, whereas other transistors, that had high gate current but were not damaged in this way, did show such an increase.

6.1 Future Work

This research suggests that radiation could be used to aid in the detection of gate oxide shorts using I_{DDQ} testing. However, the physical nature of the gate oxide shorts, through which current was increased with radiation, is unknown. The fact that the transistors, whose gate oxide was damaged using high voltage, did not show this increase in current, indicates that the gate oxide damage in these two cases is somehow different. It would be of value to determine what this difference is. This could perhaps be done by obtaining an image of the defect in both cases, or by determining their chemical composition. Including this task in this thesis was considered, but the etching and imaging processes involved were deemed to be too difficult with too little chance of success to do so given the time and resources available.

It should also be noted that, as previously mentioned, the transistors that were classified as having low gate current still exhibited a level of gate current that exceeds the expected level for the technology used. That is, these transistors were still defective to some degree. Measurements were performed in such a way to approximate defect-free transistors, but it is possible that this still introduced a degree of error into the data and results obtained. Also, the defects designed into the defective versions of the inverter chain are only approximations of actual defects, and likely differ in resistance and chemical composition from defects found

in industry-manufactured ICs. It would therefore be useful to perform this experiment on industry-manufactured ICs that are known to contain specific types of defects.

Finally, the scope and resources of this experiment did not allow for the variation of parameters such as transistor width-to-length ratios, defect sizes and resistances, and magnitude of radiation doses. It would be instructive to perform this experiment while varying these parameters in order to determine their effect on the effects of radiation. It would be particularly interesting to use a number of doses lower than the lowest ones used in this work. This could aid in determining a dose of radiation that would leave non-defective CMOS circuits completely unaffected, as well as determine the lowest amount of radiation that one could use to produce the beneficial effect described above.

Bibliography

[1] J. M. Rabaey, A. Chandrakasan, B. Nikolic, *Digital Integrated Circuits*, Prentice Hall, 2nd edition, 2003.

[2] W. Mao, R. K. Gulati, D. K. Goel, M. D. Cilletti, "QUIETEST: A Quiescent Current Testing Methodology for Detecting Leakage Faults," in *Proceedings of the IEEE International Conference on Computer-Aided Design*, 1990, pp. 180–283.

[3] M. W. Levi, "CMOS is most testable," in *Proceedings of the International Test Conference*, 1981, pp. 217–220.

[4] M. L. Bushnell and V. D. Agrawal, *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits*, Kluwer Academic Publishers, 2000.

[5] J. P. Shen, W. Maly, F. J. Ferguson, "Inductive Fault Analysis of MOS Integrated Circuits," *IEEE Design and Test*, vol. 2, no. 6, pp. 13–26, 1985.

[6] J. Ferguson and J. P. Shen, "A CMOS Fault Extractor for Inductive Fault Analysis," *IEEE Transactions on Computer-Aided Design*, vol. 7, no. 11, pp. 1181–1194, 1988.

[7] P. C. Maxwell, R. C. Aitken, K. R. Kollitz and A. C. Brown, "I_{DDQ} and AC Scan: The War Against Unmodelled Defects," in *Proceedings of the International Test Conference*, 1996, pp. 250–258.

[8] P. Franco, S. Ma, J. Chang, Y. Chu, S. Wattal, E. J. McCluskey, R. L. Stokes, W. D. Farwell, "Analysis and Detection of Timing Failures In An Experimental Test Chip," in *Proceedings of the International Test Conference*, 1996, pp. 691–700.

[9] E. J. McCluskey and C. Tsang, "Stuck-Fault Tests vs. Actual Defects," in

Proceedings of the International Test Conference, 2000, pp. 336–342.

[10] P. Nigh, W. Needham, K. Butler, P. Maxwell, R. Aitken, "An Experimental Study Comparing the Relative Effectiveness of Functional, Scan, I_{DDQ} and Delay-fault Testing," in *Proceedings of VLSI Test Symposium*, 1997, pp. 459–464.

[11] P. Nigh, D. Vallett, A. Patel, J. Wright, F. Motika, D. Forlenza, R. Kurtulik, W. Chong, "Failure Analysis of Timing and I_{DDQ}-only Failures from the SEMATECH Test Methods Experiment," in *Proceedings of the International Test Conference*, 1998, pp. 43–52.

[12] P. Nigh, W. Needham, K. Butler, P. Maxwell, R. Aitken, W. Maly, "So What Is An Optimal Test Mix? A Discussion of the SEMATECH Methods Experiment," in *Proceedings of the International Test Conference*, 1997, pp. 1037–1038.

[13] P. C. Wiscombe, "A Comparison of Stuck-at Fault Coverage and I_{DDQ} Testing on Defect Levels," in *Proceedings of the International Test Conference*, 1993, pp. 293–299.

[14] R. Perry, "I_{DDQ} Testing in CMOS Digital ASICs," *Journal of Electronic Testing: Theory and Applications*, vol. 3, no. 4, pp. 31–39, 1992.

[15] A. E. Gattiker and W. Maly, "Toward Understanding 'I_{DDQ}-Only' Fails," in *Proceedings of the International Test Conference*, 1998, pp. 174–183.

[16] R. R. Fritzmeier, J. M. Soden, R. K. Treece, C. F. Hawkins, "Increased CMOS IC Stuck-At Fault Coverage with Reduced I_{DDQ} Test Sets," in *Proceedings of the International Test Conference*, 1990, pp. 427–433.

[17] F. Zarrinfar and R. Rajsuman, "Automated I_{DDQ} Testing from CAD to Manufacturing," in *Proceedings of IEEE International Workshop on I_{DDQ} Testing*, 1995, pp. 48–51.

[18] R. Rajsuman, "I_{DDQ} Testing for CMOS VLSI," *Proceedings of the IEEE*, vol. 88, no. 4, pp. 544–566, 2000.

[19] P. Nigh and A. Gattiker, "Test Method Evaluation Experiments and Data," in *Proceedings of the International Test Conference*, 2000, pp. 454–463.

[20] C. F. Hawkins, J. M. Soden, A. W. Righter, F. J. Ferguson, "Defect Classes - An Overdue Paradigm for CMOS IC Testing," in *Proceedings of the International Test Conference*, 1994, pp. 413–425.

[21] J. M. Soden and C. F. Hawkins, "Electrical Properties and Detection Methods for CMOS IC Defects," in *Proceedings of the European Test Conference*, 1989, pp. 159–167.

[22] J. M. Acken and S. D. Millman, "Accurate Modeling and Simulation of Bridging Faults," in *Proceedings of the Custom Integrated Circuit Conference*, 1991, pp. 17.4.1–17.4.4.

[23] H. T. Vierhaus, W. Meyer, U. Glaser, "CMOS Bridges and Resistive Transistor Faults: I_{DDQ} Versus Delay Effects," in *Proceedings of the International Test Conference*, 1993, pp. 83–91.

[24] F. J. Ferguson, M. Taylor, T. Larrabee, "Testing for Parametric Faults in Static CMOS Circuits," in *Proceedings of the International Test Conference*, 1990, pp. 436–442.

[25] R. Rodriguez-Montanes, E. M. J. G. Bruls, J. Figueras, "Bridging Defects Resistance Measurements In A CMOS Process," in *Proceedings of the International Test Conference*, 1992, pp. 892–898.

[26] J. M. Soden and C. F. Hawkins, "Test Considerations for Gate Oxide Shorts in CMOS ICs," *IEEE Design and Test of Computers*, vol. 3, pp. 56–64, 1986.

[27] M. J. Middendorf and T. Hausken, "Observed Physical Effects and Failure Analysis of EOS/ESD on MOS Devices," in *Proceedings of the International Symposium for Testing and Failure Analysis*, 1984, pp. 205–213.

[28] J. M. Soden and C. F. Hawkins, "Reliability of CMOS ICs with gate oxide shorts," *Semiconductor International*, vol. 10, pp. 240–245, 1987.

[29] C. F. Hawkins and J. M. Soden, "Electrical Characteristics and Testing Considerations for Gate Oxide Shorts in CMOS ICs," in *Proceedings of the International Test Conference*, 1985, pp. 544–555.

[30] J. Segura, C. De Benito, A. Rubio, C. F. Hawkins, "A Detailed Analysis and Electrical Modeling of Gate Oxide Shorts in MOS Transistors," *Journal*

of Electronic Testing: Theory and Applications, vol. 8, no. 3, pp. 229–239, 1996.

[31] J. Segura, A. Rubio, J. Figueras, "Analysis and Modeling of MOS Devices with Gate Oxide Short Failures," in *Proceedings of the International Symposium on Circuits and Systems*, 1985, pp. 2164–2167.

[32] C. F. Hawkins and J. M. Soden, "Reliability and Electrical Properties of Gate Oxide Shorts in CMOS ICs," in *Proceedings of the International Test Conference*, 1986, pp. 443–451.

[33] H. Hao and E. J. McCluskey, "Analysis of Gate Oxide Shorts in CMOS Circuits," *IEEE Transactions on Computers*, vol. 42, no. 12, pp. 1510–1516, 1993.

[34] M. Syrzycki, "Modelling of Spot Defects in MOS Transistors," in *Proceedings of the International Test Conference*, 1987, pp. 148–156.

[35] W. Maly, P. K. Nag, P. Nigh, "Testing Oriented Analysis of CMOS ICs With Opens," in *Proceedings of the International Conference on Computer Aided Design*, 1988, pp. 344–347.

[36] V. H. Champac, A. Rubio, J. Figueras, "Electrical Model of the Floating Gate Defect in CMOS IC's: Implications on I_{DDQ} Testing," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 13, no. 3, pp. 359–369, 1994.

[37] M. Renovell and G. Gambon, "Topology Dependence of Floating Gate Faults in MOS Circuits," *Electronics Letters*, vol. 22, no. 3, pp. 152–153, 1986.

[38] R. Rodriguez-Montanes, J. A. Segura, V. H. Champac, J. Figueras, J. A. Rubio, "Current vs. Logic Testing of Gate Oxide Short, Floating Gate, and Bridging Failures in CMOS," in *Proceedings of the International Test Conference*, 1991, pp. 510–519.

[39] Semiconductor Industry Association, *International Technology Roadmap for Semiconductors, Process Integration, Devices, and Structures*, 2001 edition, `http://public.itrs.net/Files/2001ITRS/PIDS.pdf`.

[40] T. W. Williams, R. Kapur, M. R. Mercer, R. H. Dennard, W. Maly, "I_{DDQ}

testing for high performance CMOS-the next ten years," in *Proceedings of the European Test Conference*, 1996, pp. 578–583.

[41] A. Keshavarzi, K. Roy, C. F. Hawkins, "Intrinsic Leakage in Low Power Deep Submicron CMOS ICs," in *Proceedings of the International Test Conference*, 1997, pp. 146–155.

[42] J. Figueras, A. M. Brosa, A. Ferre, "Test Changes in Nanometric CMOS Technologies," *Microelectronic Engineering*, vol. 49, no. 1-2, pp. 119–133, 1999.

[43] M. Sachdev, "Current-Based Testing for Deep-Submicron VLSIs," *IEEE Design and Test of Computers*, vol. 18, no. 2, pp. 76–84, 2001.

[44] Y. Taur, D. A. Buchanan, W. Chen, D. J. Frank, K. E. Ismail, S. Lo, G. A. Sai-Halasz, R. G. Viswanathan, H. C. Wann, S. J. Wind, H. Wong, "CMOS Scaling into the Nanometer Regime," *Procedings of the IEEE*, vol. 85, no. 4, pp. 486–504, 1997.

[45] C. Thibeault, "An Histogram Based Procedure for Current Testing of Acitve Defects," in *Proceedings of the International Test Conference*, 1999, pp. 714–723.

[46] A. E. Gattiker and W. Maly, "Current Signatures: Application," in *Proceedings of the International Test Conference*, 1997, pp. 156–165.

[47] D. C. Giancoli, *Physics for Scientists and Engineers*, Prentice Hall, 2nd edition, 1988.

[48] G. C. Messenger, M. S. Ash, *The Effects of Radiation on Electronic Systems*, Van Nostrand Reinhold Company Inc., 1986.

[49] A. M. Chugg, "Ionising radiation effects: a vital issue for semiconductor electronics," *Engineering Science and Education Journal*, pp. 123–130, June 1994.

[50] T. P. Ma, P. V. Dressendorfer, *Ionizing Radiation Effects in MOS Devices and Circuits*, Wiley-Interscience, 1989.

[51] T. R. Oldham, F. B. McLean, "Total Ionizing Dose Effects in MOS Oxides and

Devices," *IEEE Transactions on Nuclear Science*, vol. 50, no. 3, pp. 483–499, 2003.

[52] G. M. Anelli, *Design and Characterization of Radiation Tolerant Integrated Circuits in Deep Submicron CMOS Technologies for the LHC Experiments*, Ph.D. thesis, Institut National Polytechnique de Grenoble, 2000.

[53] A. Giraldo, *Evaluation of Deep Submicron Technologies with Radiation Tolerant Layout for Electronics in LHC Environments*, Ph.D. thesis, Universita Degli Studi di Padova, 1998.

[54] A. Scarpa, A. Paccagnella, F. Montera, G. Ghibaudo, G. Pananakakis, G. Ghidini, P. G. Fuochi, "Ioonizing Radiation Induced Leakage Current on Ultra-Thin Gate Oxides," *IEEE Transactions on Nuclear Science*, vol. 44, no. 6, pp. 1818–1825, 1997.

[55] M. Ceschia, A. Paccagnella, A. Cester, A. Scarpa, G. Ghidini, "Radiation Induced Leakage Current and Stress Induced Leakage Current in Ultra-Thin Gate Oxides," *IEEE Transactions on Nuclear Science*, vol. 45, no. 6, pp. 2375–2382, 1998.

[56] C. H. Ling, C. H. Ang, D. S. Ang, "Characterization of Leakage Current in Thin Gate Oxide Subjected to 10 keV X-Ray Irradiation," *IEEE Transactions on Electron Devices*, vol. 47, no. 3, pp. 650–652, 2000.

[57] Taiwan Semiconductor Manufacturing Company, *TSMC 0.18um Mixed Signal 1P6M Salicide 1.8V/3.3V SPICE Models, Document No. T-018-MM-SP-002*, 2000.

[58] Fibics Incorporated, "Device modification (microsurgery)," `http://www.fibics.com/SC_FIBDevMod.html`.

[59] A. N. Campbell, K. A. Peterson, D. M. Fleetwood, J. M. Soden, "Effects of focused ion beam irradiation on MOS transistors," in *Proceedings of the Reliability Physics Symposium*, 1997, pp. 72–81.

[60] D. M. Gingrich, N. J. Buchanan, C. Cojocaru, W. Syed, "X-ray Facility in the Centre for Subatomic Research at the University of Alberta," `http://www.phys.ualberta.ca/~gingrich/atlas/`

radiation.html/xray-machine.pdf, May 2003.

[61] Department of Defense (U.S.A.), *MIL-STD-883E method 1019.5 Ionizing Radiation (Total Dose) Test Procedure*, December 1997.

[62] D. Gish and D. M. Gingrich, "X-ray Dosimetry of the Switched-Capacitor Array Controller," http://www.phys.ualberta.ca/~gingrich/atlas/radiation.html/xray-dose.pdf, September 2003.

[63] S.-H. Lo, D. A. Buchanan, Y. Taur, W. Wang, "Quantum-Mechanical Modeling of Electron Tunneling Current from the Inversion Layer of Ultra-Thin-Oxide nMOSFETs," *IEEE Electron Device Letters*, vol. 18, no. 5, pp. 209–211, 1997.

Appendix A

Layouts

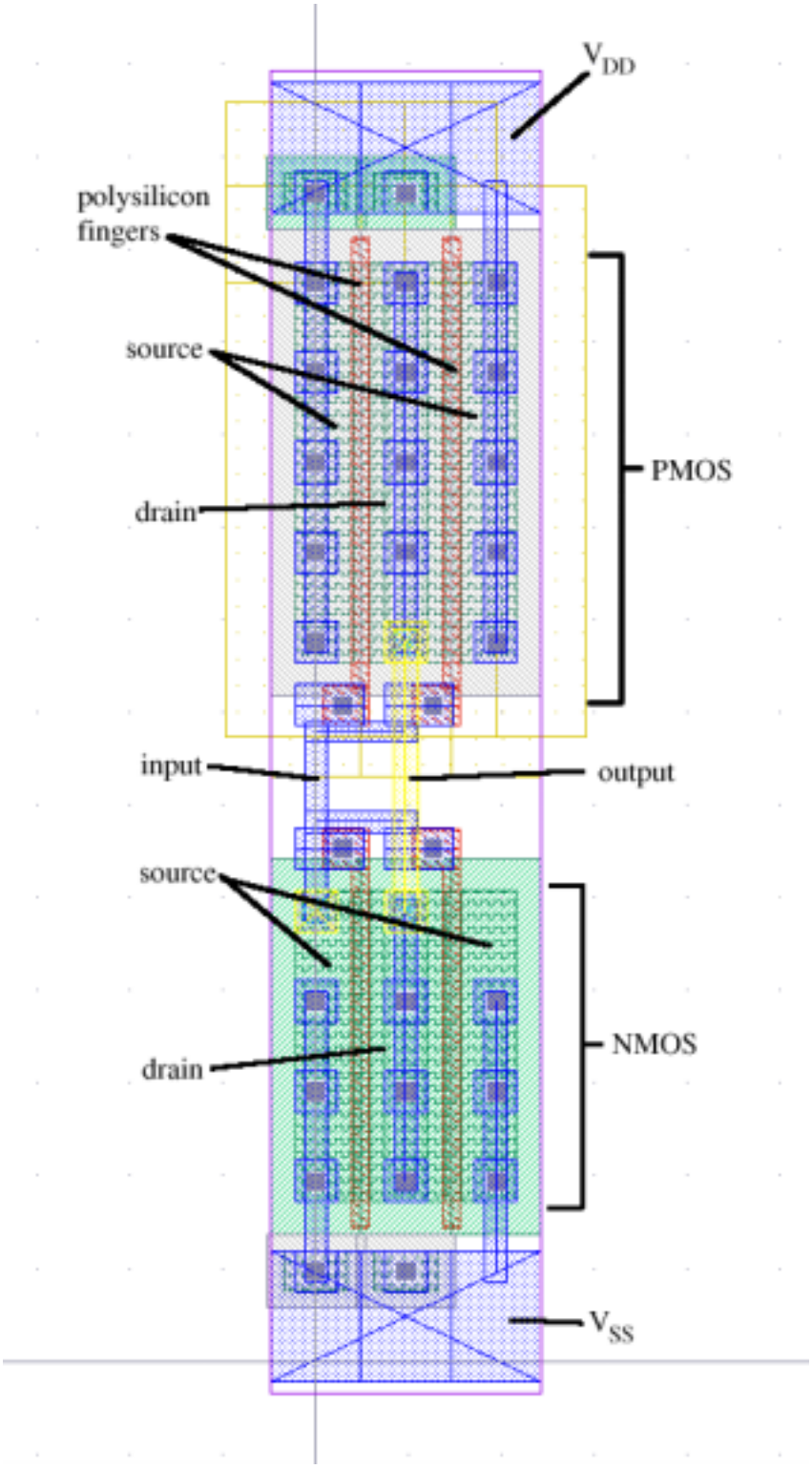


Figure A.1: Inverter layout

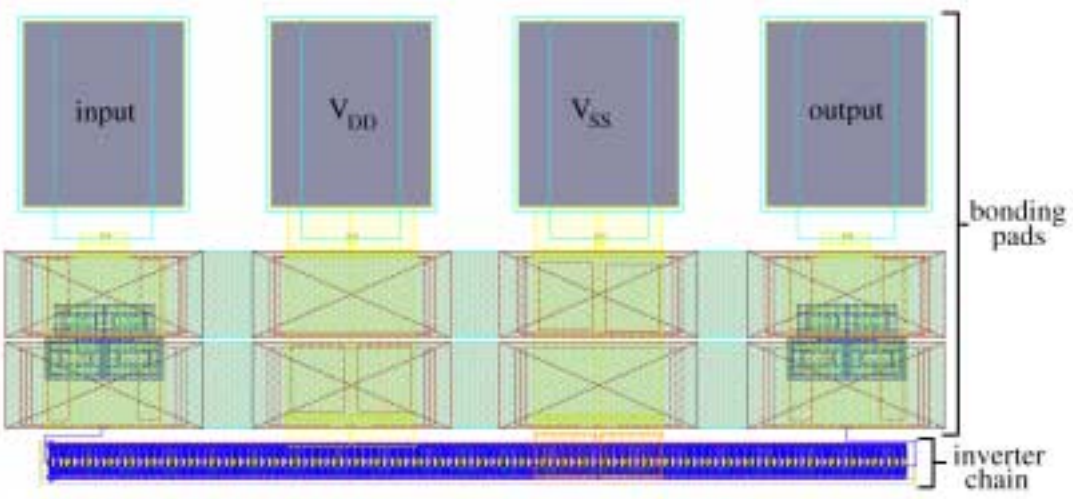


Figure A.2: Inverter chain layout

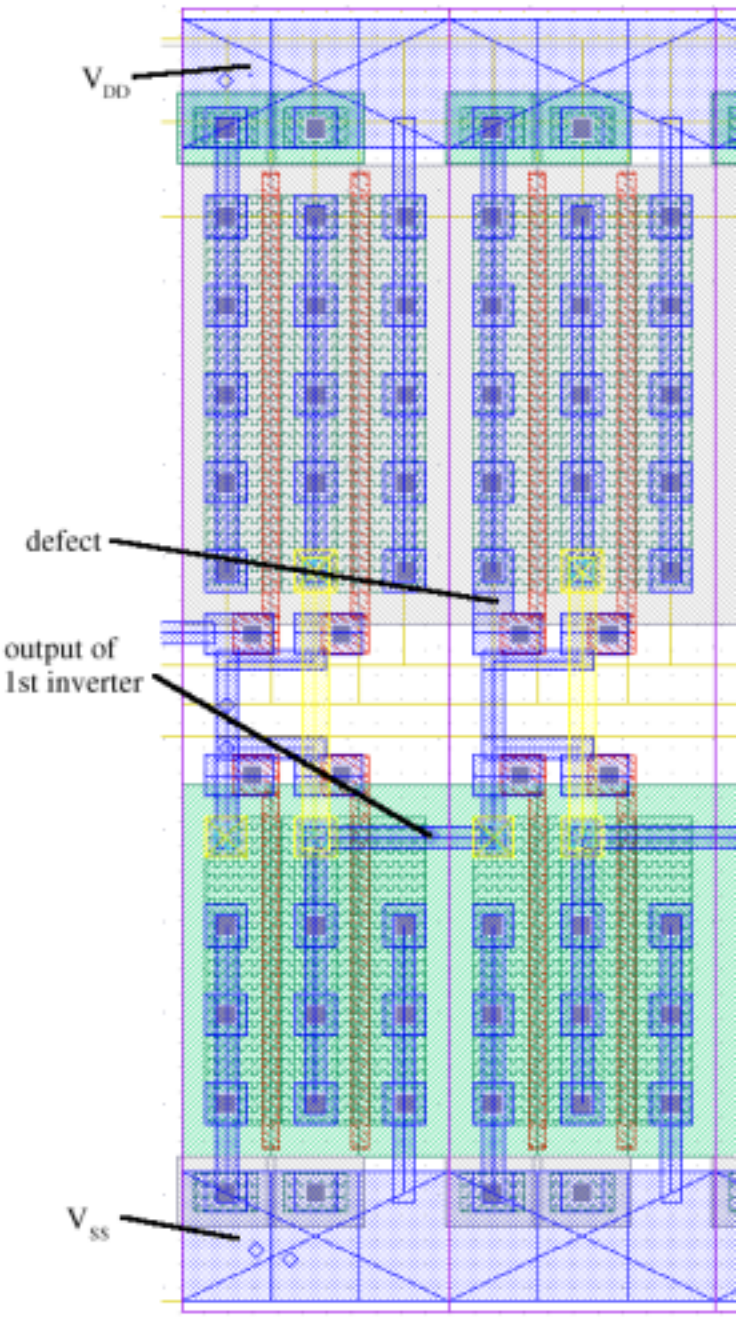


Figure A.3: Layout of V_{DD} bridge defect

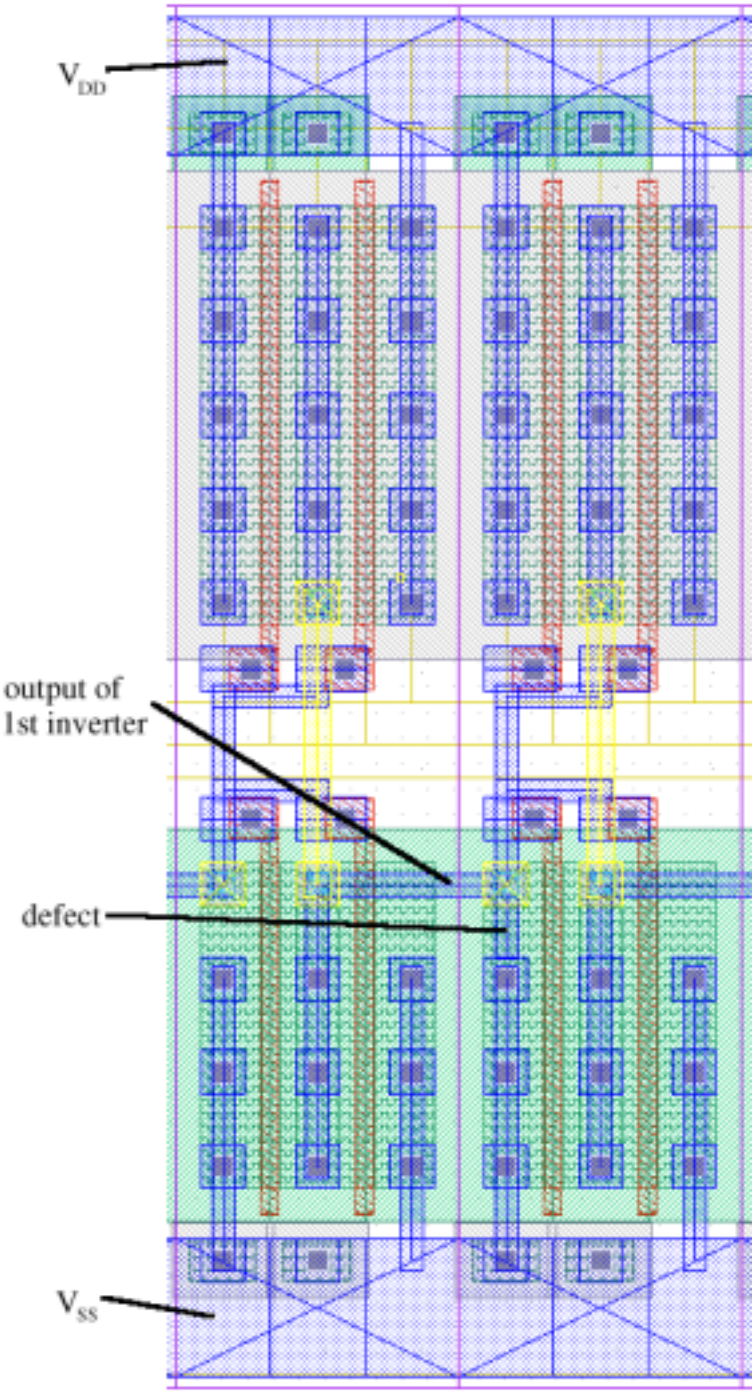


Figure A.4: Layout of V_{SS} bridge defect

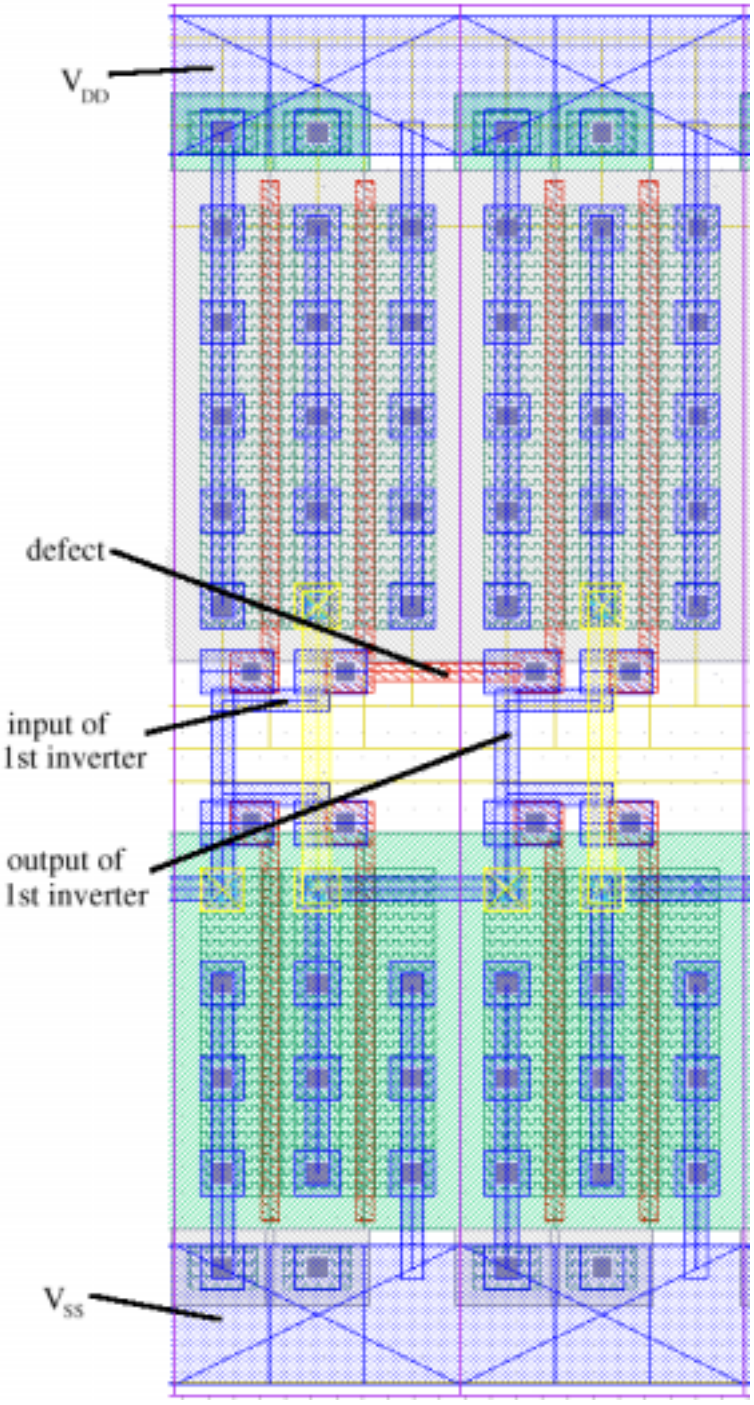


Figure A.5: Layout of input/output bridge defect

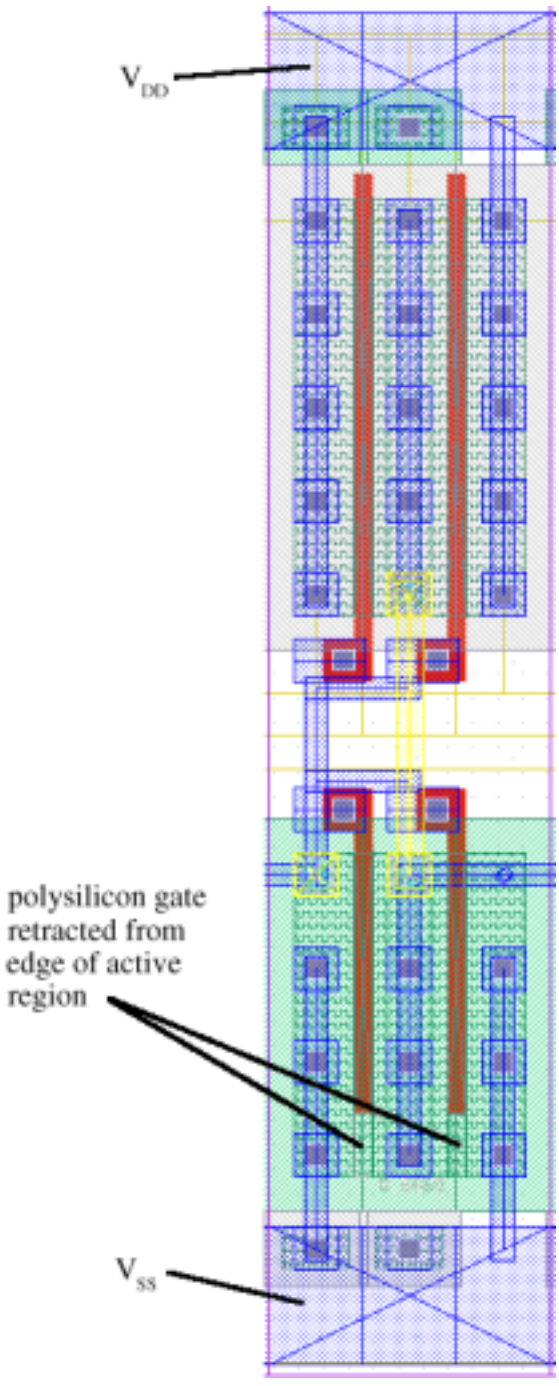


Figure A.6: Layout of NMOS stuck-on defect

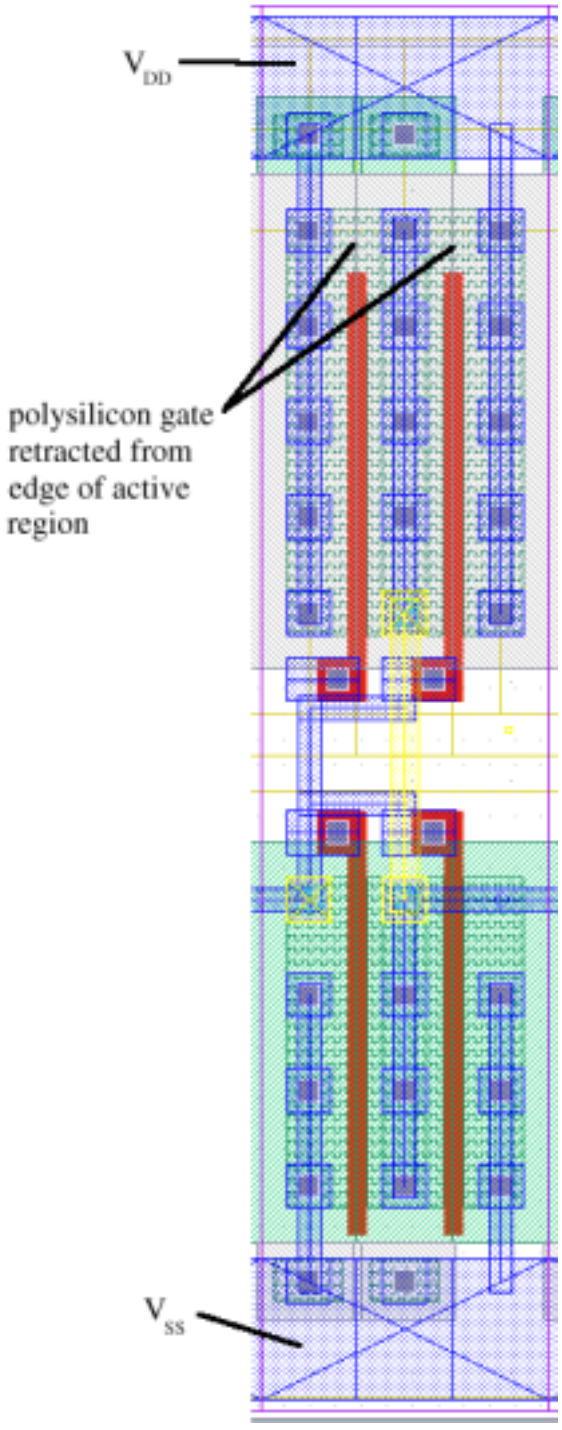


Figure A.7: Layout of PMOS stuck-on defect

Appendix B

Simulations of Inverter Chains

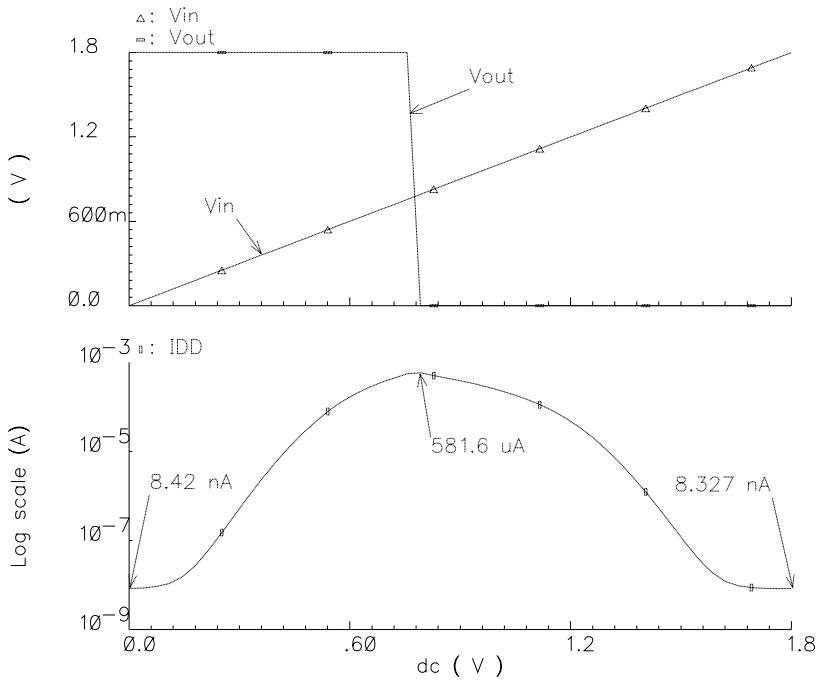


Figure B.1: Simulations of output voltage and I_{DD} versus input voltage for the defect-free inverter chain

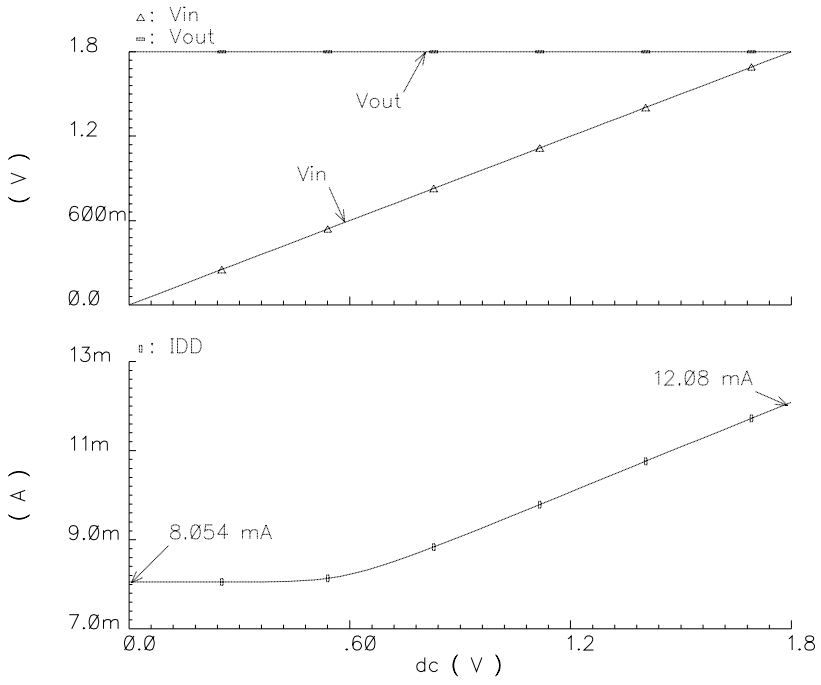


Figure B.2: Simulations of output voltage and I_{DD} versus input voltage for the inverter chain with V_{DD} bridge defects

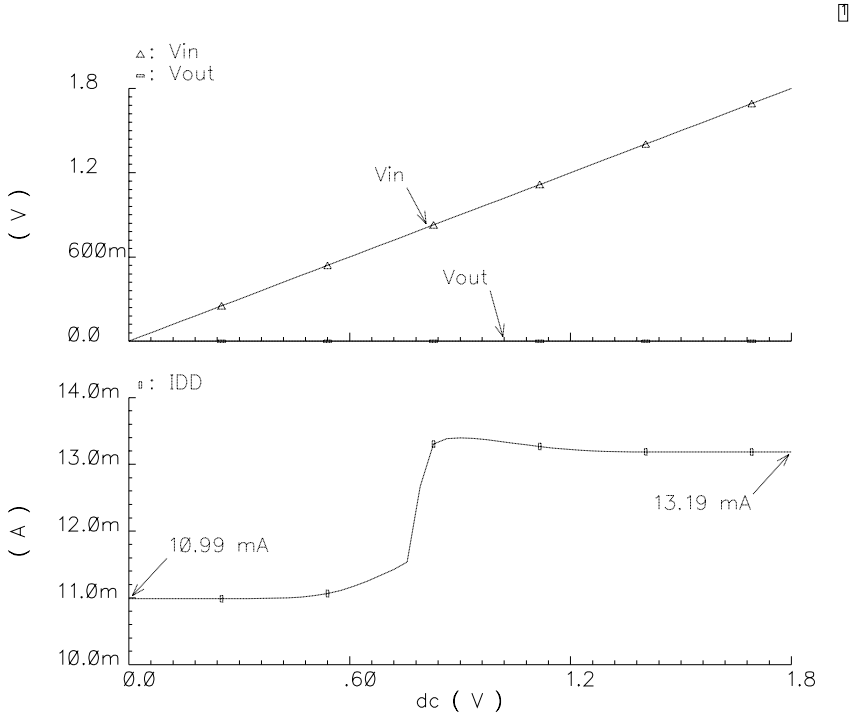


Figure B.3: Simulations of output voltage and I_{DD} versus input voltage for the inverter chain with V_{SS} bridge defects

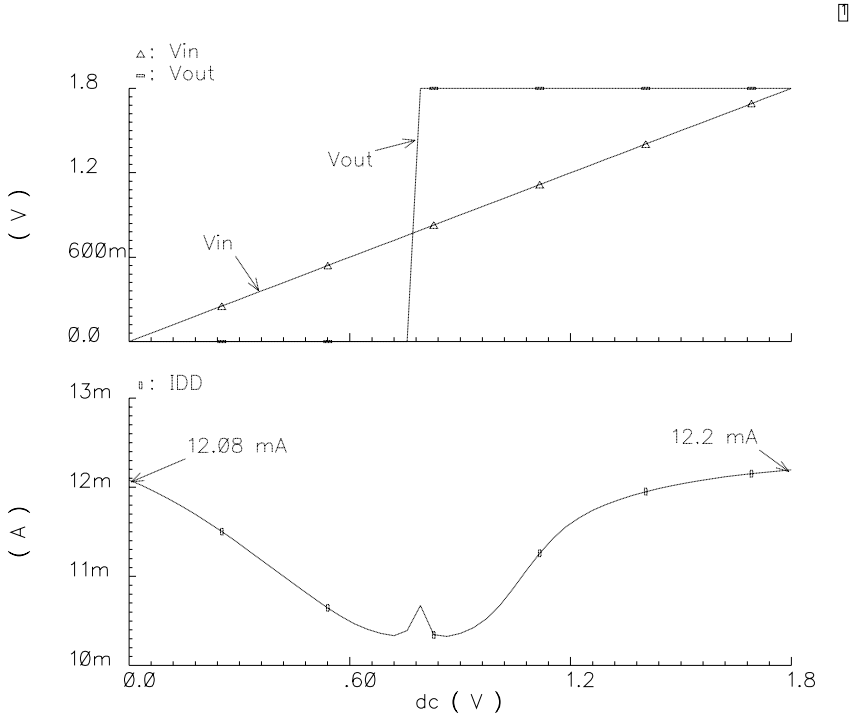


Figure B.4: Simulations of output voltage and I_{DD} versus input voltage for an inverter chain with input/output bridge defects

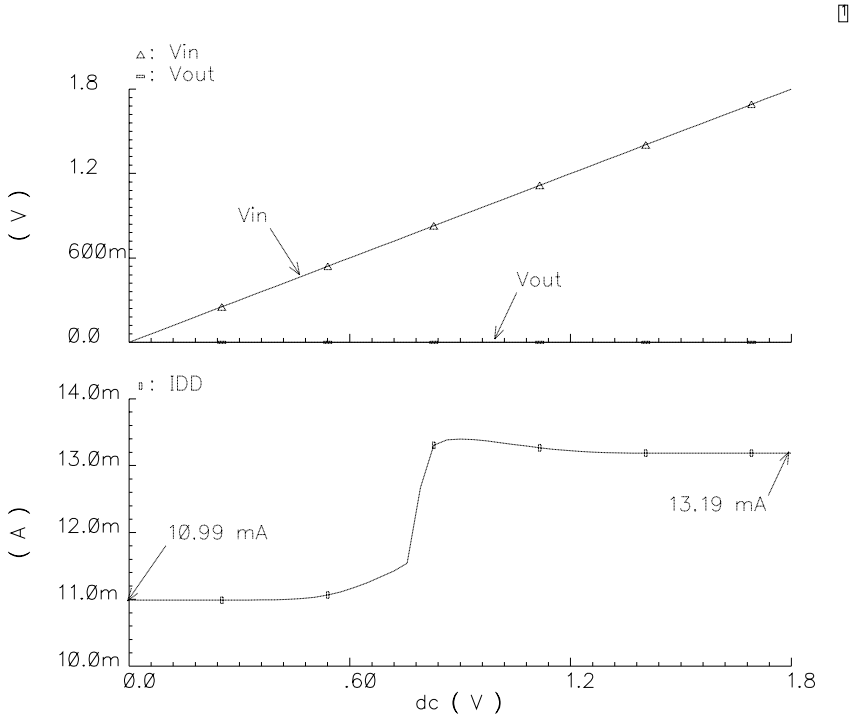


Figure B.5: Simulations of output voltage and I_{DD} versus input voltage for an inverter chain with NMOS source-drain short defects

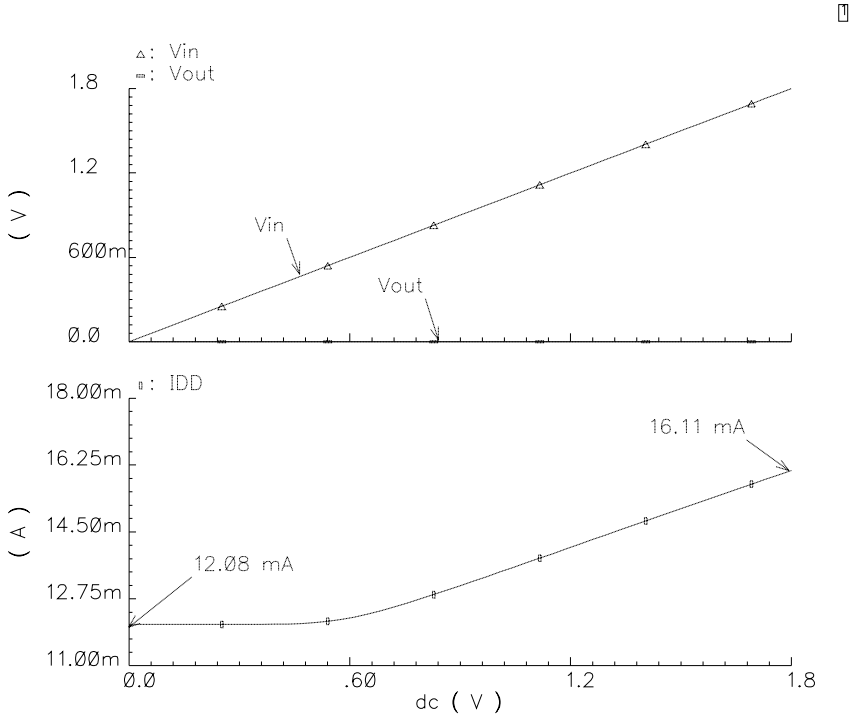


Figure B.6: Simulations of output voltage and I_{DD} versus input voltage for an inverter chain with PMOS source-drain short defects