University of Alberta Project Board (UA7K) User's Manual

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University of Alberta Project Board

User's Manual

1.0 Introduction

The UA7K is a programmable, general-purpose project board intended to be used for the EE480 digital design course. It is also intended to be useful for other course work where an "ASIC" type solution is needed.

The UA7K is basically a slimmed-down version of Altera's UP1 board. On this board students can create designs in VHDL and send them to the board via programming software and a special cable which attaches directly to the board. Programming is fast and easy, so designs can be rapidly changed, without having to remove the device from the board for programming. The Altera UP1 board has two devices, one EPM7128S (a MAX7k series device which is on our board) and one FLEX10k chip. The main difference between this board and the UA7K is that our board has space for only one device, an Altera MAX7000 series device.

The board provides many features useful for a course project board, such as push-buttons, DIP switches, LEDs, power input protection, prototyping headers, and built-in oscillators. It also provides text on the board that shows the header pin numbers and provides labels for the board's components.

For flexibility, footprints for two different versions of the MAX 7000 device are available: the 84-pin J-Lead and the 44-pin J-Lead.

1.1 MaxPlusII Software

The MaxPlusII software package can be used for all the steps of the design process: from design entry, compilation, simulation, synthesis, and finally, programming.

1.2 Download Cable

There are two different ways to program the project board. Both solutions use the MAX-PLUSII software. The first way to program the device is to use a ByteBlaster cable. The ByteBlaster cable connects to a standard parallel port. The second way to program the device is to use a BitBlaster cable. The BitBlaster cable uses a serial port connection to program the device.

Because the cable connects directly to the project board and designs are downloaded directly to the device, this means that design iterations can be accomplished quickly and easily, without having to remove the chip from the board.

For more information on the cables, see Altera's data sheet "Byte Blaster Parallel Port Download Cable" or see "Bit Blaster Serial Port Download Cable" .

2.0 Board Description

2.1 MAX 7000 Device

The UA7K has footprints for two versions of the MAX 7000 device: the 84-pin J-Lead and the 44-pin J-Lead. The 84-pin EPM7128S will probably be used exclusively, but the other footprint is there for flexibility. It should be noted that the 44pin device has not been tested in the PCB. Table 1 provided below shows the pin out of the MAX7128 device which is the one that will be typically populated.

Since the 44-pin device will not be used very often, the documentation for it is included near the end of this document. Please see "MAX7032S (44-pin) Device" on page 12 for more information.

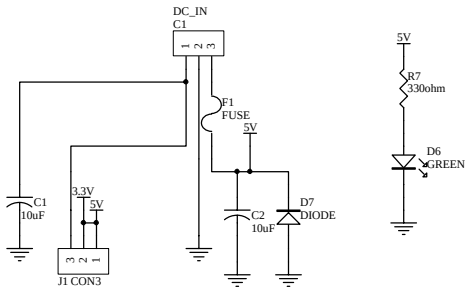
TABLE 1. EPM7128A Dedicated Pin-Outs

Dedicated Pin	84-Pin J-Lead	Project Board Connection
INPUT/GCLK1	83	Header 1 / RC Oscillator
INPUT/GCLR	1	Header 1 / PB2
INPUT/OE1	84	Header 1
INPUT/OE2/GCLK2	2	Header 1 / Crystal Oscillator
TDI	14	JTAG Connector
TMS	23	JTAG Connector
TCK	62	JTAG Connector
TDO	71	JTAG Connector
GND	7, 19, 32, 42, 47, 59, 72, 82	GND
VCCINT	3, 43	5V
VCCIO	13, 26, 38, 53, 66, 78	Va / 5V
Total User I/O Pins	64	Headers 1, 2 and 3, DIP Switches, PB1, LEDs

2.2 Power Input

The power input circuit features dual 3.3V/ 5V capability, short-circuit and reverse-polarity protection, electrolytic capacitors for regulation, and a power-on LED. This is shown in the power circuitry schematic shown on the right.

FIGURE 1. Power Supply Circuit



2.2.1 Multivolt Operation

Power is supplied to the board via a 3-pin header. Altera's Max7000 devices are capable of multi-voltage operation, allowing one device to be compatible with both 3.3V and 5V logic at the same time. This is accomplished by the Altera device having 2 sets of power pins. The first set of power pins are for an internal power supply. The second set of power supply pins are for the I/O power supply. The internal power supply must be run at 5V. The I/O power supply can be ran at either 5V or 3.3V. When the I/O uses 3.3V as its power supply it supplies a logic low of 0V, and a logic high of 3.3V. Inputs can accept a 3.3V or a 5V input because the internal circuitry is running at 5V.

The three pins on the power supply header are labeled Va, GND, and 5V. By default, the board is set up for single-voltage operation, at 5V, so normally pins GND and 5V will be connected to the power supply. The Va input is used for 3.3V operation. For more information on this, see "3.3V / 5V Operation" on page 9.

2.2.2 Input Protection

The board has a 500mA fuse for short circuit protection. A diode also protects the board from being powered with reverse polarity. If this is attempted, the diode conducts and short-circuits the power supply for a short period of time until the fuse blows. Also, if a short is ever encountered on the board then the fuse will blow if more than 500mA of current is being drawn. A 10uF electrolytic capacitor provides voltage regulation. If the board is used for 3.3V operation there is NO short circuit protection or reverse polarity protection on the 3.3V power line. There is however another 10uF electrolytic capacitor to provide voltage regulation for the 3.3V power.

2.3 Oscillators

There is space for two different oscillators on the project board, a crystal oscillator and an RC oscillator. Both are described below.

2.3.1 Crystal Oscillator

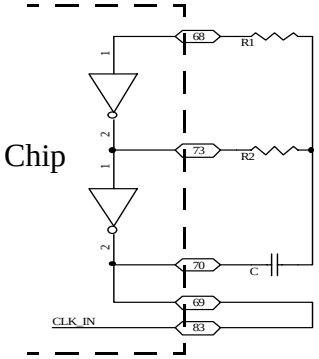
The standard EE480 board will not have a crystal oscillator, because they are quite expensive. If one is needed, any standard 4-pin oscillator can be used (they come in a 14-pin DIP package). The output of the crystal is directly connected to pin 2 (GCLK2) of the

EPM7128S device. The connection is made through J4 so that the crystal can be disconnected if required. The board can also support a half crystal which comes in a 8-pin DIP package.

The Altera UP1 board uses a 25.175 MHz crystal, but that board uses a higher speed chip (-7 opposed to our -10 chips). So, a conservative choice would be an 8MHz crystal, but requirements may vary depending on the particular design being programmed on the board.

2.3.2 RC Oscillator

FIGURE 2. Relaxation Oscillator



With some logic between input terminals, a cheap oscillator can be made from only two resistors and a capacitor:

In the above figure, positive feedback is applied to the capacitor terminal, and negative feedback is applied to R2. The system input is at R1. The frequency of the resulting oscillator is approximately:

$$f \cong 1/(2.2 \times R2 \times C)$$

This formula is most accurate if the component values have the following limitations:

$$R2 > 10R1$$

$$10K < R2 < 1M$$

$$1000pF < C < 10uF$$

On the Max7k Project Board, C = 1uF, R2 = 1MΩ. R1 consists of both a fixed and variable resistor; R1 = 430Ω + 1MΩ potentiometer.

2.4 JTAG_IN Header

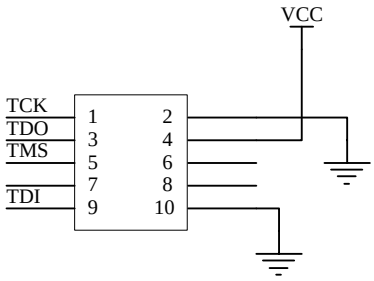
The JTAG header is where the ByteBlaster or BitBlaster is connected to the project board for programming. The Altera data book specifies how the JTAG connections are to be made to the Altera device:

TABLE 2. JTAG Header Connections

JTAG PIN	Signal	Description
1	TCK	Clock Signal
2	GND	Signal Ground
3	TDO	Data from Device
4	VCC	Power Supply
5	TMS	JTAG state machine control
6	NC	No connect
7	NC	No connect
8	NC	No connect
9	TDI	Data0
10	GND	Signal Ground

The following table gives the purpose of each pin on the JTAG header and the following figure shows the header with the connections.

FIGURE 3. JTAG Header



2.5 Prototyping Headers

TABLE 3. Header 1 Pin Connections

HOLE NUMBER	SIGNAL /PIN	HOLE NUMBER	SIGNAL/ PIN
1	75	2	76
3	77	4	NC
5	79	6	80
7	81	8	NC
9	83	10	84
11	1	12	2
13	NC	14	4
15	5	16	6
17	NC	18	8
19	9	20	10
21	11	22	NC
23	12	24	NC
25	NC	26	15
27	16	28	17
29	18	30	NC
31	20	32	21
33	22	34	NC
35	24	36	25
37	NC	38	27
39	28	40	29
41	30	42	31
43	NC	44	NC

Note: NC indicates No Connect.

TABLE 4. Header 2 Pin Connections

HOLE NUMBER	SIGNAL/PIN	HOLE NUMBER	SIGNAL/PIN
1	33	2	34
3	35	4	36
5	37	6	NC
7	39	8	40
9	41	10	NC
11	NC	12	44
13	45	14	46
15	NC	16	48
17	49	18	50
19	51	20	52
21	NC	22	NC

TABLE 5. Header 3 Pin Connections

HOLE NUMBER	SIGNAL/PIN	HOLE NUMBER	SIGNAL/PIN
1	54	2	55
3	56	4	57
5	58	6	NC
7	60	8	61
9	NC	10	63
11	64	12	65
13	NC	14	67
15	68	16	69
17	70	18	NC
19	NC	20	73
21	74	22	NC

2.6 Push-buttons

The push-buttons are 6mm momentary tact switches. The board is equipped for 4-hole or 5-hole switches. The fifth hole is for an optional ground pin for ESD protection. The signals from the push-button are pulled up with 1k resistors. The resistors used are on the same resistor array used by the JTAG connector. PB2 is connected to pin 1 of the Altera device, which is a dedicated global clear input. PB1 is connected to pin 40, a general purpose I/O pin.

TABLE 6. Push-Buttons

Button Number	Signal /Pin
PB1	40
PB2	1/ GCLR

2.7 DIP Switches

An 8-DIP switch array is available. The inputs are pulled up with 1kΩ resistors. A 10-pin (9-resistor) array is needed for these resistors.

TABLE 7. DIP Switches

Switch Number	1	2	3	4	5	6	7	8
Pin Number	44	45	46	48	49	50	51	52

2.8 LEDs

The UA7K contains 5 LEDs that are pulled-up with 330-Ω resistors. The LEDs are connected directly to the EPM7128S device. Each LED can be illuminated by driving the connected I/O pin with a logic 0. Table 8 shows the I/O pin for each LED.

FIGURE 4. LED Positions

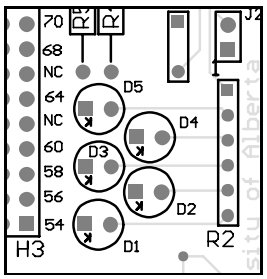


TABLE 8. LED Connections

LED #	**Pin**
1	54
2	55
3	56
4	57
5	58

3.0 Device Programming

To program the device with a design, the user needs a PC, ByteBlaster or BitBlaster cable, the MaxPlusII software, and the UA7K and power supply.

3.1 MAXPLUS2 Software

To program the UA7K board the user must be familiar with the use of the Altera MaxPlusII software package.

To program the board, do the following:

- run the “Programmer” tool, which is part of MaxPlusII.
- select “JTAG” In the menu at the top of the screen.
- make sure that “Multi-Device JTAG Chain” is checked off
- click on “Multi-Device JTAG Chain Setup...” to bring up its dialog box
- ensure that “EPM7128S” is selected under **Device Name:**
- click the “Select Programming File” button to bring up a file browsing dialog box
- search for your .pof file, which is created by the compile tool, and press **OK**
- click **Add** to add your file to the device programming list

- ensure that only one file is in the list by deleting any other files that are there
- make sure your project board is powered up, then click on “Detect JTAG Info”. It should confirm successfully.
- press **OK**. You will be taken back to the “Programmer” window.
- Press **Program** to start the operation.

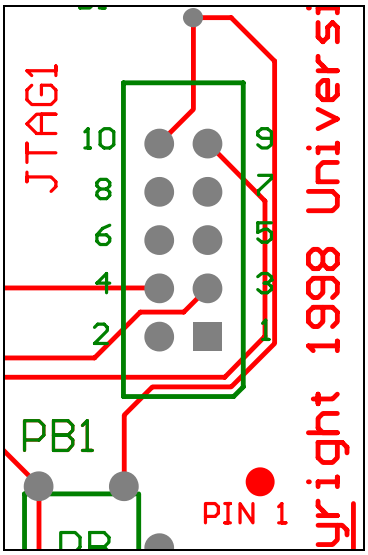
The most common thing to go wrong during this operation is to fail when trying to “Detect JTAG Info”. Possible causes of this are:

- JTAG cable not connected
- board not powered up
- more than one file selected in the device programming list
- software version not capable or licensed for programming (try a different version)

3.2 JTAG Connector

The Altera ByteBlaster cable has a polarized plug that cannot be inserted backwards into the JTAG header. The BitBlaster, however, does not have this polarized plug. (and home-made cables may not have it, either). In this case, pin 1 of the header is marked at the lower right corner of the header as shown in the picture below. On a ribbon cable the red line on one side of the cable denotes pin one. The figure below shows the PCB and the location of pin 1.

FIGURE 5. JTAG Connector



4.0 Board Configuration Options (Jumpers)

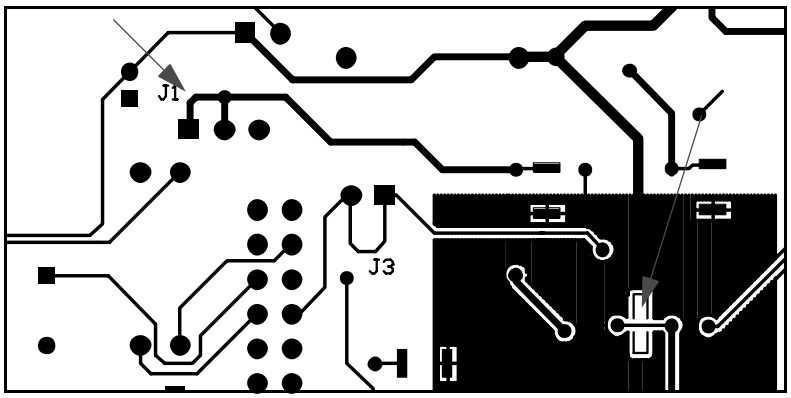
4.1 Modification Note

All of the modifications described below can be done with an exacto knife. After the modification is done a jumper block and a jumper can be installed to get the board back to the original mode of operation.

4.2 3.3V / 5V Operation

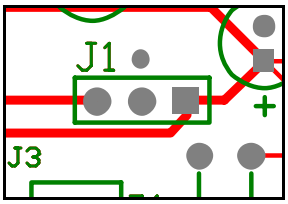
4.2.1 Modification

The board has been designed so that it can be easily modified to use a 3.3V and a 5V power supply. This mode is very useful when interfacing both 5V and 3.3V logic. There are 2 places that traces need to be cut so that the board can use multiple supply voltages. Cut the traces in the 2 spots indicated below. The trace that is labeled J1 is a trace that connects the 5V power supply to the 3.3V power supply on the board. This is done because most people will only use a single 5V power supply. The second place that needs modification is the trace in the power plane under the Max7128S device. This trace will disconnect the 5V power supply from the power plane and will cause the power plane to become a 3.3V power plane. This trace has been made easy to cut by surrounding it with a small rectangular box.



4.2.2 Jumper

A jumper now needs to be soldered into J1. Placing the jumper on the left will use the board at 3.3V. Putting the jumper on the right will cause the board to use only 5V. If a jumper is not put on and the modification was made then the MAX7128S device is not guaranteed to operate properly.



4.3 Potentiometer Bypass

Jumper 2 (J2) is intended to be used if the Pot is not populated and needs to be installed if the relaxation oscillator is used without the pot. This just removes the pot from the circuitry and allows the oscillator to operate at a fixed frequency determined by the capacitor and resistor on the board.

4.4 Oscillator Isolation

Global clock pins GCLK1 and GCLK2 are by default connected to oscillators located on the project board. GCLK1 is connected to an RC relaxation oscillator, and GCLK2 is con-

nected to a crystal oscillator. Both connections are routed through jumpers. The jumpers, by default, are shorted by traces on the PCB. Both oscillators may be effectively removed by cutting the traces between the jumper pins. GCLK1 can be isolated by cutting the trace between the holes for jumper 3 (J3). GCLK2 can be isolated by cutting the trace between the holes for jumper 4 (J4).

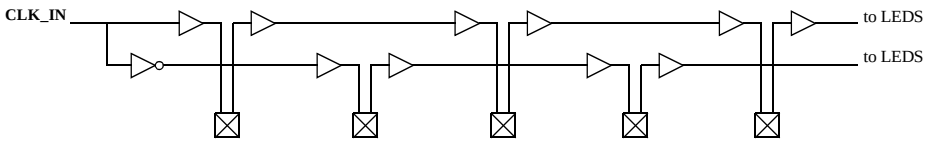
If so desired, the oscillators may be re-connected by soldering the connection where the trace was cut, or by inserting a 2-pin header and an appropriate jumper.

5.0 Board Testing

An test has been created to verify that the UA7K board is working properly.

The test verifies that the DIP switches and push-buttons work properly, the LEDs work, and that both the RC and crystal oscillators are functioning.

The general-purpose I/O pins are also tested, because the clock signal is routed all the way around the chip. The pins are configured in VHDL as *inout* pins. The test signal is output to a given pin, then that same pin is used as an input to the next pin in the chain. Two chains are used in order to detect solder bridges between adjacent pins, as in the schematic below:

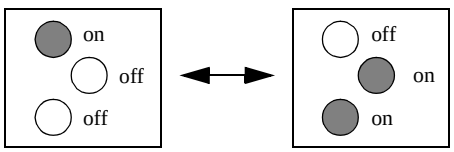


The two signal paths leapfrog over each other so that a solder bridge between adjacent I/O pins will cause one or both of the signals to go out of phase, disrupting the flashing LEDs.

5.1 Test Description

The behavior of the test is as follows:

1. A clock signal is created from the XOR of the crystal and RC oscillators. The crystal is clock divided by 8 million first, so that it is roughly 1 Hz (if the crystal is present, of course). When the RC oscillator frequency is adjusted properly, the clock signal appears to be fairly random.
2. LEDs 3 to 5 flash according to the clock signal. The pattern is shown below:



3. When PB2 or DIP switch 1 to 4 is toggled, LED 1 changes.
4. When pin 83, PB1, or DIP switch 5 to 8 is toggled, LED 2 changes.

5.2 Test Procedure

To run the test, do the following:

1. Locate the programming file for the test (check the UA7K web page)
2. Power the board on and program it. If this doesn't work with this particular board (i.e. you can program other boards) the JTAG connections could be broken, or the chip could be blown.
3. Adjust the potentiometer for the RC oscillator. You should be able to adjust the frequency such that the clock signal appears random (it is an XOR of two clocks). If there is no change, the RC oscillator is not working.
4. Verify that LEDs 3 to 5 are flashing as described above. If they are flashing improperly there is probably a solder bridge between pins or an I/O pin is stuck at a 0 or 1.
5. Toggle all DIP switches and pushbuttons. LED 1 or LED2 should change, depending on what you have pressed.

That's it for the test; go on to the next board!

6.0 MAX7032S (44-pin) Device

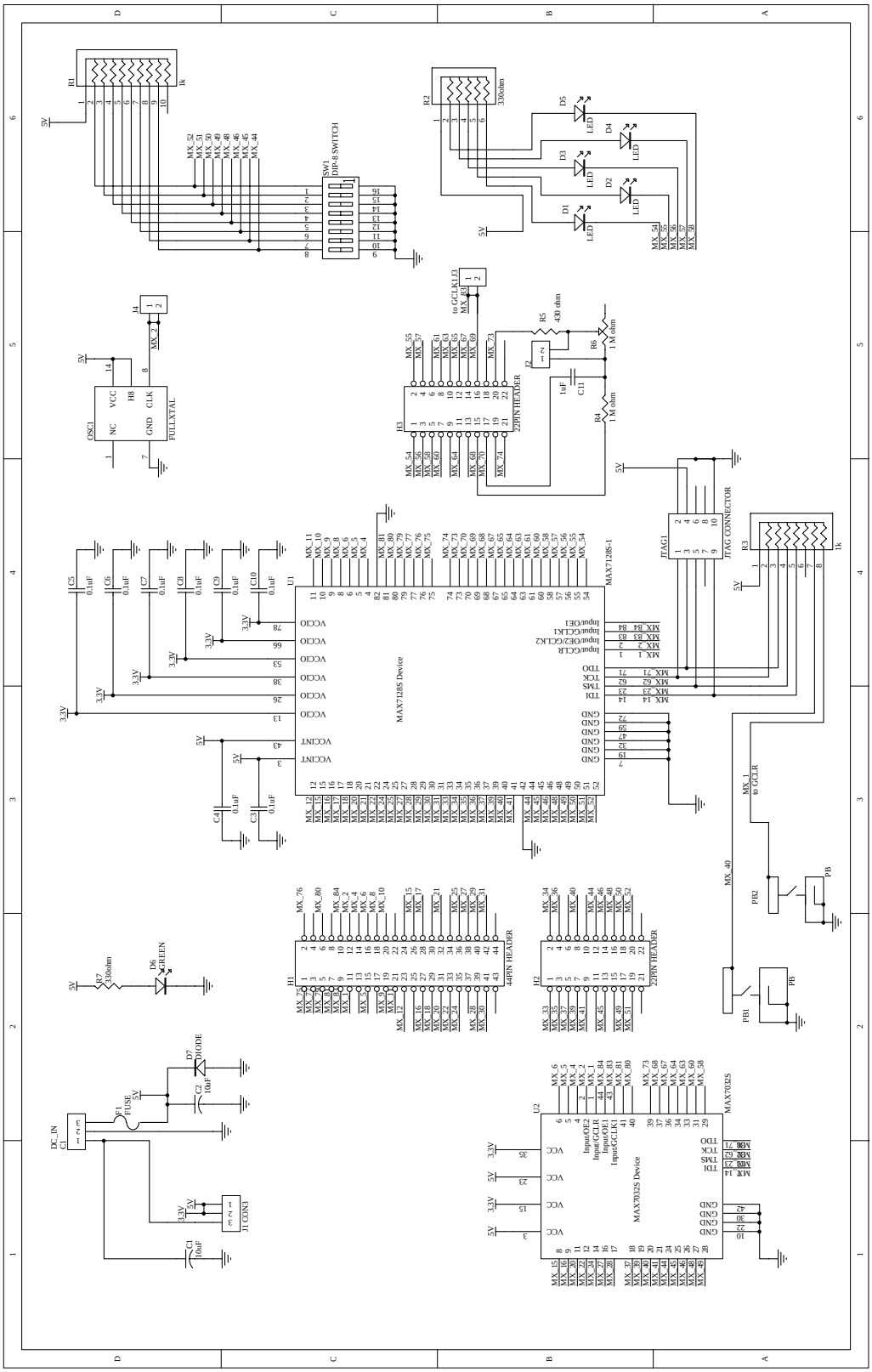
The footprint for the 44-pin device is inside the footprint for the 84-pin device. The table below gives the connections between the 84-pin footprint and the 44-pin footprint. The connections are also shown on the schematic diagram.

TABLE 9. 44Pin Device Pin Connections

84 Pin FP	44 Pin FP	84 Pin FP	44 Pin FP
15	8	16	9
20	11	22	12
24	14	27	16
28	17	37	18
39	19	40	20
41	21	44	24
45	25	46	26
48	27	49	28
6	6	5	5
4	4	2	2
1	1	84	44
83	43	81	41
80	40	73	39
68	37	67	36
64	34	63	33
60	31	58	29

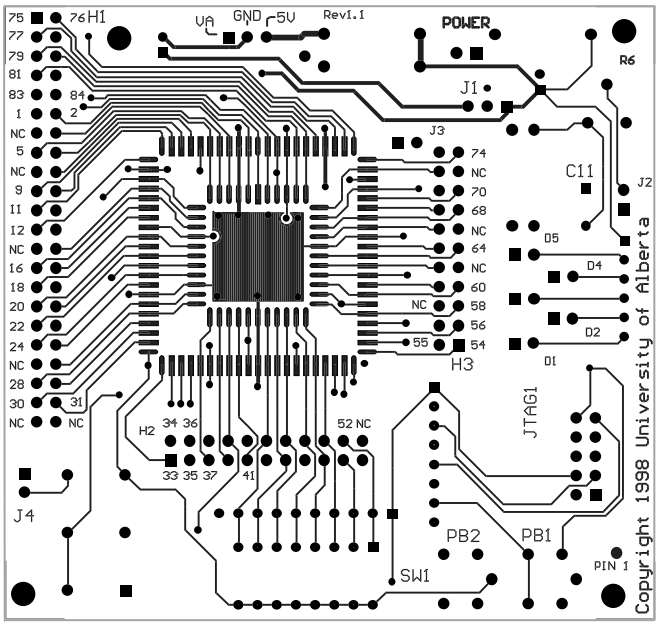
7.0 Board Schematics and PCB Images

7.1 Schematic

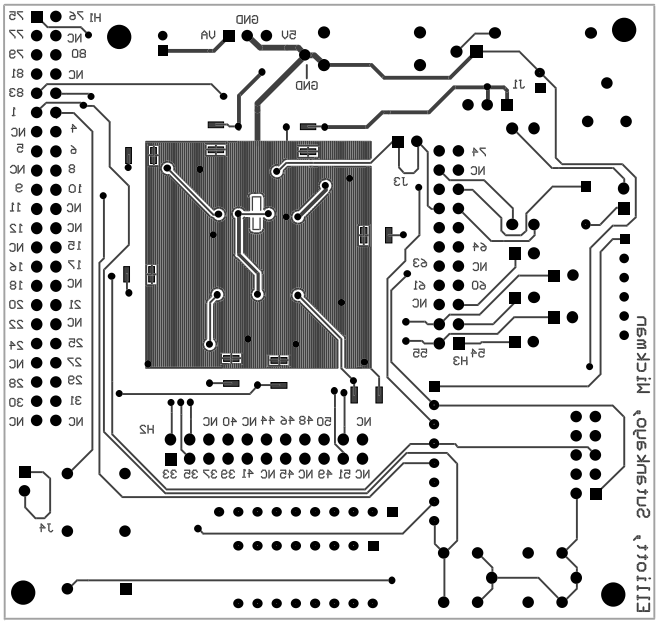


7.2 Top View

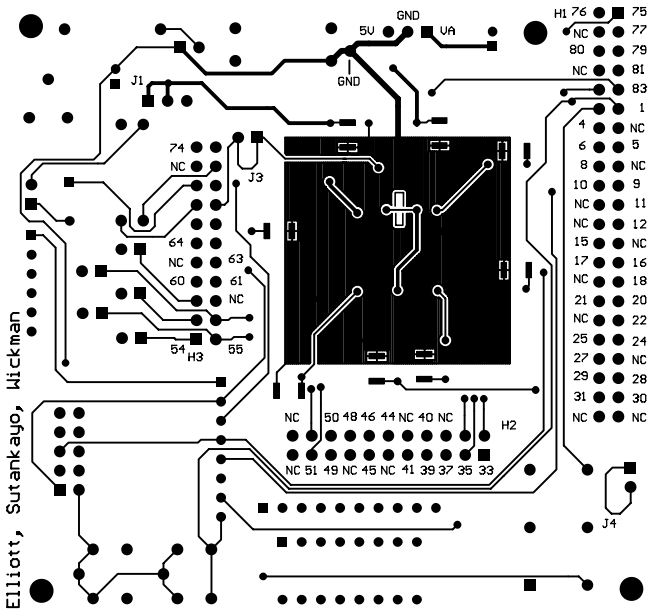
7.2.1 Top PCB



7.2.2 Bottom PCB



7.3 Bottom View



7.4 Top PCB with SilkScreen