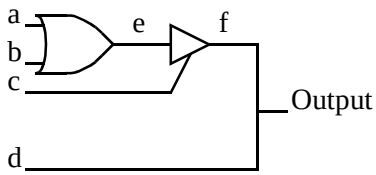
## Question 2: [ /10]

The outputs of the gates below are strongly driven. The three-state driver enable signal (*c*) is active high.




Using the IEEE 1164 VHDL std_logic signal values ( U X 0 1 Z W L H - ), resolution function and logic truth tables, complete the following partial truth table for the above circuit. Record *f* as the value that would be observed if this signal was not connected to another to form the *output*.

| *a* | *b* | *c* | *d* | *e* | *f* | *Output* |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | **0** | **Z** | **0** |
| 1 | 0 | 0 | 0 | | | |
| U | 0 | 0 | 0 | | | |
| H | 0 | 1 | Z | | | |
| Z | 1 | 1 | Z | | | |
| 0 | Z | 1 | Z | | | |
| L | 0 | 1 | Z | | | |
| 1 | 1 | - | Z | | | |
| 1 | 1 | 1 | 1 | | | |
| 1 | 1 | 1 | H | | | |
| L | 1 | U | Z | | | |
| 1 | 1 | 1 | 0 | | | |
| X | 1 | 1 | L | | | |
| 0 | 1 | X | U | | | |
| 1 | 1 | 1 | - | | | |
| H | H | W | H | | | |
| L | L | W | L | | | |
| W | 1 | X | 1 | | | |
| Z | Z | Z | Z | | | |
| 1 | 0 | 1 | U | | | |
| 0 | 0 | - | L | | | |

## Question 2: [ /10]

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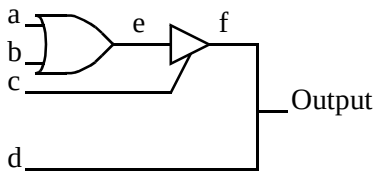


Using the IEEE 1164 VHDL std_logic signal values ( U X 0 1 Z W L H - ), resolution function and logic truth tables, complete the following partial truth table for the above circuit. Record *f* as the value that would be observed if this signal was not connected to another to form the *output*.

| *a* | *b* | *c* | *d* | *e* | *f* | *Output* |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | **0** | **Z** | **0** |
| 1 | 0 | 0 | 0 | | | |
| U | 0 | 0 | 0 | | | |
| H | 0 | 1 | Z | | | |
| Z | 1 | 1 | Z | | | |
| 0 | Z | 1 | Z | | | |
| L | 0 | 1 | Z | | | |
| 1 | 1 | - | Z | | | |
| 1 | 1 | 1 | 1 | | | |
| 1 | 1 | 1 | H | | | |
| L | 1 | U | Z | | | |
| 1 | 1 | 1 | 0 | | | |
| X | 1 | 1 | L | | | |
| 0 | 1 | X | U | | | |
| 1 | 1 | 1 | - | | | |
| H | H | W | H | | | |
| L | L | W | L | | | |
| W | 1 | X | 1 | | | |
| Z | Z | Z | Z | | | |
| 1 | 0 | 1 | U | | | |
| 0 | 0 | - | L | | | |