

Fingerprint Sensor - Serial Communication

ECE492 – Winter 2014 - Group 9

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Introduction

Initially, we had trouble sourcing an affordable fingerprint sensor for our design project. We stumbled across a fingerprint on adafruit that seemed to fit the bill. It is the ZFM-20 series sensor from ZhianTec.

Connectivity

The device can be powered by and communicate with the DE2 without additional hardware. The provided Buffered FIFO JTAG UART (RS-232) can be used for communication. Originally we utilized the JTAG UART in the provided university IP, but ran into issues with RX buffer overflowing. A hardware buffered solution alleviates these issues. The sensor can be powered by the 5V pin on the DE2 GPIO header.


Communication

There is source code to accompany this application note (ZFMComm.h, ZFMComm.cpp & ZFM_CONST.h). These files can be imported into the NIOS-II environment and compiled with g++.

Usage is available in doxygen style comments in the code.

Example

There is an example of the usage attached to this document and available at <http://github.com/berickson1/DE2-Adafruit-ZFM-20>



FIFOed UART (RS-232 serial port)9.3.0
 fifoed_avalon_uart

Documentation

Block Diagram

Show signals

- s1_clock
- s1_clock_res
- g1
- s1

Parameters

clock_freq:

Configuration/Baud Rate

Baud Rate (bps):

Fixed baud rate (no software control)

Configuration

data bits:

parity:

stop bits:

Configuration/Flow Control

Include CTS/RTS pins and control register bits

Configuration/Streaming Data (DMA) control

Include end-of-packet register

Simulation

Simulated transmitter Baud Rate:

Simulated RXD-input character stream:

TX FIFO usage

Include transmit FIFOs

TX FIFO depth (words):

Build FIFOs from LEs

TX IRQ Threshold (words):

RX FIFO usage

Include receive FIFOs

RX FIFO depth (words):

Build FIFOs from LEs

RX IRQ Threshold (words):

Enable Rx Timeout

Timeout in Character periods:

Enable Rx Gap detection

Timeout in Character periods:

Enable Timestamp register

Use external logic for timestamp. Internal is the baudrate/8

Width of timestamp fifo and register:

Enable PE, FE, BRK, ROE, GAP, RxEMPTY fifo data

Driver: Pass error bits with data bits.

FIFO Exorts

Export FIFO used signals

MISC

Connect the IRQ to the avalon fabric

Create hardware CTS input (only valid with fifos)

Create hardware which asserts only when uart is transmitting. usefull for RS485

Additional References

Datasheet - Attached