

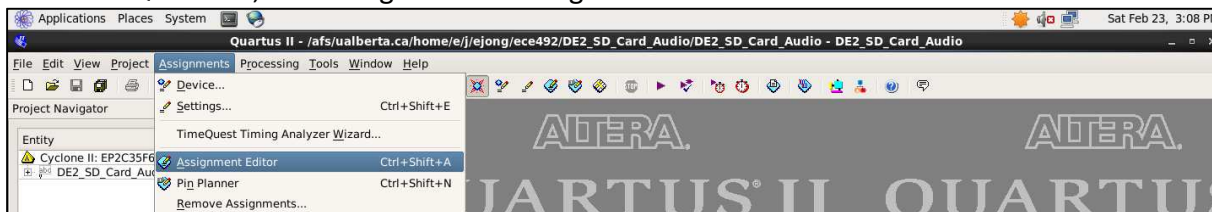
Application Note – GPIO Internal Pull-Up Resistor

System: Quartus II V10.1 with Altera DE2 FPGA board

Description: The DE2 board provides a weak, internal pull-up resistor for all GPIO pins. Enabling it saves you from having to use external resistors for your project circuitry. The internal resistor is about 25 kΩ but will vary. Please note that the Bus Hold option for tri-stated pins must be OFF if you want to use the internal pull-up.

Steps:

- In Quartus II, click Assignments > Assignment Editor



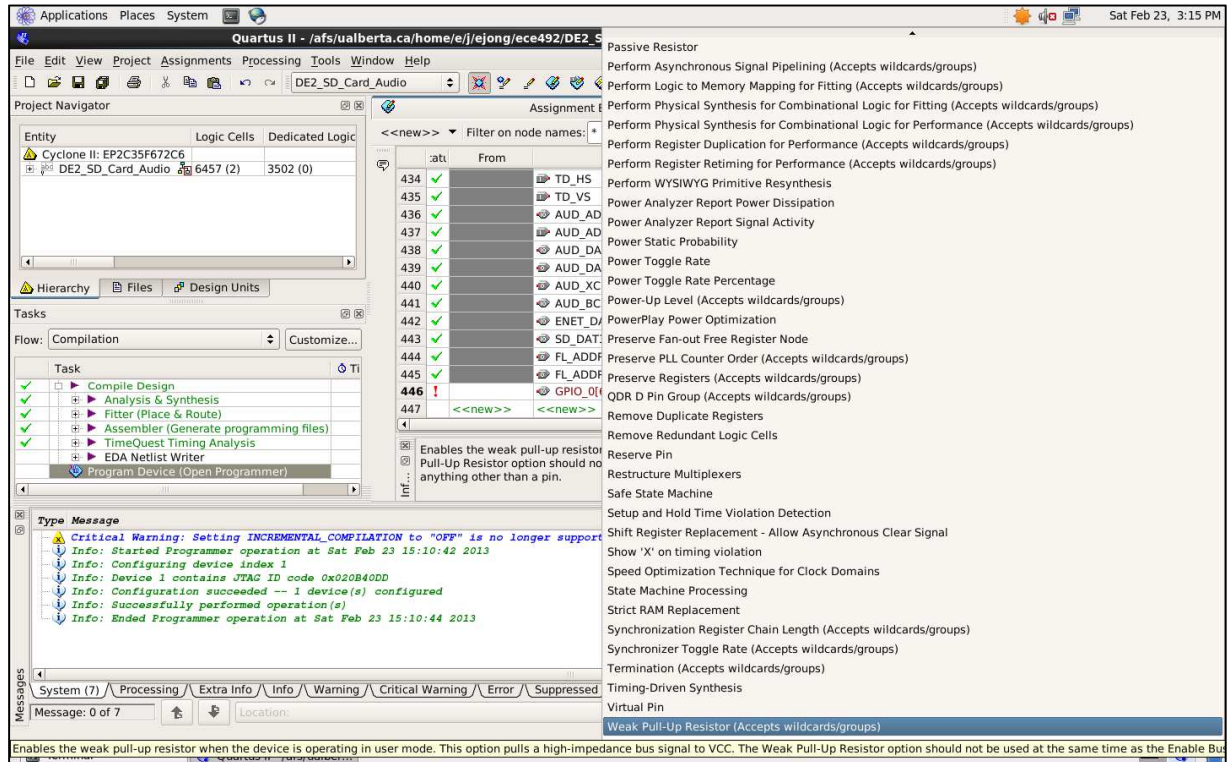
- This shows all your component pins

.atu	From	To	Assignment Name	Value	Enabled
350	✓	SD_CMD	Location	PIN_Y21	Yes
351	✓	SD_CLK	Location	PIN_AD25	Yes
352	✓	GPIO_0[0]	Location	PIN_D25	Yes
353	✓	GPIO_0[1]	Location	PIN_J22	Yes
354	✓	GPIO_0[2]	Location	PIN_E26	Yes
355	✓	GPIO_0[3]	Location	PIN_E25	Yes
356	✓	GPIO_0[4]	Location	PIN_F24	Yes
357	✓	GPIO_0[5]	Location	PIN_F23	Yes
358	✓	GPIO_0[6]	Location	PIN_J21	Yes
359	✓	GPIO_0[7]	Location	PIN_J20	Yes

- Scroll to the bottom and double-click <<new>> under “To”
- Type in the name of your GPIO pin

.atu	From	To	Assignment Name	Value	Enabled
434	✓	TD_HS	I/O Standard	3.3-V LVTTTL	Yes
435	✓	TD_VS	I/O Standard	3.3-V LVTTTL	Yes
436	✓	AUD_ADCLRCK	I/O Standard	3.3-V LVTTTL	Yes
437	✓	AUD_ADCCDAT	I/O Standard	3.3-V LVTTTL	Yes
438	✓	AUD_DACLCK	I/O Standard	3.3-V LVTTTL	Yes
439	✓	AUD_DACDAT	I/O Standard	3.3-V LVTTTL	Yes
440	✓	AUD_XCK	I/O Standard	3.3-V LVTTTL	Yes
441	✓	AUD_BCLK	I/O Standard	3.3-V LVTTTL	Yes
442	✓	ENET_DATA[0]	I/O Standard	3.3-V LVTTTL	Yes
443	✓	SD_DAT3	I/O Standard	3.3-V LVTTTL	Yes
444	✓	FL_ADDR[20]	I/O Standard	3.3-V LVTTTL	Yes
445	✓	FL_ADDR[21]	I/O Standard	3.3-V LVTTTL	Yes
446	!	GPIO_0[6]			Yes
447		<<new>>	<<new>>		

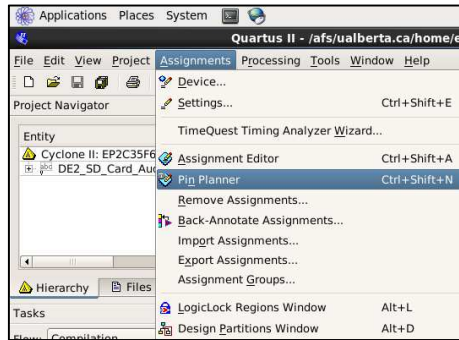
- Double-click the blank space under “Assignment Name”
- Scroll down and click on “Weak Pull-Up Resistor (Accepts wildcards/groups)”



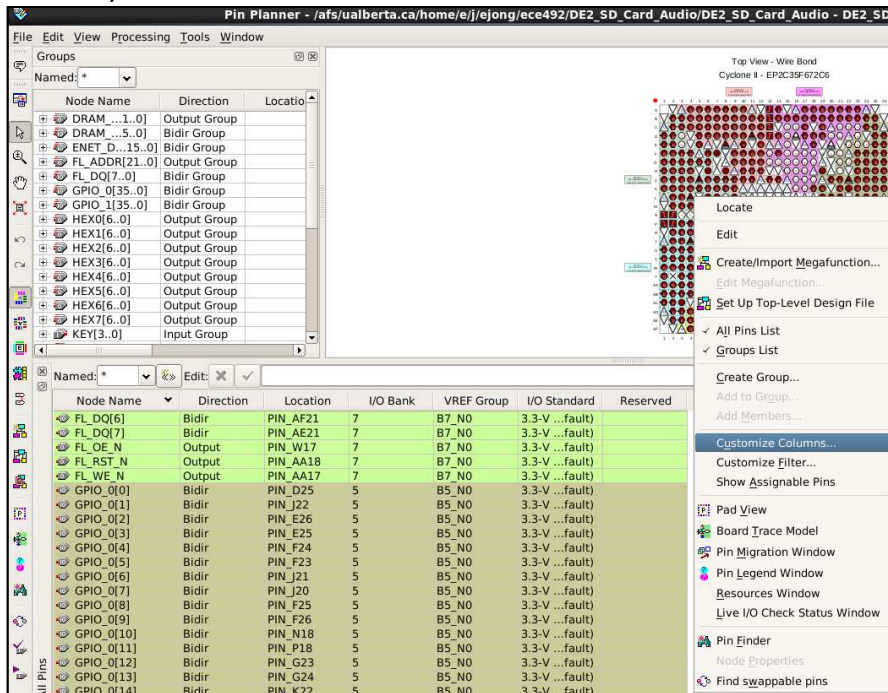
- Click and change “Value” to On
- “Enabled” should be Yes by default
- Ensure that the name listed under “Entity” is your top level

Pin	From	To	Assignment Name	Value	Enabled	Entity
434		TD_HS	I/O Standard	3.3-V LVTTTL	Yes	
435		TD_VS	I/O Standard	3.3-V LVTTTL	Yes	
436		AUD_ADCLRCK	I/O Standard	3.3-V LVTTTL	Yes	
437		AUD_ADCDATA	I/O Standard	3.3-V LVTTTL	Yes	
438		AUD_DACLK	I/O Standard	3.3-V LVTTTL	Yes	
439		AUD_DACDATA	I/O Standard	3.3-V LVTTTL	Yes	
440		AUD_XCK	I/O Standard	3.3-V LVTTTL	Yes	
441		AUD_BCLK	I/O Standard	3.3-V LVTTTL	Yes	
442		ENET_DATA[0]	I/O Standard	3.3-V LVTTTL	Yes	
443		SD_DAT3	I/O Standard	3.3-V LVTTTL	Yes	
444		FL_ADDR[20]	I/O Standard	3.3-V LVTTTL	Yes	
445		FL_ADDR[21]	I/O Standard	3.3-V LVTTTL	Yes	
446		GPIO_0[6]	Weak Pull-Up Resistor	Off	Yes	DE2_S...Audio
447	<<new>>	<<new>>	<<new>>	Off		
				On		

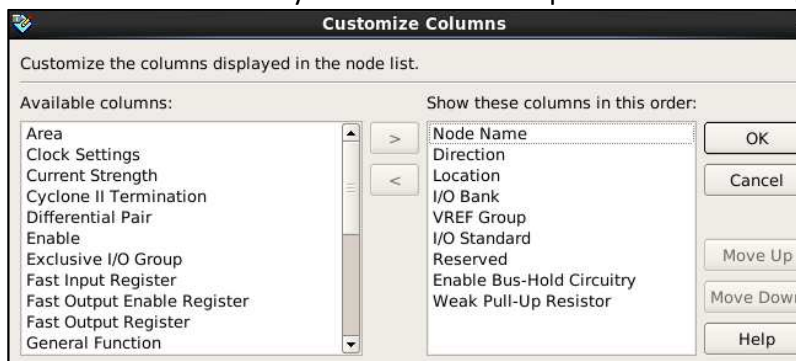
- Done! You can review your edits under Pin Planner in Quartus II



- Right-click anywhere and select “Customize Columns...”



- Move “Enable Bus-Hold Circuitry” and “Weak Pull-Up Resistor” to the right window



- Ensure the bus-hold isn't ON if your internal resistor is (should be OFF by default)
- You can also set your resistors(s) here and see it reflected in “Assignment Editor”

The screenshot shows the Assignment Editor interface. On the left, a list of nodes is displayed with columns for Node Name, Direction, and Location. On the right, a detailed view of the I/O pin configuration for GPIO_0[4] is shown, including a grid of pins and a table of pin assignments.

Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved	Enable Bus-Hold Circuitry	Weak Pull-Up Resistor
GPIO_0[4]	Bidir	PIN_F24	5	B5_NO	3.3-V ...fault)			
GPIO_0[5]	Bidir	PIN_F23	5	B5_NO	3.3-V ...fault)			
GPIO_0[6]	Bidir	PIN_J21	5	B5_NO	3.3-V ...fault)			On
GPIO_0[7]	Bidir	PIN_J20	5	B5_NO	3.3-V ...fault)			

Example multimeter readings with a simple on/off switch:

- Power supply from GPIO pin 29: 3.310 vdc
- GPIO pin without internal resistor: 1.071 vdc
- GPIO pin with internal resistor: 3.072 vdc

References:

1. <http://www.altera.com/support/devices/io/features/io-features.html#ProgrammablePullupResistor>

Programmable Pull-up Resistor

When to Use

- Use when there is a need to pull a pin signal level to V_{CCIO} when it is tri-stated.
- Use to replace a weak external pull-up resistor. The pull-up resistance varies with process, voltage, and temperature conditions.
- Use external components if you require precision values.
- Use in combination with open-drain output option.

How to Use

- In the Assignment Editor, set the weak pull-up assignment to ON to enable the on-chip pull-up resistor for the pin.

Feature Availability

- All user I/Os.


Feature Limitations

- Not supported in dedicated configuration pins and dedicated clock input pins.
- Not available in pins that are using bus hold option.

2. http://www.altera.com/literature/hb/cyc2/cyc2_cii5v1.pdf

Programmable Pull-Up Resistor

Each Cyclone II device I/O pin provides an optional programmable pull-up resistor during user mode. If you enable this feature for an I/O pin, the pull-up resistor (typically 25 kΩ) holds the output to the V_{CCIO} level of the output pin's bank.

 If the programmable pull-up is enabled, the device cannot use the bus-hold feature. The programmable pull-up resistors are not supported on the dedicated configuration, JTAG, and dedicated clock pins.

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Cyclone II Device Handbook, Volume 1

3. http://www.cs.columbia.edu/~%20sedwards/classes/2013/4840/DE2_schematics.pdf

