Tutorial of VGA Streaming

To display Strings and Pixels on the same screen, and using stream router, colour space converter to achieve grayscale display

Kwan Yin Lau and Jun Zhao (group 3)

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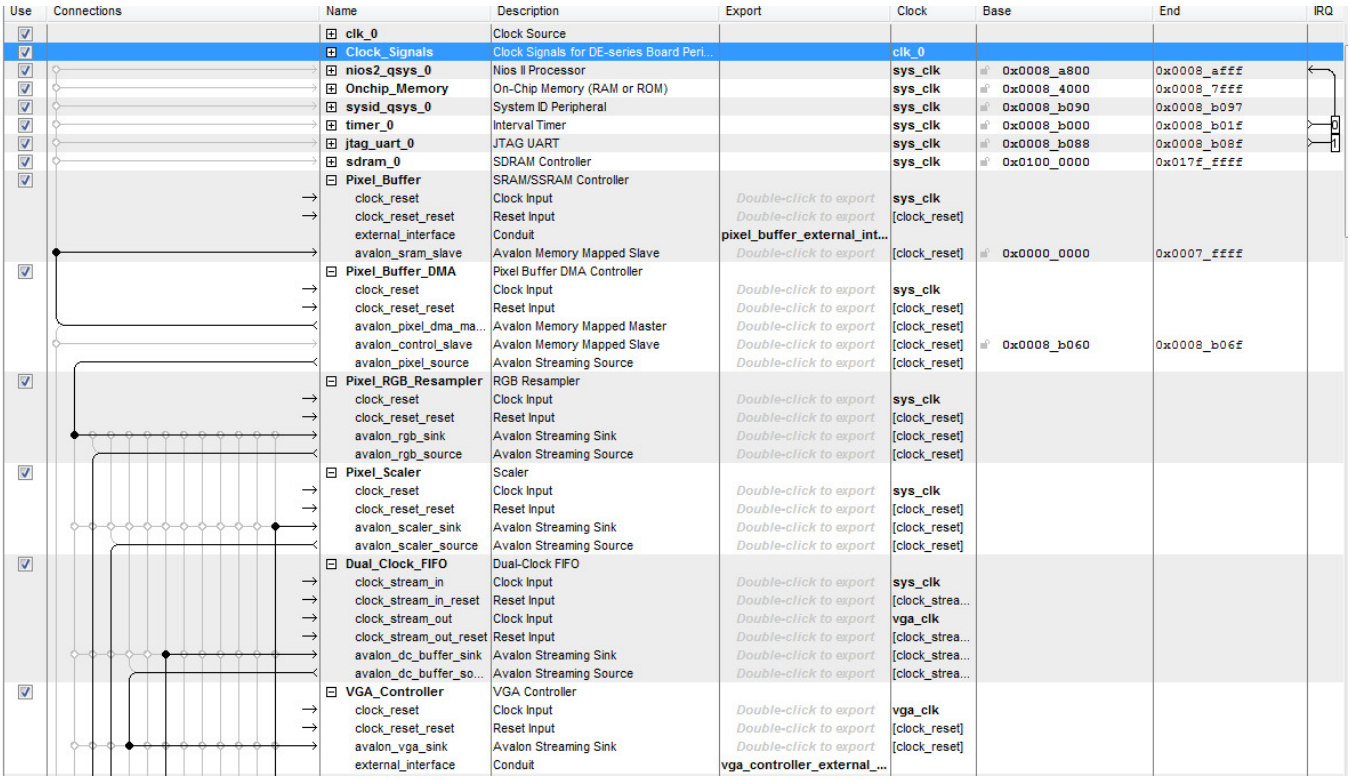
Introduction

This tutorial will demonstrate how to apply several University Program Video IP cores from Altera DE2 board in order to perform VGA streaming. This project could read a pixel frame from SRAM (or video if the input to SRAM is continuous). The main functionalities are to add strings on the same VGA screen with the pixel frame output, and also provide a run-time switch between colour display and grayscale display. The hardware and software components are modified from ECE 492 lab materials and Altera templates. The major University Program Video IP cores in this tutorial are Character Buffer for VGA Display, Alpha Blender, RGB Resampler, Colour-Space Converter and Video-Stream Router. For basic VGA pixel display setup, please refer to another appnote of our group.

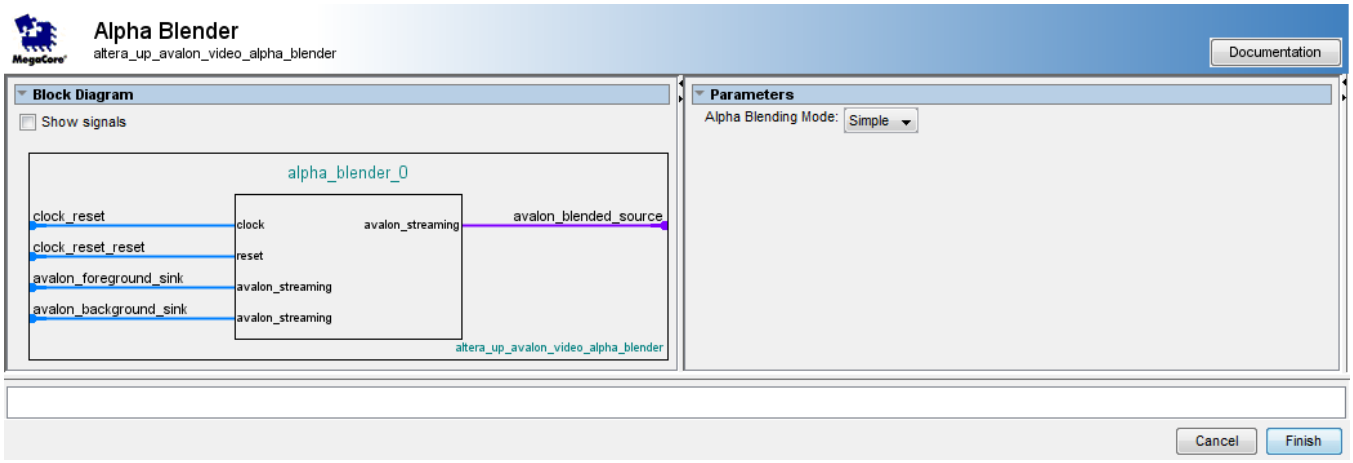
Procedure to display Strings and Pixels on the same screen

1. Please follow the steps in appnote “Tutorial of displaying pixels on VGA monitor” to build the basic VGA pixel stream first. You should have the following set up in Qsys. Noted that VGA needs another clock input, that can be generated from the core of Clock Signals for DE-series Board peripherals.

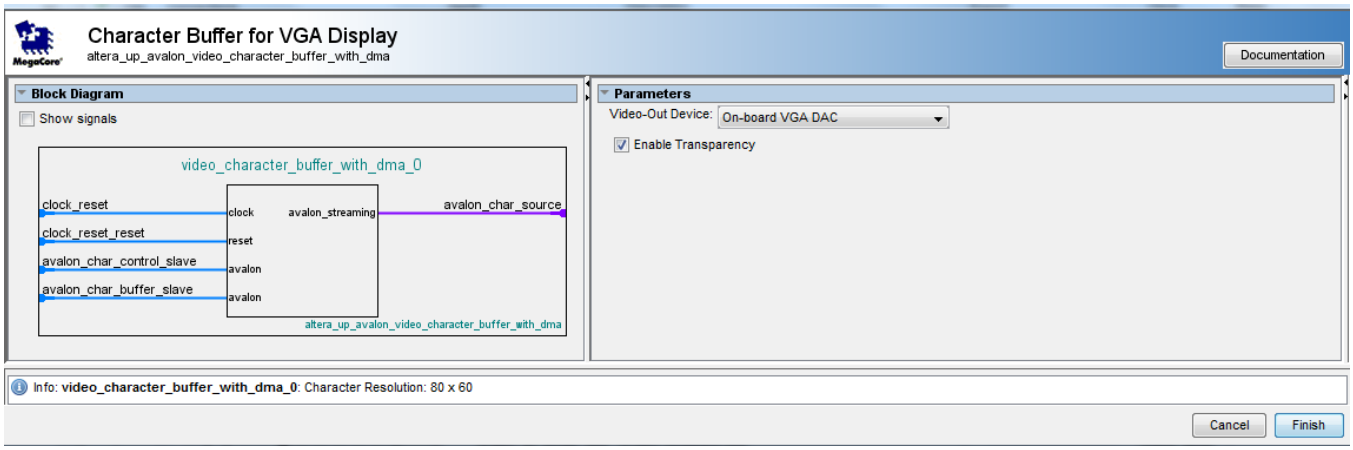


Use	Connections	Name	Description	Export	Clock	Base	End	IRQ
☑		clk_0	Clock Source					
☑		Clock_Signals	Clock Signals for DE-series Board Peri...		clk_0			
☑		nios2_qsys_0	Nios II Processor		sys_clk	0x0008_a800	0x0008_afff	
☑		Onchip_Memory	On-Chip Memory (RAM or ROM)		sys_clk	0x0008_4000	0x0008_7fff	
☑		sysid_qsys_0	System ID Peripheral		sys_clk	0x0008_b090	0x0008_b097	
☑		timer_0	Interval Timer		sys_clk	0x0008_b000	0x0008_b01f	0
☑		jtag_uart_0	JTAG UART		sys_clk	0x0008_b088	0x0008_b08f	1
☑		sdram_0	SDRAM Controller		sys_clk	0x0100_0000	0x017f_ffff	
☑		Pixel_Buffer	SRAM/SSRAM Controller					
	→	clock_reset	Clock Input	Double-click to export	sys_clk			
	→	clock_reset_reset	Reset Input	Double-click to export	[clock_reset]			
		external_interface	Conduit	pixel_buffer_external_int...				
		avalon_sram_slave	Avalon Memory Mapped Slave	Double-click to export	[clock_reset]	0x0000_0000	0x0007_ffff	
☑		Pixel_Buffer_DMA	Pixel Buffer DMA Controller					
	→	clock_reset	Clock Input	Double-click to export	sys_clk			
	→	clock_reset_reset	Reset Input	Double-click to export	[clock_reset]			
		avalon_pixel_dma_ma...	Avalon Memory Mapped Master	Double-click to export	[clock_reset]			
		avalon_control_slave	Avalon Memory Mapped Slave	Double-click to export	[clock_reset]	0x0008_b060	0x0008_b06f	
		avalon_pixel_source	Avalon Streaming Source	Double-click to export	[clock_reset]			
☑		Pixel_RGB_Resampler	RGB Resampler					
	→	clock_reset	Clock Input	Double-click to export	sys_clk			
	→	clock_reset_reset	Reset Input	Double-click to export	[clock_reset]			
		avalon_rgb_sink	Avalon Streaming Sink	Double-click to export	[clock_reset]			
		avalon_rgb_source	Avalon Streaming Source	Double-click to export	[clock_reset]			
☑		Pixel_Scaler	Scaler					
	→	clock_reset	Clock Input	Double-click to export	sys_clk			
	→	clock_reset_reset	Reset Input	Double-click to export	[clock_reset]			
		avalon_scaler_sink	Avalon Streaming Sink	Double-click to export	[clock_reset]			
		avalon_scaler_source	Avalon Streaming Source	Double-click to export	[clock_reset]			
☑		Dual_Clock_FIFO	Dual-Clock FIFO					
	→	clock_stream_in	Clock Input	Double-click to export	sys_clk			
	→	clock_stream_in_reset	Reset Input	Double-click to export	[clock_strea...			
	→	clock_stream_out	Clock Input	Double-click to export	vga_clk			
	→	clock_stream_out_reset	Reset Input	Double-click to export	[clock_strea...			
		avalon_dc_buffer_sink	Avalon Streaming Sink	Double-click to export	[clock_strea...			
		avalon_dc_buffer_so...	Avalon Streaming Source	Double-click to export	[clock_strea...			
☑		VGA_Controller	VGA Controller					
	→	clock_reset	Clock Input	Double-click to export	vga_clk			
	→	clock_reset_reset	Reset Input	Double-click to export	[clock_reset]			
		avalon_vga_sink	Avalon Streaming Sink	Double-click to export	[clock_reset]			
		external_interface	Conduit	vga_controller_external_...				

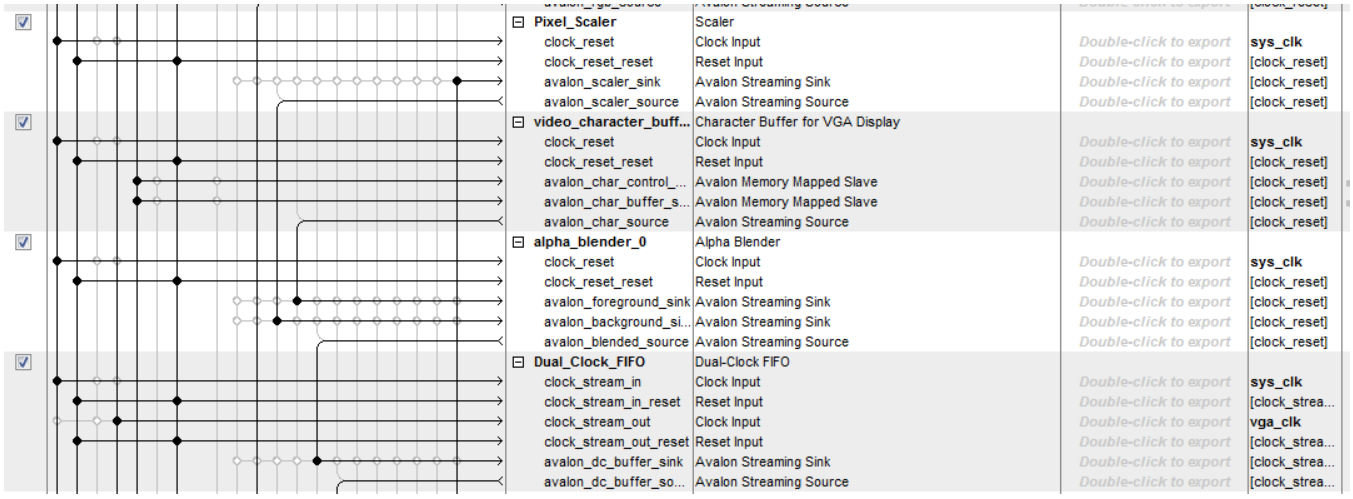
2. To display strings and pixels on the same screen, we need to add two components: the Character Buffer for VGA Display and Alpha Blender.



remember to check the Enable Transparency.



3. Connect the two components between Scalar and Dual-Clock FIFO as follows.The source of Scalar goes to background sink of alpha blender and the source of Character buffer goes to foreground sink of alpha blender.



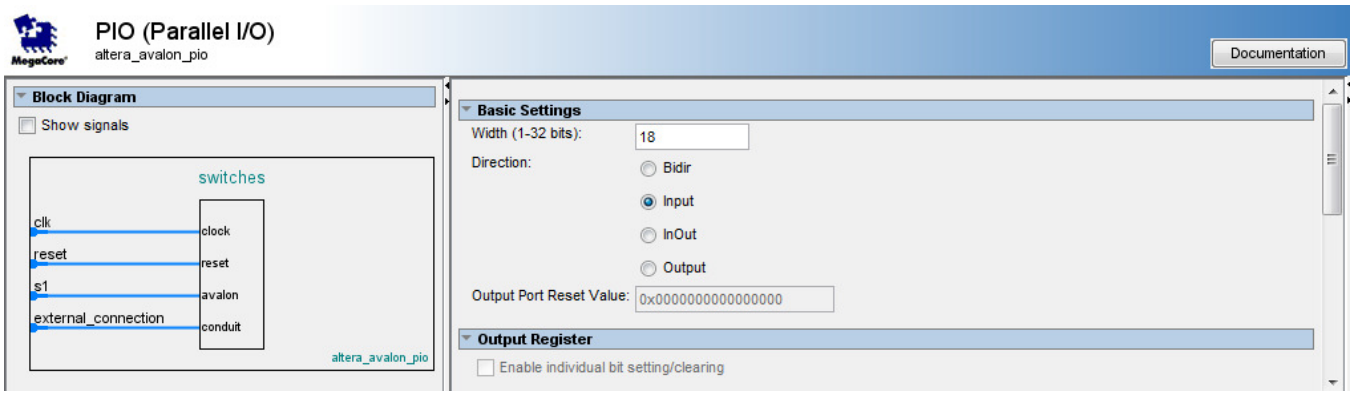
4. Nothing needed to add in the top level file. Just Generate and compile. Add the following code in your software:

```
#include "altera_up_avalon_video_character_buffer_with_dma.h"
alt_up_char_buffer_dev *char_buf_dev;
// Open the char buffer device
char_buf_dev = alt_up_char_buffer_open_dev(
      "/dev/video_character_buffer_with_dma_0");
if (char_buf_dev == NULL) {
      printf("Error: could not open char buffer device \n");
} else {
      printf("Opened char buffer device \n");
}
alt_up_char_buffer_init(char_buf_dev);
alt_up_char_buffer_clear(char_buf_dev);
alt_up_char_buffer_string(char_buf_dev, "A String in Char Buffer.", x, y);
```

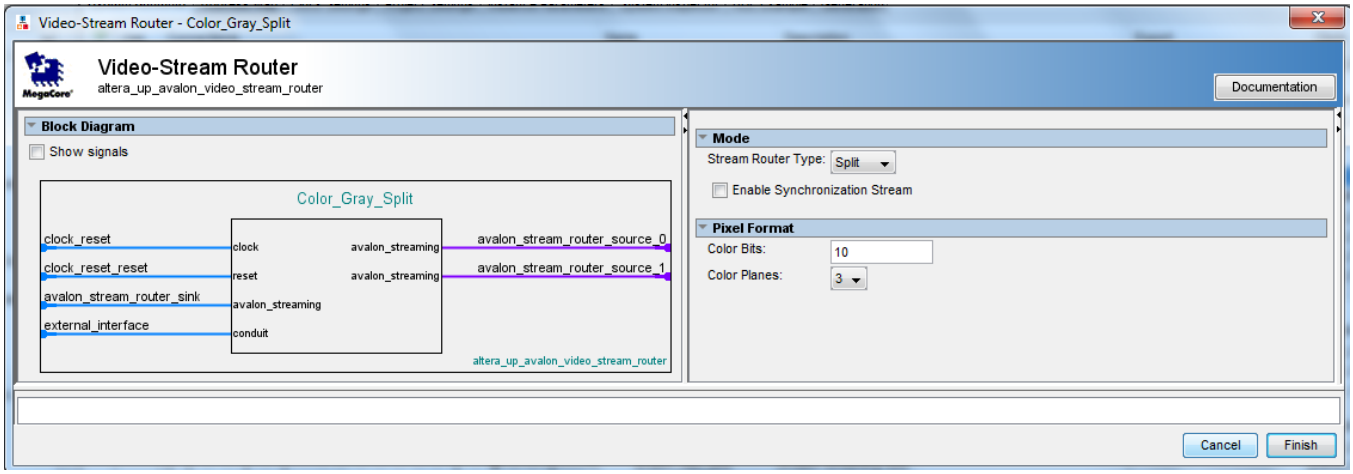
Noted that the string parameter passes into `alt_up_char_buffer_open_dev` `"/dev/video_character_buffer_with_dma_0"` must be the same with the component name you define in Qsys but not copied from system.h as usual.
Call `alt_up_char_buffer_string` with any strings you want to display together with x and y coordinates on the VGA screen.

Procedure to set up a run-time switch between colour display and grayscale display

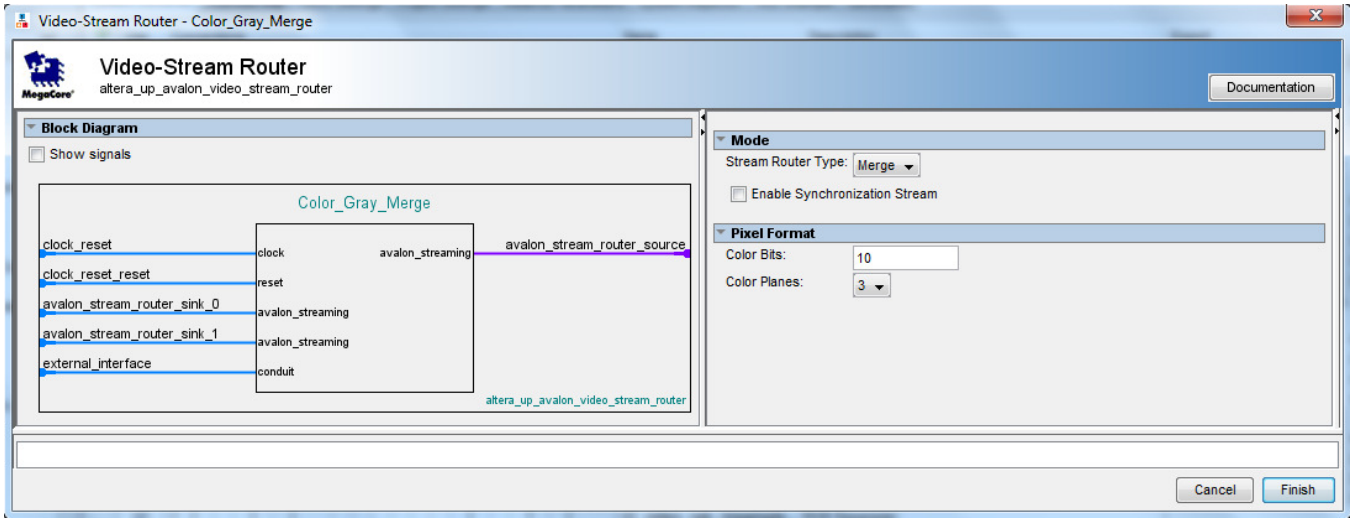
1. Start from the current VGA project. First add PIO for on board switches.



2. To implement the run-time switching between colour and grayscale display, we need a “MUX” and a “DEMUX” on the VGA avalon Stream with a select signal from a switch. The “MUX” and “DEMUX” can be implement with the Video-Stream Router core. So add two of them, one with split mode and one with merge mode.



when conduit signal is 0, input sink will output to source 0; when conduit signal is 1, input sink will output to source 1.



when conduit signal is 0, input sink 0 will output to source; when conduit signal is 1, input sink 1 will output to source.

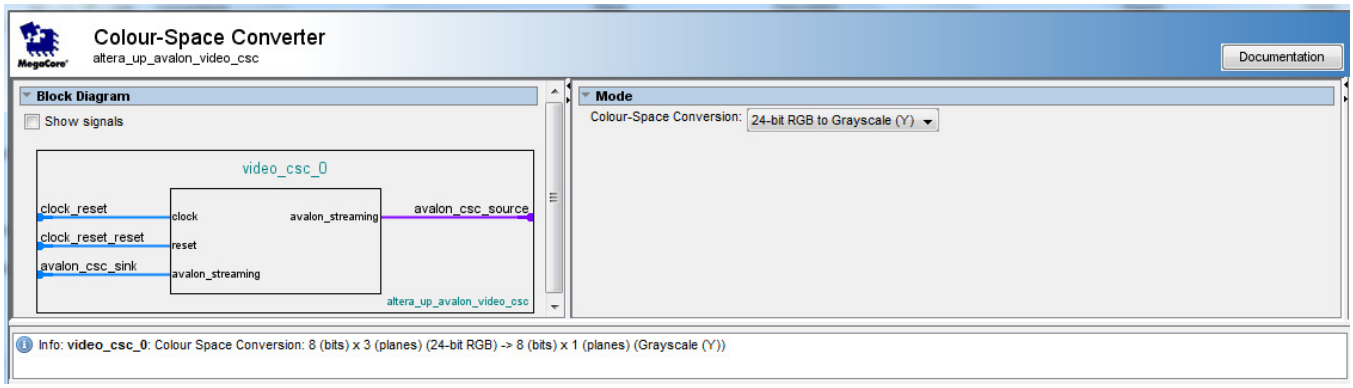
Then export both conduit signals for split and merge, lets use SW(0) to be the select signal, then modify the top level file as following:
declare an additional signal and connects it after BEGIN

```
signal SW_0 : std_logic;
SW_0 <= SW(0);
```

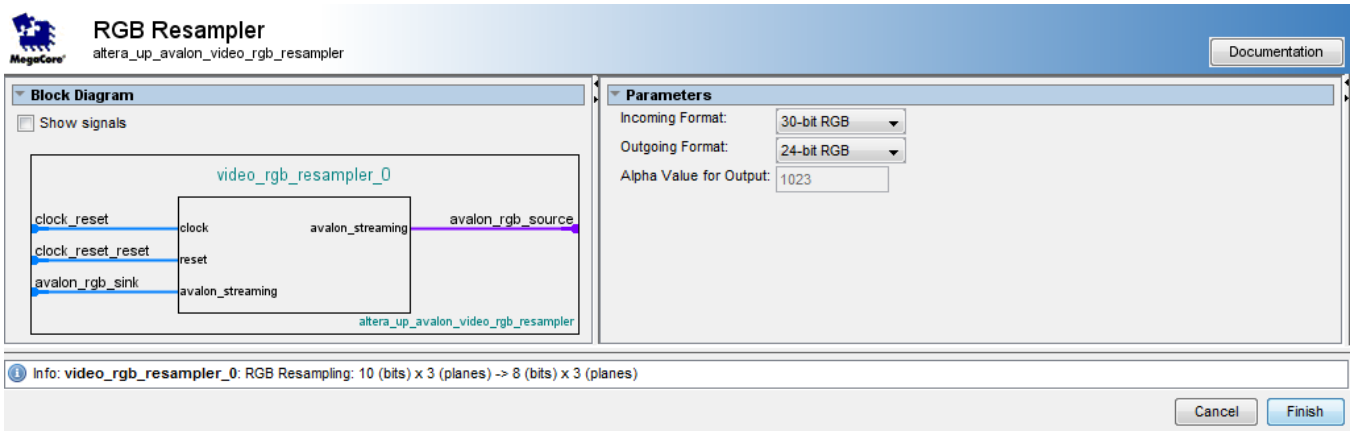
add these connections to port map

```
switches_external_connection_export(0)=> SW_0,
color_gray_merge_external_interface_export    => SW_0,
color_gray_split_external_interface_export    => SW_0,
```

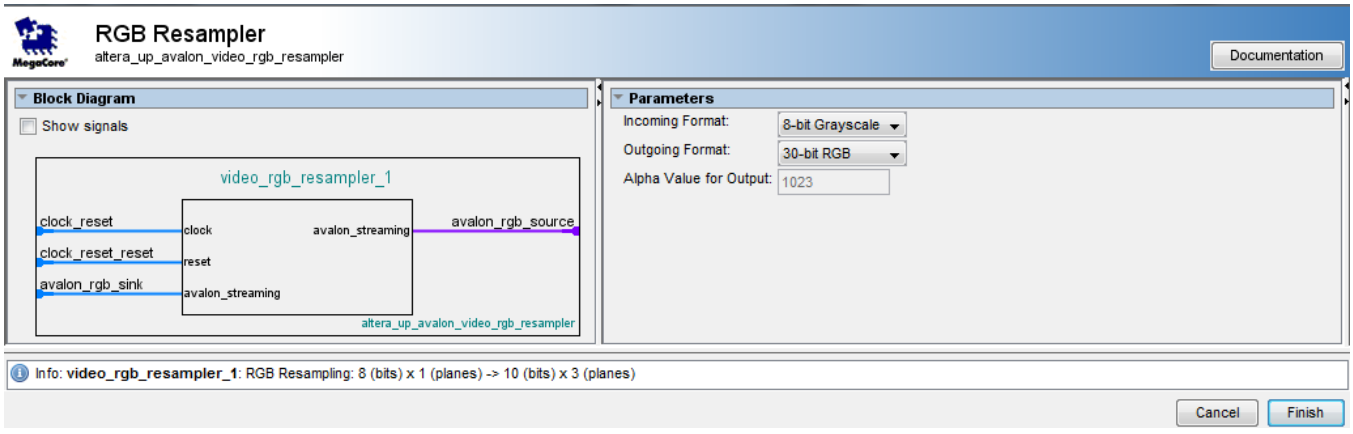
3. To change the input stream from colour to grayscale, Colour-Space Converter is used. Choose 24-bit RGB to Y.



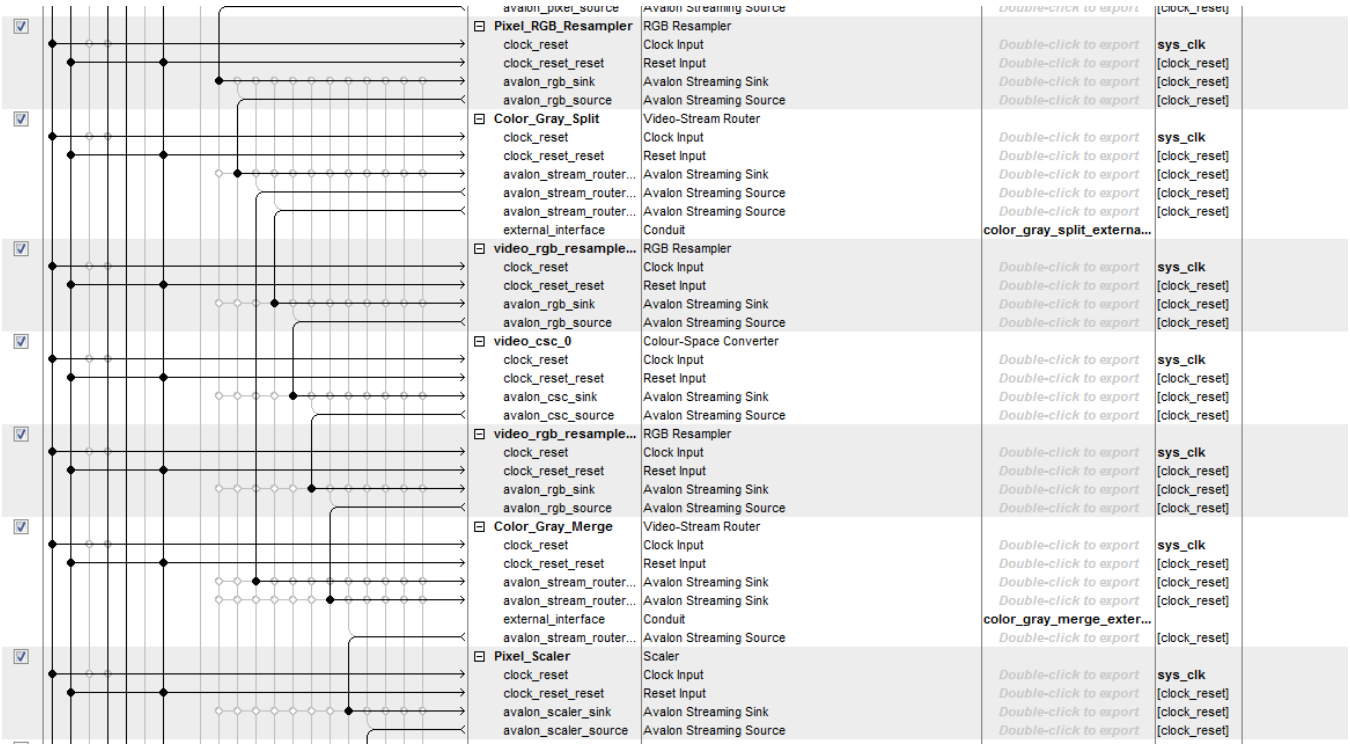
4. Since Colour-Space Converter only supports 24-bit RGB input, we need a RGB Resampler to convert the 30-bit RGB input stream to 24-bit.



5. Another RGB Resampler is needed to convert 8 bit Grayscale output from Colour-Space Converter to 30-bit RGB for VGA output.

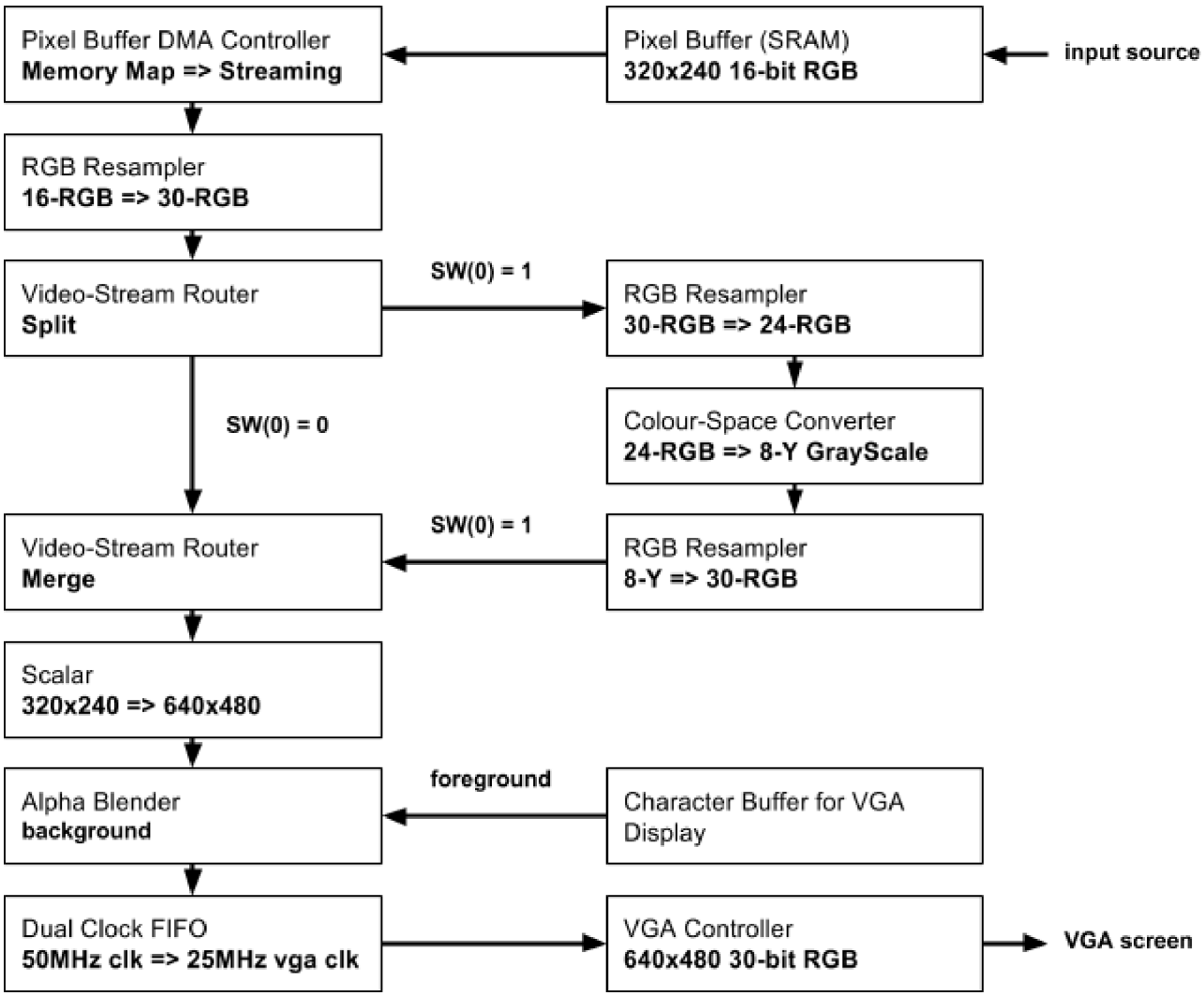


6. Connect the related components all together as follows. Add the new components between RGB Resampler and Scalar in the original design.



7. Generate and Compile the project. Once the Device had been programmed on the board, we can check the correctness by turning on and off SW(0), the default background on VGA screen will switch between colour and grayscale.

A flow diagram is included here to clarify the whole design.



Source Documentation and Reference

PIO: Chapter 10 of the Embedded Peripherals IP User Guide – Altera Quartus® II design software
ug_embedded_ip.pdf
altera_avalon_pio_regs.h

Altera University Program Video IP cores
file:///C:/altera/12.1sp1/ip/University_Program/Audio_Video/Video/doc/Video.pdf

Code modified from Hello MicroC/OS-II template from Nios II Software Build Tools for Eclipse.