Application Note – GPIO Internal Pull-Up Resistor

System: Quartus II V10.1 with Altera DE2 FPGA board

Description: The DE2 board provides a weak, internal pull-up resistor for all GPIO pins. Enabling it saves you from having to use external resistors for your project circuitry. The internal resistor is about 25 k Ω but will vary. Please note that the Bus Hold option for tri-stated pins must be OFF if you want to use the internal pull-up.

Steps:

• In Quartus II, click Assignments > Assignment Editor



• This shows all your component pins

4			Assignment Editor	×			
< <new>> Filter on node names: *</new>							
Ð	:atı	From	То	Assignment Name	Value	Enabled	
35	50 🖌		SD_CMD	Location	PIN_Y21	Yes	
35	51 🖌		DCLK	Location	PIN_AD25	Yes	
35	52 🖌		@ GPIO_0[0]	Location	PIN_D25	Yes	
35	53 🖌		GPIO_0[1]	Location	PIN_J22	Yes	
35	54 🖌		@ GPIO_0[2]	Location	PIN_E26	Yes	
35	55 🖌		@ GPIO_0[3]	Location	PIN_E25	Yes	
35	56 🖌		GPIO_0[4]	Location	PIN_F24	Yes	
35	57 🖌		GPIO_0[5]	Location	PIN_F23	Yes	
35	58 🖌		@ GPIO_0[6]	Location	PIN_J21	Yes	
35	59 🖌		@ GPIO_0[7]	Location	PIN_J20	Yes	

- Scroll to the bottom and double-click <<new>> under "To"
- Type in the name of your GPIO pin

	:atı	From	То	Assignment Name	Value	Enabled
434	~		D TD_HS	I/O Standard	3.3-V LVTTL	Yes
435	~		D TD_VS	I/O Standard	3.3-V LVTTL	Yes
436	-		AUD_ADCLRCK	I/O Standard	3.3-V LVTTL	Yes
437	-		AUD_ADCDAT	I/O Standard	3.3-V LVTTL	Yes
438	~		AUD_DACLRCK	I/O Standard	3.3-V LVTTL	Yes
439	-		AUD_DACDAT	I/O Standard	3.3-V LVTTL	Yes
440	-		AUD_XCK	I/O Standard	3.3-V LVTTL	Yes
441	~		AUD_BCLK	I/O Standard	3.3-V LVTTL	Yes
442	-		ENET_DATA[0]	I/O Standard	3.3-V LVTTL	Yes
443	~		SD_DAT3	I/O Standard	3.3-V LVTTL	Yes
444	-		FL_ADDR[20]	I/O Standard	3.3-V LVTTL	Yes
445	~		FL_ADDR[21]	I/O Standard	3.3-V LVTTL	Yes
446	1		@ GPIO_0[6]			Yes
447		< <new>></new>	< <new>></new>	< <new>></new>		

- Double-click the blank space under "Assignment Name"
- Scroll down and click on "Weak Pull-Up Resistor (Accepts wildcards/groups)"

Feb. 23, 2013

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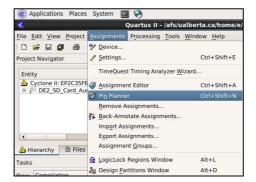
🎆 Applications Places System 🗾 🥱		👙 🎝 🖬 👘 Sat Feb 23, 3:15 PM		
K Quartus II - /afs/ualb	erta.ca/home/e/j/ejong/ece492/DE2_S	Passive Resistor		
Eile Edit View Project Assignments Processing Tools Wi	ndow <u>H</u> elp	Perform Asynchronous Signal Pipelining (Accepts wildcards/groups)		
🗅 🗃 🖬 🎒 🎒 🐰 🗞 🛍 🛍 🗠 🜼 DE2_SD_Card	_Audio 💠 🐹 🐓 🥒 🏈 🍕	Perform Logic to Memory Mapping for Fitting (Accepts wildcards/groups)		
Project Navigator Ø 8	Assignment E	Perform Physical Synthesis for Combinational Logic for Fitting (Accepts wildcards/groups)		
		Perform Physical Synthesis for Combinational Logic for Performance (Accepts wildcards/groups)		
Entity Logic Cells Dedicated Logic	< <new>> Filter on node names: *</new>	Perform Register Duplication for Performance (Accepts wildcards/groups)		
Cyclone II: EP2C35F672C6 DE2 SD Card Audio a 6457 (2) 3502 (0)	😨 ati From	Perform Register Retiming for Performance (Accepts wildcards/groups)		
_ He per DE2_SD_Card_Audio and 6457 (2) 3502 (0)	434 ✓ 🗊 TD_HS	Perform WYSIWYG Primitive Resynthesis		
	435 🖌 🗃 TD_VS	Power Analyzer Report Power Dissipation		
	436 🖌 🔍 AUD_AD	Power Analyzer Report Signal Activity		
	437 🖌 🖝 AUD_AD	Power Static Probability		
()	438 🖌 🛛 🐵 AUD_DA	Power Toggle Rate		
	439 🖌 💿 AUD_DA	Power Toggle Rate Percentage		
A Hierarchy 🖹 Files 🗗 Design Units		Power-Up Level (Accepts wildcards/groups)		
asks Ø 🕱		PowerPlay Power Optimization		
low: Compilation Customize		Preserve Fan-out Free Register Node		
Iow: Compilation Customize		Preserve Pan-out Free Register Node Preserve PLL Counter Order (Accepts wildcards/groups)		
Task Ó Ti		Preserve PLL Counter Order (Accepts wildcards/groups) Preserve Registers (Accepts wildcards/groups)		
✓ 🖞 🕨 Compile Design		ODR D Pin Group (Accepts wildcards/groups)		
	447 < <new>> <<new>></new></new>			
 ✓ B ► Assembler (Generate programming files) 	(•	Remove Duplicate Registers		
✓ ImeQuest Timing Analysis	Enables the weak pull-up resistor	Remove Redundant Logic Cells		
EDA Netlist Writer	Pull-Up Resistor option should no	Reserve Pin		
Program Device (Open Programmer)	: anything other than a pin. 드	Restructure Multiplexers		
	<u> </u>	Safe State Machine		
Type Message		Setup and Hold Time Violation Detection		
Critical Warning: Setting INCREMENTAL_COMPIL		Shift Register Replacement - Allow Asynchronous Clear Signal		
 i) Info: Started Programmer operation at Sat Fe i) Info: Configuring device index 1 	b 23 15:10:42 2013	Show 'X' on timing violation		
Info: Device 1 contains JTAG ID code 0x020B4	DD	Speed Optimization Technique for Clock Domains		
- Ú Info: Configuration succeeded 1 device(s)	configured	State Machine Processing		
 i) Info: Successfully performed operation(s) i) Info: Ended Programmer operation at Sat Feb 	23 15.10.44 2013	Strict RAM Replacement		
Vinter inder regenmet operation at out res		Synchronization Register Chain Length (Accepts wildcards/groups)		
		Synchronizer Toggle Rate (Accepts wildcards/groups)		
3 4		- Termination (Accepts wildcards/groups)		
System (7) / Processing / Extra Info / Info / Warning	\ Critical Warning /\ Error /\ Suppressed	Timing-Driven Synthesis		
Message: 0 of 7 🏦 😽 Location:		Virtual Pin		
		Weak Pull-Up Resistor (Accepts wildcards/groups)		
	and a weather with a state back for an	ance bus signal to VCC. The Weak Pull-Up Resistor option should not be used at the same time as the Enable I		

- Click and change "Value" to On
- "Enabled" should be Yes by default
- Ensure that the name listed under "Entity" is your top level

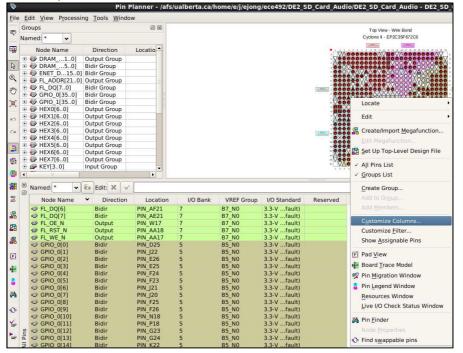
	:atı	From	То	Assignment Name	Value	Enabled	Entity
434	~	l.	D TD_HS	I/O Standard	3.3-V LVTTL	Yes	
435	~		D TD_VS	I/O Standard	3.3-V LVTTL	Yes	
436	~		AUD_ADCLRCK	I/O Standard	3.3-V LVTTL	Yes	
437	~		AUD_ADCDAT	I/O Standard	3.3-V LVTTL	Yes	
438	~		AUD_DACLRCK	I/O Standard	3.3-V LVTTL	Yes	
439	~	1	AUD_DACDAT	I/O Standard	3.3-V LVTTL	Yes	
440	~		AUD_XCK	I/O Standard	3.3-V LVTTL	Yes	
441	-		AUD_BCLK	I/O Standard	3.3-V LVTTL	Yes	
442	~		ENET_DATA[0]	I/O Standard	3.3-V LVTTL	Yes	
443	~		SD_DAT3	I/O Standard	3.3-V LVTTL	Yes	
444	~		FL_ADDR[20]	I/O Standard	3.3-V LVTTL	Yes	
445	45 🖌 🐵 FL ADDR[21]		I/O Standard	3.3-V LVTTL	Yes		
446	1		GPIO_0[6]	Weak Pull-Up Resistor		Yes	DE2_SAudio
447		< <new>></new>	< <new>></new>	< <new>></new>	Off		
					On		

• Done! You can review your edits under Pin Planner in Quartus II

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Right-click anywhere and select "Customize Columns..."

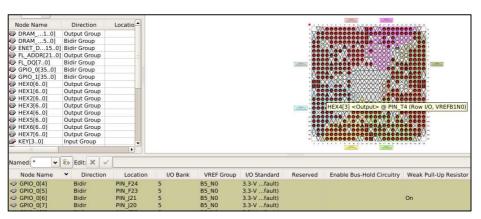


• Move "Enable Bus-Hold Circuitry" and "Weak Pull-Up Resistor" to the right window

Customize Columns Customize the columns displayed in the node list. Available columns: Show these columns in this order:						
Clock Settings Current Strength Cyclone II Termination Differential Pair		<	Direction Location I/O Bank VREF Group	Cancel		
Enable Exclusive I/O Group Fast Input Register			I/O Standard Reserved Enable Bus-Hold Circuitry	Move Up		
Fast Output Enable Register			Weak Pull-Up Resistor	Move Down		
Fast Output Register General Function	-			Help		

- Ensure the bus-hold isn't ON if your internal resistor is (should be OFF by default)
- You can also set your resistors(s) here and see it reflected in "Assignment Editor"

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Example multimeter readings with a simple on/off switch:

- Power supply from GPIO pin 29: 3.310 vdc
- GPIO pin without internal resistor: 1.071 vdc
- GPIO pin with internal resistor: 3.072 vdc

References:

1. <u>http://www.altera.com/support/devices/io/features/io-features.html#ProgrammablePullupResistor</u>

Programmable Pull-up Resistor

When to Use

- Use when there is a need to pull a pin signal level to V_{CCIO} when it is tri-stated.
- Use to replace a weak external pull-up resistor. The pull-up resistance varies with process, voltage, and temperature conditions.
- Use external components if you require precision values.
- Use in combination with open-drain output option.

How to Use

 In the Assignment Editor, set the weak pull-up assignment to ON to enable the on-chip pull-up resistor for the pin.

Feature Availability

All user I/Os.

Feature Limitations

- Not supported in dedicated configuration pins and dedicated clock input pins.
- Not available in pins that are using bus hold option.

2. http://www.altera.com/literature/hb/cyc2/cyc2_cii5v1.pdf

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Programmable Pull-Up Resistor

Each Cyclone II device I/O pin provides an optional programmable pull-up resistor during user mode. If you enable this feature for an I/O pin, the pull-up resistor (typically 25 k Ω) holds the output to the V_{CCIO} level of the output pin's bank.

If the programmable pull-up is enabled, the device cannot use the bus-hold feature. The programmable pull-up resistors are not supported on the dedicated configuration, JTAG, and dedicated clock pins.

> 2–51 Cyclone II Device Handbook, Volume 1

- PIO B26 PIO B22 IO B23 PIO B24 PIO B25 D3 B33 B35 RAT54 RAT545 (GPIO 0) RN3 5 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38 40 9 11 13 15 17 19 21 23 25 27 29 31 33 35 37 39 VCC5 47 N33 VCC33r BOX 2X20 47
- 3. http://www.cs.columbia.edu/~%20sedwards/classes/2013/4840/DE2_schematics.pdf